HN29W256H02TE-1

Controller for AND Flash Memory

HITACHI

ADE-203-1040B (Z)
Rev. 2.0
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Description

HN29W256H02TE-1 is a controller IC for flash ATA card. This IC is manufactured using Hitachi 0.5 µm CMOS technology, and integrates control logic with SH1•CPU core. This IC is able to control maximum 32 pieces of Hitachi 256 Mega bit Flash Memory HN29W25611, and is used to build Flash ATA Card and CompactFlash™.

Features

- Comform to PC-ATA Card and CompactFlash™ specification standard
- Control maximum 32 pieces of Hitachi 256 Mega bit Flash memory HN29W25611
- Operate by 3.3 V or 5 V single power supply
- Support card density up to 1024 Mega bytes
- Execute internal self-diagnostic program at V_{CC} power on
- Operate in 3 modes
  - — Memory Card Mode
  - — I/O Card Mode
  - — True-IDE Mode
- Assure a high reliability based on the internal ECC (Error Correcting Code) function
- Support Auto Sleep Mode
- Support interleave operation

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*CFA: CompactFlash™ Association.

Pin Assignment

		Memory card mode		I/O card mode		True IDE mode		
NO.	Controller	Signal name	I/O	Signal name	I/O	Signal name	I/O	Remarks*1
1	H_OEB	–OE	I	–OE	I	–ATASTEL	I	PT5D21
2	H_A[10]	A10	I	A10	I	A10	I	PT5D01
3	H_CE2B	–CE2	I	–CE2	I/O	–CE2	I/O	PT5D21V
4	H_CE1B	–CE1	I	–CE1	I	–CE1	I	PT5D21V
5	H_D[15]	D15	I/O	D15	I/O	D15	I/O	PT5BH3CX
6	H_D[7]	D07	I/O	D07	I/O	D07	I/O	PT5BH3CX
7	H_D[14]	D14	I/O	D14	I/O	D14	I/O	PT5BH3CX
8	GND	GND	—	GND	—	GND	—	PV0AL
9	H_D[6]	D06	I/O	D06	I/O	D06	I/O	PT5BH3CX
10	H_D[13]	D13	I/O	D13	I/O	D13	I/O	PT5BH3CX
11	H_D[5]	D05	I/O	D05	I/O	D05	I/O	PT5BH3CX
12	H_D[12]	D12	I/O	D12	I/O	D12	I/O	PT5BH3CX
13	H_D[4]	D04	I/O	D04	I/O	D04	I/O	PT5BH3CX
14	H_D[11]	D11	I/O	D11	I/O	D11	I/O	PT5BH3CX
15	H_D[3]	D03	I/O	D03	I/O	D03	I/O	PT5BH3CX
16	VDD	VDD	—	VDD	—	VDD	—	PV3I
17	TEST1	—	I	—	I	—	I	—
18	PORST_	PORST	I	PORST	I	PORST	I	PC3D21
19	TEST2	—	I	—	I	—	I	PC3D21U
20	TEST3	—	I	—	I	—	I	PC3D21U
21	GND	GND	—	GND	—	GND	—	PV0I
22	XIN	XIN	I	XIN	I	XIN	I	PC3X11H
23	XOUT	XOUT	O	XOUT	O	XOUT	O	PC3X11OH
24	GND	GND	—	GND	—	GND	—	PV0A
25	VDD	VDD	—	VDD	—	VDD	—	PV3A
26	TEST4	—	O	—	O	—	O	PC3O01C
27	TEST5	—	O	—	O	—	O	PC3O01C
28	TEST6	—	O	—	O	—	O	PC3O01C
29	TEST7	—	O	—	O	—	O	PC3O01C
30	TEST8	—	O	—	O	—	O	PC3O01C

Pin Assignment (cont.)

		Memory card mode		I/O card mode		True IDE mode		
NO.	Controller	Signal name	I/O	Signal name	I/O	Signal name	I/O	Remarks*[1]
31	TEST9	—	O	—	O	—	O	PC3O01C
32	TEST10	—	O	—	O	—	O	PC3O01C
33	TEST11	—	O	—	O	—	O	PC3O01C
34	GND	GND	—	GND	—	GND	—	PV0A
35	TEST12	—	O	—	O	—	O	PC3O01C
36	TEST13	—	O	—	O	—	O	PC3O01C
37	F_CDE_BB	F_CDE_BB	O	F_CDE_BB	O	F_CDE_BB	O	PC3O03C
38	F_WE_B0B	F_WE_B0B	O	F_WE_B0B	O	F_WE_B0B	O	PC3O03C
39	F_WE_B1B	F_WE_B1B	O	F_WE_B1B	O	F_WE_B1B	O	PC3O03C
40	F_SC_B0	F_SC_B0	O	F_SC_B0	O	F_SC_B0	O	PC3O03C
41	F_SC_B1	F_SC_B1	O	F_SC_B1	O	F_SC_B1	O	PC3O03C
42	F_D_B[7]	F_D_B[7]	I/O	F_D_B[7]	I/O	F_D_B[7]	I/O	PC3B43UC
43	F_D_B[6]	F_D_B[6]	I/O	F_D_B[6]	I/O	F_D_B[6]	I/O	PC3B43UC
44	F_D_B[5]	F_D_B[5]	I/O	F_D_B[5]	I/O	F_D_B[5]	I/O	PC3B43UC
45	F_D_B[4]	F_D_B[4]	I/O	F_D_B[4]	I/O	F_D_B[4]	I/O	PC3B43UC
46	VDD	VDD	—	VDD	—	VDD	—	PV3I
47	TEST14	—	—	—	—	—	—	—
48	GND	GND	—	GND	—	GND	—	PV0A
49	VDD	VDD	—	VDD	—	VDD	—	PV3I
50	F_D_B[3]	F_D_B[3]	I/O	F_D_B[3]	I/O	F_D_B[3]	I/O	PC3B43UC
51	GND	GND	—	GND	—	GND	—	PV0I
52	F_D_B[2]	F_D_B[2]	I/O	F_D_B[2]	I/O	F_D_B[2]	I/O	PC3B43UC
53	F_D_B[1]	F_D_B[1]	I/O	F_D_B[1]	I/O	F_D_B[1]	I/O	PC3B43UC
54	F_D_B[0]	F_D_B[0]	I/O	F_D_B[0]	I/O	F_D_B[0]	I/O	PC3B43UC
55	F_OE_B0B	F_OE_B0B	O	F_OE_B0B	O	F_OE_B0B	O	PC3O03C
56	F_OE_B1B	F_OE_B1B	O	F_OE_B1B	O	F_OE_B1B	O	PC3O03C
57	F_RSTB	F_RSTB	O	F_RSTB	O	F_RSTB	O	PC3O03C
58	F_RDY	F_RDY	I	F_RDY	I	F_RDY	I	PC3D21U
59	F_CEB[0]	F_CEB_0	O	F_CEB_0	O	F_CEB_0	O	PC3O03C
60	F_CEB[1]	F_CEB_1	O	F_CEB_1	O	F_CEB_1	O	PC3O03C

Pin Assignment (cont.)

		Memory card mode		I/O card mode		True IDE mode		
NO.	Controller	Signal name	I/O	Signal name	I/O	Signal name	I/O	Remarks*[1]
61	F_CEB[2]	F_CEB_2	O	F_CEB_2	O	F_CEB_2	O	PC3O03C
62	F_CEB[3]	F_CEB_3	O	F_CEB_3	O	F_CEB_3	O	PC3O03C
63	F_CEB[4]	F_CEB_4	O	F_CEB_4	O	F_CEB_4	O	PC3O03C
64	F_CEB[5]	F_CEB_5	O	F_CEB_5	O	F_CEB_5	O	PC3O03C
65	GND	GND	—	GND	—	GND	—	PV0A
66	F_CEB[6]	F_CEB_6	O	F_CEB_6	O	F_CEB_6	O	PC3O03C
67	F_CEB[7]	F_CEB_7	O	F_CEB_7	O	F_CEB_7	O	PC3O03C
68	F_CDE_AB	F_CDE_AB	O	F_CDE_AB	O	F_CDE_AB	O	PC3O03C
69	GND	GND	—	GND	—	GND	—	PV0I
70	F_WE_A0B	F_WE_A0B	O	F_WE_A0B	O	F_WE_A0B	O	PC3O03C
71	F_WE_A1B	F_WE_A1B	O	F_WE_A1B	O	F_WE_A1B	O	PC3O03C
72	F_SC_A0	F_SC_A0	O	F_SC_A0	O	F_SC_A0	O	PC3O03C
73	F_SC_A1	F_SC_A1	O	F_SC_A1	O	F_SC_A1	O	PC3O03C
74	F_D_A[7]	F_D_A7	I/O	F_D_A7	I/O	F_D_A7	I/O	PC3B43UC
75	F_D_A[6]	F_D_A6	I/O	F_D_A6	I/O	F_D_A6	I/O	PC3B43UC
76	VDD	VDD	—	VDD	—	VDD	—	PV3A
77	F_D_A[5]	F_D_A5	I/O	F_D_A5	I/O	F_D_A5	I/O	PC3B43UC
78	F_D_A[4]	F_D_A4	I/O	F_D_A4	I/O	F_D_A4	I/O	PC3B43UC
79	F_D_A[3]	F_D_A3	I/O	F_D_A3	I/O	F_D_A3	I/O	PC3B43UC
80	F_D_A[2]	F_D_A2	I/O	F_D_A2	I/O	F_D_A2	I/O	PC3B43UC
81	GND	GND	—	GND	—	GND	—	PV0A
82	F_D_A[1]	F_D_A1	I/O	F_D_A1	I/O	F_D_A1	I/O	PC3B43UC
83	F_D_A[0]	F_D_A0	I/O	F_D_A0	I/O	F_D_A0	I/O	PC3B43UC
84	F_OE_A0B	F_OE_A0B	O	F_OE_A0B	O	F_OE_A0B	O	PC3O03C
85	F_OE_A1B	F_OE_A1B	O	F_OE_A1B	O	F_OE_A1B	O	PC3O03C
86	TEST15	—	—	—	—	—	—	—
87	VCC	VCC	—	VCC	—	VCC	—	PV5IL
88	H_D[10]	D10	I/O	D10	I/O	D10	I/O	PT5BH3CX
89	H_IOIS16B	WP	O	–IOIS16	O	–IOIS16	O	PT5N03C
90	H_D[9]	D9	I/O	D9	I/O	D9	I/O	PT5BH3CX

Pin Assignment (cont.)

		Memory card mode		I/O card mode		True IDE mode		
NO.	Controller	Signal name	I/O	Signal name	I/O	Signal name	I/O	Remarks*1
91	H_D[2]	D2	I/O	D2	I/O	D2	I/O	PT5BH3CX
92	H_D[8]	D8	I/O	D8	I/O	D8	I/O	PT5BH3CX
93	GND	GND	—	GND	—	GND	—	PV0AL
94	H_D[1]	D1	I/O	D1	I/O	D1	I/O	PT5BH3CX
95	H_STSCHGB	BVD1	I/O	–STSCHG	I/O	–PDIAG	I/O	PT5B43VX
96	H_D[0]	D0	I/O	D0	I/O	D0	I/O	PT5BH3CX
97	DASP	BVD2	I/O	–SPKR	I/O	–DASP	I/O	PT5B43VX
98	H_A[0]	A0	I	A0	I	A0	I	PT5D01
99	H_REGB	–REG	I	–REG	I	–REG	I	PT5D21V
100	H_A[1]	A1	I	A1	I	A1	I	PT5D01
101	H_INPACKB	–INPACK	O	–INPACK	O	–INPACK	O	PT5T43C
102	H_A[2]	A2	I	A2	I	A2	I	PT5D01
103	H_WAITB	–WAIT	O	–WAIT	O	IORDY	O	PT5B43C
104	H_A[3]	A3	I	A3	I	A3	I	PT5D01
105	H_RESET	RESET	I	RESET	I	–RESET	I	PT5D01
106	VCC	VCC	—	VCC	—	VCC	—	PV5AL
107	H_A[4]	A4	I	A4	I	A4	I	PT5D01
108	H_A[5]	A5	I	A5	I	A5	I	PT5D01
109	CSEL	–CSEL	I	–CSEL	I	–CSEL	I	PT5B43C
110	TEST16	—	I/O	—	I/O	—	I/O	PT5B43VX
111	GND	GND	—	GND	—	GND	—	PV0AL
112	H_A[6]	A6	I	A6	I	A6	I	PT5D01
113	H_IREQB	RDY/–BSY	O	–IREQ	O	INTRQ	O	PT5T43C
114	H_A[7]	A7	I	A7	I	A7	I	PT5D01
115	H_WEB	–WE	I	–WE	I	–WE	I	PT5D21V
116	H_A[8]	A8	I	A8	I	A8	I	PT5D01
117	H_IOWRB	–IOWR	I	–IOWR	I/O	–IOWR	I/O	PT5D21V
118	GND	GND	—	GND	—	GND	—	PV0IL
119	H_A[9]	A9	I	A9	I	A9	I	PT5D01
120	H_IORDB	–IORD	I	–IORD	I/O	–IORD	I/O	PT5D21V

Note: 1. Type of input/output buffer

PT5D01	:	TTL level input (level sifter)
PT5D21	:	TTL schmitt input (level sifter)
PT5D21V	:	TTL schmitt input with 100 kΩ pull-up resister (level sifter)
PT5BH3CX	:	TTL level input/output (level sifter output, 2 mA/3 mA)
PT5B43VX	:	TTL level input/output with 100 kΩ pull-up resister (level sifter output, 2 mA/3 mA)
PT5B43C	:	TTL level input/output (level sifter, 3 mA)
PT5N03C	:	Open drain output (level sifter, 3 mA)
PT5T43C	:	3-state output (level sifter, 3 mA)
PC3D21	:	CMOS level schmitt input
PC3D21U	:	CMOS level schmitt input with pull-up resister
PC3O01C	:	Totempole output (1 mA)
PC3O03C	:	Totempole output (3 mA)
PC3B43UC	:	CMOS level input/output with pull-up resister (3 mA)
PC3X11H	:	Crystal OSC input
PC3X11OH	:	Crystal OSC output
PV0A	:	Output GND
PV0I	:	Core and iuput GND
PV3A	:	Output VCC
PV3I	:	Core and input VCC
PV0AL	:	Output GND (level sifter)
PV0IL	:	Core and iuput GND (level sifter)
PV5AL	:	Output VCC (level sifter)
PV5IL	:	Core and input VCC (level sifter)

Host Interface Pin Explanation

Signal name	Direction	Pin No.	Description
A10 to A0 (PC Card Memory mode)	I	2, 119, 116, 114, 112, 108, 107, 104, 102, 100, 98	Address bus is A10 to A0. A10 is MSB and A0 is LSB.
A10 to A0 (PC Card I/O mode)			
A2 to A0 (True IDE mode)		102, 100, 98	Address bus is A10 to A0. Only A2 to A0 are used, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory mode)	I/O	95	BVD1 outputs the battery voltage status in the card. This output line is constantly driven to a high state since a battery is not required for this product.
-STSCHG (PC Card I/O mode)			-STSCHG is used for changing the status of Configuration and status register in attribute area.
-PDIAG (True IDE mode)			-PDIAG is the Pass Diagnostic signal in Master/Slave handshake protocol.
BVD2 (PC Card Memory mode)	I/O	97	BVD2 outputs the battery voltage status in the card. This output line is constantly driven to a high state since a battery is not required for this product.
-SPKR (PC Card I/O mode)			-SPKR outputs speaker signals. This output line is constantly driven to a high state since this product does not support the audio function.
-DASP (True IDE mode)			-DASP is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CE1, -CE2 (PC Card Memory mode) Card Enable	I	3, 4	-CE1 and -CE2 are low active card select signals. Byte/Word/Odd byte mode are defined by combination of -CE1, -CE2 and A0.
-CE1, -CE2 (PC Card I/O mode) Card Enable			
-CE1, -CE2 (True IDE mode)			-CE2 is used for select the Alternate Status Register and the Device Control Register while -CE1 is the chip select for the other task file registers.
-CSEL (PC Card Memory mode)	I	109	This signal is not used.
-CSEL (PC Card I/O mode)			
-CSEL (True IDE mode)			This signal is used to configure this device as a Master or a Slave when configured in the True IDE mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Signal name	Direction	Pin No.	Description
D15 to D0 (PC Card Memory mode)	I/O	5, 7, 10, 12, 14, 88, 90, 92, 6, 9, 11, 13, 15, 91, 94, 96	Data bus is D15 to D0. D0 is the LSB of the even byte of the word. D8 is the LSB of the odd byte of the word.
D15 to D0 (PC Card I/O mode)			
D15 to D0 (True IDE mode)			
GND (PC Card Memory mode)	—	8, 21, 24, 34, 48, 51, 65, 69, 81, 93, 111, 118	Ground
GND (PC Card I/O mode)			
GND (True IDE mode)			
-INPACK (PC Card Memory mode)	O	101	This signal is not used and should not be connected at the host.
-INPACK (PC Card I/O mode) Input Acknowledge			This signal is asserted low by this card when the card is selected and responding to an I/O read cycle at the address that is on the address bus during -CE and -IORD are low. This signal is used for the input data buffer control.
-INPACK (True IDE mode)			This signal is not used and should not be connected at the host.
-IORD (PC Card Memory mode)	I	120	This signal is not used.
-IORD (PC Card I/O mode)			-IORD is used for control of read data in I/O task file area. This card does not respond to -IORD until I/O card interface setting up.
-IORD (True IDE mode)			-IORD is used for control of read data in I/O task file area. This card does not respond to -IORD until True IDE interface setting up.
-IOWR (PC Card Memory mode)	I	117	This signal is not used.
-IOWR (PC Card I/O mode)			-IOWR is used for control of data write in I/O task file area. This card does not respond to -IOWR until I/O card interface setting up.
-IOWR (True IDE mode)			-IOWR is used for control of data write in I/O task file area. This card does not respond to -IOWR until True IDE interface setting up.

Signal name	Direction	Pin No.	Description
-OE (PC Card Memory mode)	I	1	-OE is used for the control of reading register's data in attribute area or task file area.
-OE (PC Card I/O mode)			-OE is used for the control of reading register's data in attribute area.
-ATASEL (True IDE mode)			To enable True IDE mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory mode)	O	113	The signal is RDY/-BSY pin. RDY/-BSY pin turns low level during the card internal initialization operation at VCC applied or reset applied, so next access to the card should be after the signal turned high level.
-IREQ (PC Card I/O mode)			This signal is active low -IREQ pin. The signal of low level indicates that the card is requesting software service to host, and high level indicates that the card is not requesting.
INTRQ (True IDE mode)			This signal is the active high Interrupt Request to the host.
-REG (PC Card Memory mode) Attribute memory select	I	99	-REG is used during memory cycles to distinguish between task file and attribute memory accesses. High for task file, Low for attribute memory is accessed.
-REG (PC Card I/O mode)			-REG is constantly low when task file or attribute memory is accessed.
-REG (True IDE mode)			This input signal is not used and should be connected to VCC.
RESET (PC Card Memory mode)	I	105	This signal is active high RESET pin. If this signal is asserted high, the card internal initialization begins to operate. During the card internal initialization RDY/-BSY is low. After the card internal initialization RDY/-BSY is high.
RESET (PC Card I/O mode)			This signal is active high RESET pin. If this signal is asserted high, the card internal initialization begins to operate. In this mode, RDY/-BSY signal can not be used, so using Status Register the Ready/Busy status can be confirmed.
-RESET (True IDE mode)			This signal is active low -RESET pin. If this signal is asserted low, all the register's in this card are reset. In this mode, RDY/-BSY signal can not be used, so using status register the Ready/Busy status can be confirmed.

Signal name	Direction	Pin No.	Description
VCC/VDD (PC Card Memory mode)	—	16, 25, 46, 49, 76, 87, 106	+5 V, +3.3 V power.
VCC/VDD (PC Card I/O mode)			
VCC/VDD (True IDE mode)			
-WAIT (PC Card Memory mode)	O	103	This signal is active low -WAIT pin. In this card this signal is constantly high level.
-WAIT (PC Card I/O mode)			
IORDY (True IDE mode)			This output signal may be used as IORDY. In this card this signal is constantly high impedance.
-WE (PC Card Memory mode)	I	115	-WE is used for the control of writing register's data in attribute memory area or task file area.
-WE (PC Card I/O mode)			-WE is used for the control of writing register's data in attribute memory area.
-WE (True IDE mode)			This input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory mode) Write Protect	O	89	WP is held low because this card does not have write protect switch.
-IOIS16 (PC Card I/O mode)			-IOIS16 is asserted when task file registers are accessed in 16-bit mode.
-IOIS16 (True IDE mode)			This output signal is asserted low when this device is expecting a word data transfer cycle. Initial mode is 16-bit. If the user issues a Set Feature Command to put the device in Byte access mode, the card permits 8-bit accesses.

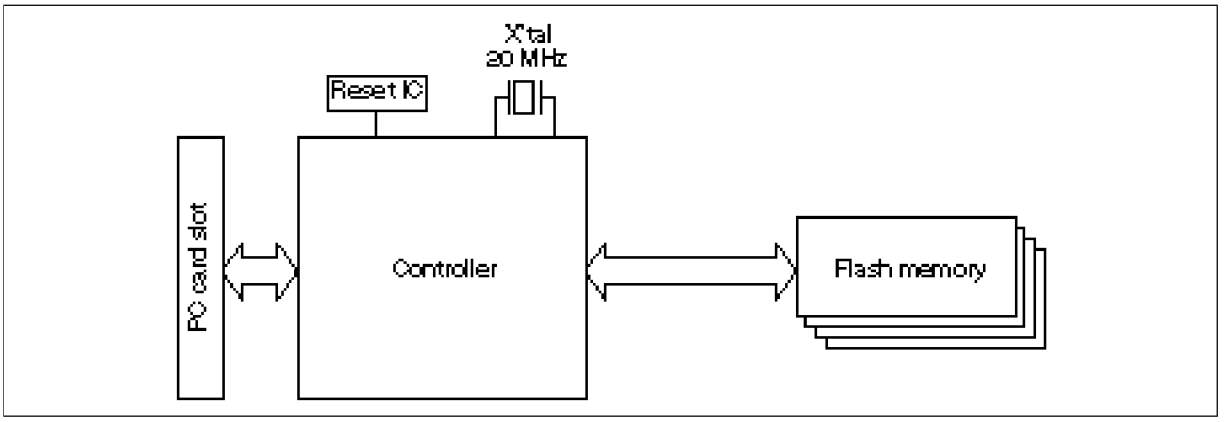
Flash Memory Interface Pin Explanation

Signal name	Direction	Pin No.	Description
F_D_A[0] to F_D_A[7] F_D_B[0] to F_D_B[7]	I/O	83, 82, 80, 79, 78, 77, 75, 74, 54, 53, 52, 50, 45, 44, 43, 42	This bus is used as command, address and data bus for flash memory.
F_CEB[0] to F_CEB[7]	O	59, 60, 61, 62, 63, 64, 66, 67	Flash chip enable is used to select the flash memory.
F_OE_A0B, F_OE_A1B, F_OE_B0B, F_OE_B1B	O	84, 85, 55, 56	Flash output enable is used to control read data output from the flash memory.
F_WE_A0B, F_WE_A1B, F_WE_B0B, F_WE_B1B	O	70, 71, 38, 39	Flash write enable is used to strobe command and address. The command and address are latched at the rising edge of the flash write enable.
F_SC_A0, F_SC_A1, F_SC_B0, F_SC_B1	O	72, 73, 40, 41	Serial clock is used to read memory data and strobe programming data. The programming data is lached at the rising edge of the serial clock.
F_RSTB	O	57	Flash reset must be kept at V_{ILR} (VSS ± 0.2 V) while VCC is turned on and off to prevent flash memory from unintentional erase or programming. Flash reset must be lept at V_{IHR} (VCC ± 0.2 V) after VCC becomes stable and flash memory is in various operation such as programming, erase and read.
F_CDE_AB, F_CDE_BB	O	68, 37	Command data enable is used to control the multiplexed flash bus when flash write enable is asserted. Command and data are latched when command data is low, and address is latched when command data enable is high.
F_RDY	I	58	Flash ready/busy is driven low by flash memory during program or erase operation. Flash ready/busy becomes high impedance at the completion of the program or erase operation.

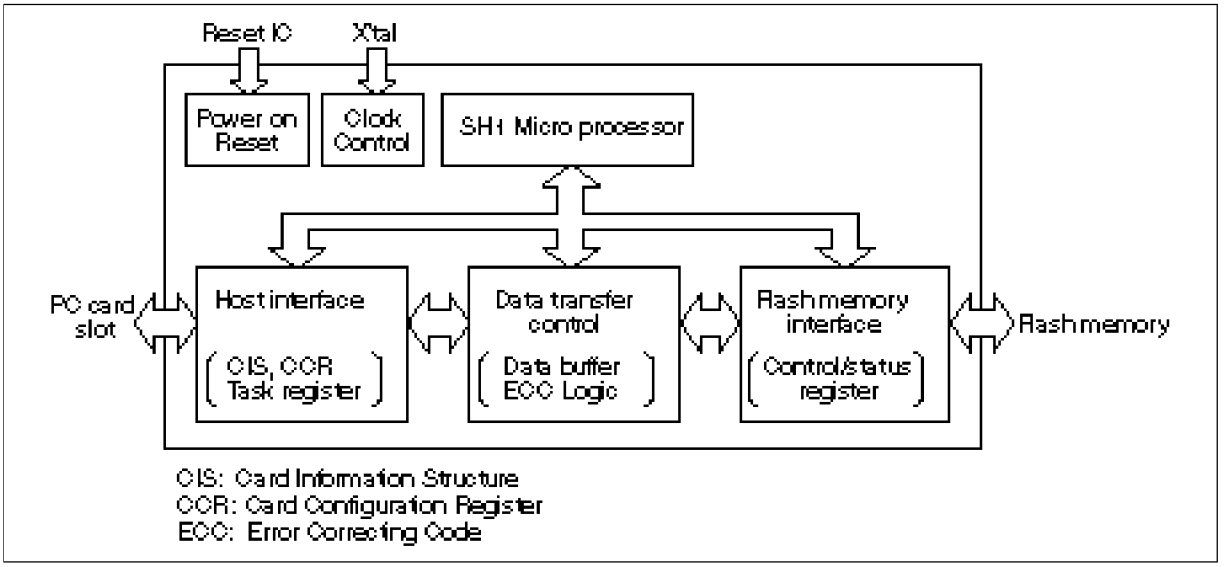
Other Pin Explanation

Signal name	Direction	Pin No.	Description
XIN, XOUT	I/O	22, 23	XIN and XOUT are used to connect crystal oscillator.
PORST_	I	18	This pin is used to connect reset IC for power on reset.
TEST1	I	17	TEST1 is used for diagnostic test, and should be kept at VDD.
TEST2 to TEST16	I	19, 20, 26, 27, 28, 29, 30, 31, 32, 33, 35, 36, 47, 86, 110	TEST2 to TEST16 are used for diagnostic test, and should be open.

Card Block Diagram



Controller Block Diagram



Note: The HITACHI Flash controller recover from 3-symbol errors of the data field (512-byte + 8-byte: ECC) and 2-symbol error of control field (32-byte) during read operation.

Host Access Specifications

1. Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of -REG = "L" as follows. That region can be accessed by Byte/Word/Odd-byte modes which are defined by PC card standard specifications.

Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	invalid
Word access (16-bit)	L	L	L	×	L	H	invalid	even byte
Odd byte access (8-bit)	L	L	H	×	L	H	invalid	High-Z

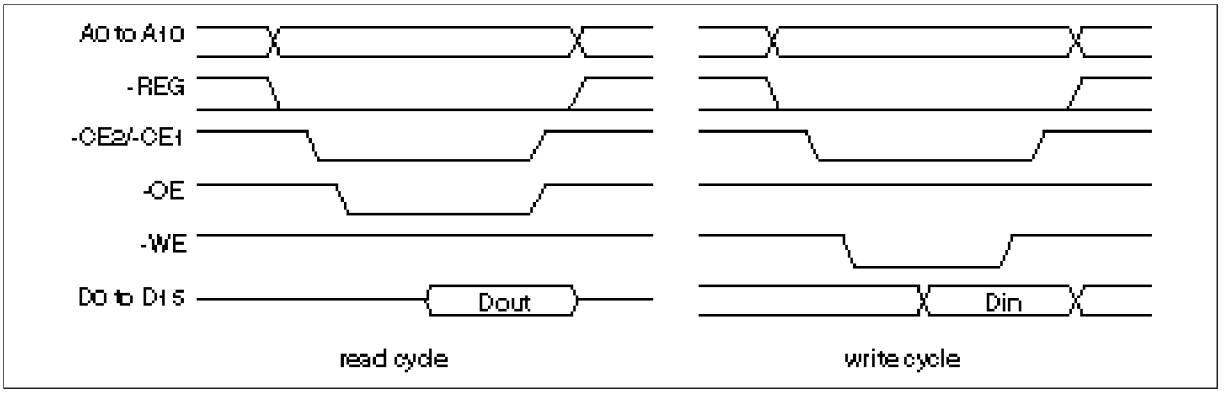
Note: ×: L or H

Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	Don't care	even byte
	L	H	L	H	H	L	Don't care	Don't care
Word access (16-bit)	L	L	L	×	H	L	Don't care	even byte
Odd byte access (8-bit)	L	L	H	×	H	L	Don't care	Don't care

Note: ×: L or H

Attribute Access Timing Example



2. Task File register access specifications

There are two cases of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each case of Task File register read and write operations are executed under the condition as follows. That area can be accessed by Byte/Word/Odd Byte mode which are defined by PC card standard specifications.

(1) I/O address map

Task File Register Read Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16-bit)	L	L	L	×	L	H	H	H	odd byte	even byte
Odd byte access (8-bit)	L	L	H	×	L	H	H	H	odd byte	High-Z

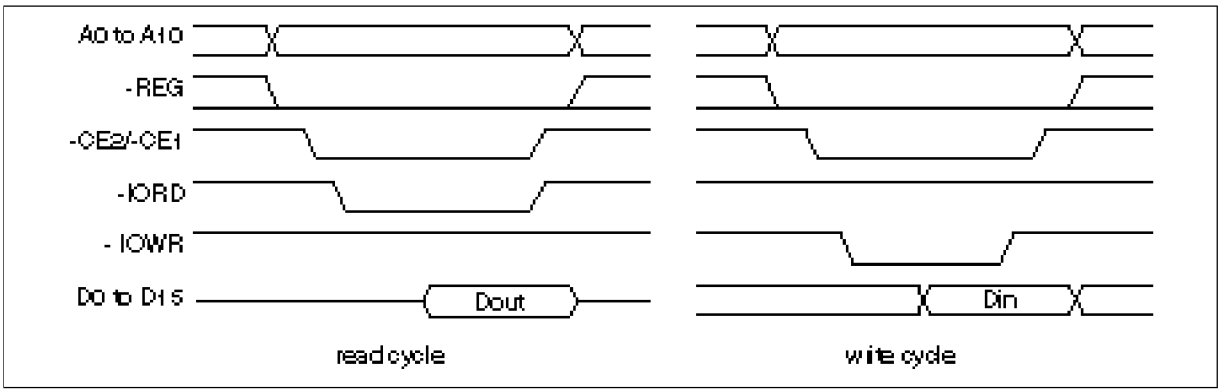
Note: ×: L or H

Task File Register Write Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16-bit)	L	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access (8-bit)	L	L	H	×	H	L	H	H	odd byte	Don't care

Note: ×: L or H

Task File Register Access Timing Example (1)



(2) Memory address map

Task File Register Read Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	High-Z	High-Z
Byte access (8-bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16-bit)	H	L	L	×	L	H	H	H	odd byte	even byte
Odd byte access (8-bit)	H	L	H	×	L	H	H	H	odd byte	High-Z

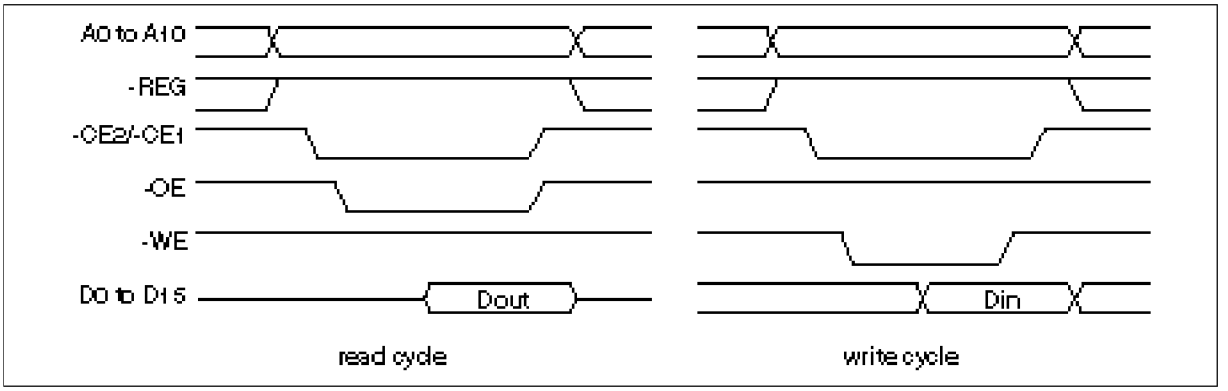
Note: ×: L or H

Task File Register Write Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access (8-bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16-bit)	H	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access (8-bit)	H	L	H	×	H	L	H	H	odd byte	Don't care

Note: ×: L or H

Task File Register Access Timing Example (2)



3. True IDE Mode

The card can be configured in a True IDE mode of operation. This card is configured in this mode only when the -OE input signal is asserted GND by the host. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operation to the task file and data register are allowed. If this card is configured during power on sequence, data register are accessed in word (16-bit). The card permits 8-bit accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	×	×	×	High-Z	High-Z
Standby mode	H	H	×	×	×	High-Z	High-Z
Data register access	H	L	0	L	H	odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	status out
Other task file access	H	L	1-7H	L	H	High-Z	data

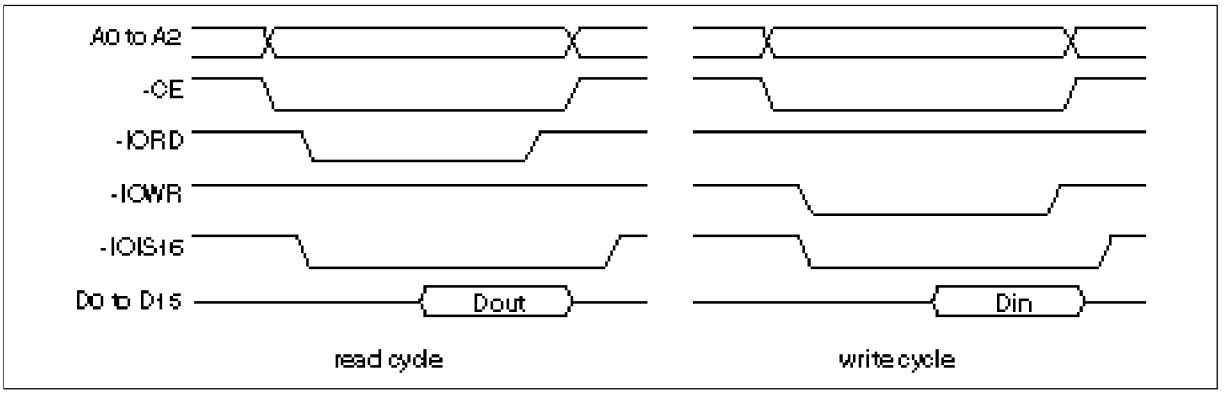
Note: ×: L or H

True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	×	×	×	don't care	don't care
Standby mode	H	H	×	×	×	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control in
Other task file access	H	L	1-7H	H	L	don't care	data

Note: ×: L or H

True IDE Mode I/O Access Timing Example



Configuration register specifications

This card supports four Configuration registers for the purpose of the configuration and observation of this card. These registers can be used in memory card mode and I/O card mode. In True IDE mode, these registers can not be used.

1. Configuration Option register (Address 200H)

This register is used for the configuration of the card configuration status and for the issuing soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevlREQ	INDEX					

Note: initial value: 00H

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to "1", places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to "0", places the card in the reset state of Hard Reset (This bit is set to "0" by Hard Reset) . Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevlREQ (HOST->)	R/W	This bit sets to "0" when pulse mode interrupt is selected, and "1" when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bits is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is "000000" for the purpose of Memory card interface recognition.

INDEX bit assignment

INDEX bit								
5	4	3	2	1	0	Card mode	Task File register address	Mapping mode
0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	memory mapped
0	0	0	0	0	1	I/O card	xx0H to xxFH	contiguous I/O mapped
0	0	0	0	1	0	I/O card	1F0H to 1F7H, 3F6H to 3F7H	primary I/O mapped
0	0	0	0	1	1	I/O card	170H to 177H, 376H to 377H	secondary I/O mapped

2. Configuration and Status register (Address 202H)

This register is used for observing the card state.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

Note: initial value: 00H

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that CRDY/-BSY bit on Pin Replacement register is set to "1". When CHGED bit is set to "1", -STSCHG pin is held "L" at the condition of SIGCHG bit set to "1" and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to "1", -STSCHG pin is controlled by CHGED bit. If this bit is set to "0", -STSCHG pin is kept "H".
IOIS8 (HOST->)	R/W	The host sets this field to "1" when it can provide I/O cycles only with on 8 bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to "1", the card enters sleep state (Power Down mode). When this bit is reset to "0", the card transfers to idle state (active mode). RRDY/-BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command.
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero.

3. Pin Replacement register (Address 204H)

This register is used for providing the signal state of -IREQ signal when the card configured I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0

Note: initial value: 0CH

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to "1" when the RRDY/-BSY bit changes state. This bit may also be written by the host.
RRDY/-BSY (HOST->)	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-BSY bit masking.

4. Socket and Copy register (Address 206H)

This register is used for identification of the card from the other cards. Host can read and write this register. This register should be set by host before this card's Configuration Option register set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0

Note: initial value: 00H

Name	R/W	Function
DRV# (HOST->)	R/W	This fields are used for the configuration of the plural cards. When host configures the plural cards, written the card's copy number in this field. In this way, host can perform the card's master/slave organization.

CIS informations

After the assembled Flash card, CIS information should be programmed into the Flash. For example, CIS information of HITACHI's Flash card is defined as follows.

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
000H	01H	CISTPL_DEVICE								Device info tuple	Tuple code
002H	04H	TPL_LINK								Link length is 4 byte	Link to next tuple
004H	DFH	Device type				WPS	Device speed			Device type = DH: I/O device WPS = 1: No WP Device speed = 7: ext speed	Device type, WPS, speed
006H	4AH	EXT	Speed mantissa				Speed exponent			400 ns if no wait	Extended speed
008H	01H	1x					2k units			2k byte of address space	Device size
00AH	FFH	List end marker								End of device	END marker
00CH	1CH	CISTPL_DEVICE_OC								Other conditions device info tuple	Tuple code
00EH	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
010H	02H	EXT	Reserved			V_{CC}			MWAIT	3 V, wait is not used	Other conditions info field
012H	D9H	Device type				WPS	Device speed			Device type = DH: I/O device WPS = 1: No WP Device speed = 1: 250 ns	Device type, WPS, speed
014H	01H	1x					2k units			2k byte of address space	Device size
016H	FFH	List end marker								End of device	END marker
018H	18H	CISTPL_JEDEC_C								JEDEC ID common memory	Tuple code
01AH	02H	TPL_LINK								Link length is 2 bytes	Link to next tuple
01CH	DFH	PCMCIA's manufacturer's JEDEC ID code								Manufacturer's ID code	JEDEC ID of PC Card ATA
01EH	01H	PCMCIA JEDEC device code								2nd byte of JEDEC ID	
020H	20H	CISTPL_MANFID								Manufacturer's ID code	Tuple code
022H	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
024H	07H	Low byte of PCMCIA manufacturer's code								HITACHI JEDEC manufacturer's ID	Low byte of manufacturer's ID code
026H	00H	High byte of PCMCIA manufacturer's code								Code of 0 because other byte is JEDEC 1 byte manufacture's ID	High byte of manufacturer's ID code
028H	00H	Low byte of product code								HITACHI code for PC CARD ATA	Low byte of product code
02AH	00H	High byte of product code									High byte of product code

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
02CH	15H	CISTPL_VERS_1	Level 1 version/product info	Tuple code
02EH	15H	TPL_LINK	Link length is 15h bytes	Link to next tuple
030H	04H	TPPLV1_MAJOR	PCMCIA2.0/JEIDA4.1	Major version
032H	01H	TPPLV1_MINOR	PCMCIA2.0/JEIDA4.1	Minor version
034H	48H		‘ H ’	Info string 1
036H	49H		‘ I ’	
038H	54H		‘ T ’	
03AH	41H		‘ A ’	
03CH	43H		‘ C ’	
03EH	48H		‘ H ’	
040H	49H		‘ I ’	
042H	00H		Null terminator	
044H	46H		‘ F ’	Info string 2
046H	4CH		‘ L ’	
048H	41H		‘ A ’	
04AH	53H		‘ S ’	
04CH	48H		‘ H ’	
04EH	00H		Null terminator	
050H	35H		‘ 5 ’	Vender specific strings
052H	2EH		‘ . ’	
054H	30H		‘ 0 ’	
056H	00H		Null terminator	
058H	FFH	List end marker	End of device	END marker
05AH	21H	CISTPL_FUNCID	Function ID tuple	Tuple code
05CH	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
05EH	04H	TPLFID_FUNCTION = 04H	Disk function, may be silicon, may be removable	PC card function code
060H	01H	Reserved R P	R = 0: No BIOS ROM P = 1: Configure card at power on	System initialization byte

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
062H	22H	CISTPL_FUNCE	Function extension tuple	Tuple code
064H	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
066H	01H	Disk function extension tuple type	Disk interface type	Extension tuple type for disk
068H	01H	Disk interface type	PC card ATA interface	Interface type
06AH	22H	CISTPL_FUNCE	Function extension tuple	Tuple code
06CH	03H	TPL_LINK	Link length is 3 bytes	Link to next tuple
06EH	02H	Disk function extension tuple type	Single drive	Extension tuple type for disk
070H	0CH	Reserved D U S V	No V_{PP}, silicon, single drive V = 0: No V_{PP} required S = 1: Silicon U = 1: Unique serial # D = 0: Single drive on card	Basic ATA option parameters byte 1
072H	0FH	R I E N P3 P2 P1 P0	P0: Sleep mode supported P1: Standby mode supported P2: Idle mode suppported P3: Drive auto power control N: Some config excludes 3X7 E: Index bit is emulated I: Twin IOIS16# data reg only R: Reserved	Basic ATA option parameters byte 2
074H	1AH	CISTPL_CONFIG	Configuration tuple	Tuple code
076H	05H	TPL_LINK	Link length is 5 bytes	Link to next tuple
078H	01H	RFS RMS RAS	RFS: Reserved RMS: TPCC_RMSK size - 1 = 0 RAS: TPCC_RADR size - 1 = 1 1 byte register mask 2 byte config base address	Size of fields byte TPCC_SZ
07AH	03H	TPCC_LAST	Entry with config index of 03H is final entry in table	Last entry of config registers
07CH	00H	TPCC_RADR (LSB)	Configuration registers are located at 200H in REG space	Location of config registers
07EH	02H	TPCC_RADR (MSB)		
080H	0FH	Reserved S P C I	I: Configuration index C: Configuration and status P: Pin replacement S: Socket and copy	Configuration registers present mask TPCC_RMSK

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
082H	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
084H	08H	TPL_LINK								Link length is 8 bytes	Link to next tuple
086H	C0H	I	D	Configuration index						Memory mapped I/O configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
088H	40H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP used B = 0: BVD1 and BVD2 not used IF type = 0: Memory interface	Interface description field TPCE_IF
08AH	A1H	M	MS		IR	IO	T	P		M = 1: Misc info present MS = 01: Memory space info single 2-byte length IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
08CH	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
08EH	55H	X	Mantissa			Exponent				Nominal voltage = 5 V	V_{CC} nominal value
090H	08H	Length in 256 bytes pages (LSB)								Length of memory space is 2 kB	Memory space description structures (TPCE_MS)
092H	00H	Length in 256 bytes pages (MSB)									
094H	20H	X	R	P	R O	A	T			X = 0: No more misc fields R: Reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
096H	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
098H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
09AH	00H	I	D	Configuration index						Memory mapped I/O configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
09CH	01H	M	MS		IR	IO	T		P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
09EH	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0A0H	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0A2H	1EH	X	Extension							+0.3 V	Extension byte
0A4H	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0A6H	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
0A8H	0AH	TPL_LINK								Link length is 10 bytes	Link to next tuple
0AAH	C1H	I	D	Configuration INDEX						Contiguous I/O mapped ATA registers configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 1	Configuration table index byte TPCE_INDX
0ACH	41H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
0AEH	99H	M	MS		IR	IO	T	P		M = 1: Misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 1: I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0B0H	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0B2H	55H	X	Mantissa				Exponent			Nominal voltage = 5 V	V_{CC} nominal value
0B4H	64H	R	S	E	IO AddrLine					S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLine: 4 lines decoded	I/O space description field TPCE_IO
0B6H	F0H	S	P	L	M	V	B	I	N	S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 1: Bit mask of IRQs present V = 0: No vender unique IRQ B = 0: No bus error IRQ I = 0: No IO check IRQ N = 0: No NMI	Interrupt request description structure TPCE_IR

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0B8H	FFH	IRQ 7	IRQ 6	IRQ 5	IRQ 4	IRQ 3	IRQ 2	IRQ 1	IRQ0	IRQ level to be routed 0 to 15 recommended	Mask extension byte 1 TPCE_IR
0BAH	FFH	IRQ 15	IRQ 14	IRQ 13	IRQ 12	IRQ 11	IRQ 10	IRQ 9	IRQ8	Recommended routing to any “normal, maskable” IRQ.	Maskextension byte 2 TPCE_IR
0BCH	20H	X	R	P	RO	A	T			X = 0: Nomore misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0BEH	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
0C0H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
0C2H	01H	I	D	Configuration index						Contiguous I/O mapped ATA registers configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 1	Configuration table index byte TPCE_INDX
0C4H	01H	M	MS			IR	IO	T	P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0C6H	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0C8H	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0CAH	1EH	X	Extension							+0.3 V	Extension byte
0CCH	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0CEH	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
0D0H	0FH	TPL_LINK								Link length is 15 bytes	Link to next tuple
0D2H	C2H	I	D	Configuration INDEX						ATA primary I/O mapped configuration I = 1: Interface byte follows D = 1: default entry follows Configuration index = 2	Configuration table index byte TPCE_INDX
0D4H	41H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
0D6H	99H	M	MS		IR	IO	T	P		M = 1: misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 1: I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0D8H	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0DAH	55H	X	Mantissa			Exponent				Nominal voltage = 5 V	V_{CC} nominal value
0DCH	EAH	R	S	E	IO AddrLine					R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
0DEH	61H	LS		AS		N range				LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 bytes N Range = 1: Address range - 1	I/O range format description

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0E0H	F0H									1st I/O base address (LSB)	1st I/O range address
0E2H	01H									1st I/O base address (MSB)	
0E4H	07H									1st I/O length - 1	1st I/O range length
0E6H	F6H									2nd I/O base address (LSB)	2nd I/O range address
0E8H	03H									2nd I/O base address (MSB)	
0EAH	01H									2nd I/O length - 1	2nd I/O range length
0ECH	EEH	S	P	L	M	IRQ level				S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level is IRQ14	Interrupt request description structure TPCE_IR
0EEH	20H	X	R	P	RO	A	T			X = 0: Nomore misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0F0H	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
0F2H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
0F4H	02H	I	D	Configuration index						ATA primary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 2	Configuration table index byte TPCE_INDX
0F6H	01H	M	MS			IR	IO	T	P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0F8H	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0FAH	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0FCH	1EH	X	Extension							+0.3 V	Extension byte
0FEH	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
100H	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
102H	0FH	TPL_LINK								Link length is 15 bytes	Link to next tuple
104H	C3H	I	D	Configuration INDEX						ATA secondary I/O mapped configuration I = 1: Interface byte follows D = 1: default entry Configuration index = 3	Configuration table index byte TPCE_INDX
106H	41H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
108H	99H	M	MS		IR	IO	T	P		M = 1: misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 1: I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
10AH	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
10CH	55H	X	Mantissa				Exponent			Nominal voltage = 5 V	V_{CC} nominal value
10EH	EAH	R	S	E	IO AddrLine					R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
110H	61H	LS		AS		N range				LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 bytes N Range = 1: Address range - 1	I/O range format description

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
112H	70H									1st I/O base address (LSB)	1st I/O range address
114H	01H									1st I/O base address (MSB)	
116H	07H									1st I/O length - 1	1st I/O range length
118H	76H									2nd I/O base address (LSB)	2nd I/O range address
11AH	03H									2nd I/O base address (MSB)	
11CH	01H									2nd I/O length - 1	2nd I/O range length
11EH	EEH	S	P	L	M	IRQ level				S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level is IRQ14	Interrupt request description structure TPCE_IR
120H	20H	X	R	P	RO	A	T			X = 0: Nomore misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
122H	1BH	CISTPL_CFTABLE_ENTRY								Configuration table entry tuple	Tuple code
124H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
126H	03H	I	D	Configuration index						ATA secondary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 3	Configuration table index byte TPCE_INDX
128H	01H	M	MS			IR	IO	T	P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
12AH	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
12CH	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
12EH	1EH	X	Extension							+0.3 V	Extension byte
130H	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current
132H	14H	CISTPL_NO_LINK								No link control tuple	Tuple code
134H	00H									Link is 0 bytes	Link to next tuple
136H	FFH	CISTPL_END								End of list tuple	Tuple code

Task File register specification

These registers are used for reading and writing the storage data in this card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addresses are shown as follows.

Memory map (INDEX = 0)

-REG	A10	A9 to A4	A3	A2	A1	A0	Offset	-OE = L	-WE = L
1	0	×	0	0	0	0	0H	Data register	Data register
1	0	×	0	0	0	1	1H	Error register	Feature register
1	0	×	0	0	1	0	2H	Sector count register	Sector count register
1	0	×	0	0	1	1	3H	Sector number register	Sector number register
1	0	×	0	1	0	0	4H	Cylinder low register	Cylinder low register
1	0	×	0	1	0	1	5H	Cylinder high register	Cylinder high register
1	0	×	0	1	1	0	6H	Drive head register	Drive head register
1	0	×	0	1	1	1	7H	Status register	Command register
1	0	×	1	0	0	0	8H	Dup. even data register	Dup. even data register
1	0	×	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
1	0	×	1	1	0	1	DH	Dup. error register	Dup. feature register
1	0	×	1	1	1	0	EH	Alt. status register	Device control register
1	0	×	1	1	1	1	FH	Drive address register	Reserved
1	1	×	×	×	×	0	8H	Even data register	Even data register
1	1	×	×	×	×	1	9H	Odd data register	Odd data register

Contiguous I/O map (INDEX = 1)

-REG	A10 to A4	A3	A2	A1	A0	Offset	-IORD = L	-IOWR = L
0	×	0	0	0	0	0H	Data register	Data register
0	×	0	0	0	1	1H	Error register	Feature register
0	×	0	0	1	0	2H	Sector count register	Sector count register
0	×	0	0	1	1	3H	Sector number register	Sector number register
0	×	0	1	0	0	4H	Cylinder low register	Cylinder low register
0	×	0	1	0	1	5H	Cylinder high register	Cylinder high register
0	×	0	1	1	0	6H	Drive head register	Drive head register
0	×	0	1	1	1	7H	Status register	Command register
0	×	1	0	0	0	8H	Dup. even data register	Dup. even data register
0	×	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
0	×	1	1	0	1	DH	Dup. error register	Dup. feature register
0	×	1	1	1	0	EH	Alt. status register	Device control register
0	×	1	1	1	1	FH	Drive address register	Reserved

Primary I/O map (INDEX = 2)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD = L	-IOWR = L
0	×	1FH	0	0	0	0	Data register	Data register
0	×	1FH	0	0	0	1	Error register	Feature register
0	×	1FH	0	0	1	0	Sector count register	Sector count register
0	×	1FH	0	0	1	1	Sector number register	Sector number register
0	×	1FH	0	1	0	0	Cylinder low register	Cylinder low register
0	×	1FH	0	1	0	1	Cylinder high register	Cylinder high register
0	×	1FH	0	1	1	0	Drive head register	Drive head register
0	×	1FH	0	1	1	1	Status register	Command register
0	×	3FH	0	1	1	0	Alt. status register	Device control register
0	×	3FH	0	1	1	1	Drive address register	Reserved

Secondary I/O map (INDEX = 3)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD = L	-IOWR = L
0	×	17H	0	0	0	0	Data register	Data register
0	×	17H	0	0	0	1	Error register	Feature register
0	×	17H	0	0	1	0	Sector count register	Sector count register
0	×	17H	0	0	1	1	Sector number register	Sector number register
0	×	17H	0	1	0	0	Cylinder low register	Cylinder low register
0	×	17H	0	1	0	1	Cylinder high register	Cylinder high register
0	×	17H	0	1	1	0	Drive head register	Drive head register
0	×	17H	0	1	1	1	Status register	Command register
0	×	37H	0	1	1	0	Alt. status register	Device control register
0	×	37H	0	1	1	1	Drive address register	Reserved

True IDE Mode I/O map

-CE2	-CE1	A2	A1	A0	-IORD = L	-IOWR = L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

1. Data register: This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

2. Error register: This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0" (Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	"0"	IDNF	"0"	ABRT	"0"	AMNF

bit	Name	Function
7	BBK (Bad BlocK detected)	This bit is set when a Bad Block is detected in requested ID field.
6	UNC (Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF (ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (ABoRTed command)	This bit is set if the command has been aborted because of the card status condition. (Not ready, Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

3. Feature register: This register is write only register, and provides information regarding features of the drive which the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

4. Sector count register: This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request. This register's initial value is "01H".

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5. Sector number register: This register contains the starting sector number which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

6. Cylinder low register: This register contains the low 8-bit of the starting cylinder address which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

7. Cylinder high register: This register contains the high 8-bit of the starting cylinder address which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

8. Drive head register: This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	LBA	1	DRV	Head number			

bit	Name	Function
7	1	This bit is set to "1".
6	LBA	LBA is a flag to select either Cylinder / Head / Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00 : Sector Number Register D7-D0. LBA15-LBA08 : Cylinder Low Register D7-D0. LBA23-LBA16 : Cylinder High Register D7-D0. LBA27-LBA24 : Drive / Head Register bits HS3-HS0.
5	1	This bit is set to "1".
4	DRV (DRiVe select)	This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3 to 0	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

9. Status register: This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX = 1, 2, 3) and level interrupt mode, -IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF (Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seek complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to "0".
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register or Error register. This bit is cleared by the next command.

10. Alternate status register: This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that -IREQ is not negated when data read.

11. Command register: This register is write only register, and it is used for writing the command at executing the drive operation. The command code written in the command register, after the parameter is written in the Task File during the card is Ready state.

Command	Command code	Used parameter						
		FR	SC	SN	CY	DR	HD	LBA
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

Note: FR: Feature register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder register
DR: DRV bit of Drive Head register
HD: Head Number of Drive Head register
LBA: Logical Block Address Mode Supported
Y: The register contains a valid parameter for this command.
N: The register does not contain a valid parameter for this command.

12. Device control register: This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
×	×	×	×	1	SRST	nIEN	0

bit	Name	Function
7 to 4	×	don't care
3	1	This bit is set to "1".
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN (Interrupt ENable)	This bit is used for enabling -IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.
0	0	This bit is set to "0".

13. Drive Address register: This register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
×	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

bit	Name	Function
7	×	This bit is unknown
6	nWTG (WriTing Gate)	This bit is unknown
5 to 2	nHS3-0 (Head Select3-0)	These bits is the negative value of Head Select bits (bit 3 to 0) in Drive/Head register.
1	nDS1 (Idrive Select1)	This bit is unknown
0	nDS0 (Idrive Select0)	This bit is unknown

ATA Command specifications

This table summarizes the ATA command set with the paragraphs. Following shows the support commands and command codes which are written in command registers.

ATA Command Set

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5H or 98H	—	—	—	—	Y	—	—
2	Execute drive diagnostic	90H	—	—	—	—	Y	—	—
3	Erase sector(s)	C0H	—	Y	Y	Y	Y	Y	Y
4	Format track	50H	—	Y	—	Y	Y	Y	Y
5	Identify Drive	ECH	—	—	—	—	Y	—	—
6	Idle	E3H or 97H	—	Y	—	—	Y	—	—
7	Idle immediate	E1H or 95H	—	—	—	—	Y	—	—
8	Initialize drive parameters	91H	—	Y	—	—	Y	Y	—
9	Read buffer	E4H	—	—	—	—	Y	—	—
10	Read multiple	C4H	—	Y	Y	Y	Y	Y	Y
11	Read long sector	22H, 23H	—	—	Y	Y	Y	Y	Y
12	Read sector (s)	20H, 21H	—	Y	Y	Y	Y	Y	Y
13	Read verify sector (s)	40H, 41H	—	Y	Y	Y	Y	Y	Y
14	Recalibrate	1XH	—	—	—	—	Y	—	—
15	Request sense	03H	—	—	—	—	Y	—	—
16	Seek	7XH	—	—	Y	Y	Y	Y	Y
17	Set features	EFH	Y	—	—	—	Y	—	—
18	Set multiple mode	C6H	—	Y	—	—	Y	—	—
19	Set sleep mode	E6H or 99H	—	—	—	—	Y	—	—
20	Stand by	E2H or 96H	—	—	—	—	Y	—	—
21	Stand by immediate	E0H or 94H	—	—	—	—	Y	—	—
22	Translate sector	87H	—	Y	Y	Y	Y	Y	Y
23	Wear level	F5H	—	—	—	—	Y	Y	—
24	Write buffer	E8H	—	—	—	—	Y	—	—
25	Write long sector	32H or 33H	—	—	Y	Y	Y	Y	Y
26	Write multiple	C5H	—	Y	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	—	Y	Y	Y	Y	Y	Y
28	Write sector	30H or 31H	—	Y	Y	Y	Y	Y	Y
29	Write sector(s) w/o erase	38H	—	Y	Y	Y	Y	Y	Y
30	Write verify	3CH	—	Y	Y	Y	Y	Y	Y

Note: FR: Feature Register
SC: Sector Count register (00H to FFH)
SN: Sector Number register (01H to 20H)
CY: Cylinder Low/High register (to)
DR: Drive bit of Drive/Head register
HD: Head No.(0 to 3) of Drive/Head register
NH: No. of Heads
Y: Set up
—: Not set up

1. Check Power Mode (code: E5H or 98H): This command checks the power mode.

2. Execute Drive Diagnostic (code: 90H): This command performs the internal diagnostic tests implemented by the Card.

3. Erase Sector(s) (code: C0H): This command is used to erase data sectors.

4. Format Track (code: 50H): This command writes the desired head and cylinder of the selected drive. But selected sector data is not exchange. This card excepts a sector buffer of data from the host to follow the command with same protocol as the Write Sector Command.

5. Identify Drive (code: ECH): This command enables the host to receive parameter information from the Card.

Identify Drive Information

Word address	Default value	Total bytes	Data field type information
0	848AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	XXXX	2	Number of unformatted bytes per sector
6	XXXX	2	Default number of sectors per track
7 to 8	XXXX	4	Number of sectors per card (Word7 = MSW, Word8 = LSW)
9	0000H	2	Reserved
10 to 19	XXXX	20	Reserved
20	0002H	2	Buffer type (dual ported)
21	0002H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23 to 46	XXXX	48	Firmware revision in ASCII etc.
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT Supported (bit 8), LBA supported (bit9)
50	0000H	2	Reserved
51	0100H	2	PIO data transfer cycle timing mode 1
52	0000H	2	DMA data transfer cycle timing mode not Supported
53 to 58	XXXX	12	Reserved
59	010XH	2	Multiple sector setting is valid
60 to 61	XXXX	4	Total number of sectors addressable in LBA Mode
62 to 255	0000H	388	Reserved

6. Idle (code: E3H or 97H): This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

7. Idle Immediate (code: E1H or 95H): This command causes the Card to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

8. Initialize Drive Parameters (code: 91H): This command enables the host to set the number of sectors per track and the number of heads per cylinder.

9. Read Buffer (code: E4H): This command enables the host to read the current contents of the card's sector buffer.

10. Read Multiple (code: C4H): This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

11. Read Long Sector (code: 22H or 23H): This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.

12. Read Sector(s) (code: 20H, 21H): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

13. Read Verify Sector(s) (code: 40H or 41H): This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host .

14. Recalibrate (code: 1XH): This command is effectively a NOP command to the Card and is provided for compatibility purposes.

15. Request Sense (code: 03H): This command requests an extended error code after command ends with an error.

16. Seek (code: 7XH): This command is effectively a NOP command to the Card although it does perform a range check.

17. Set Features (code: EFH): This command is used by the host to establish or select certain features.

Feature	Operation
01H	Enable 8-bit data transfers.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
81H	Disable 8-bit data transfers.
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

18. Set Multiple Mode (code: C6H): This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands.

19. Set Sleep Mode (code: E6H or 99H): This command causes the Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

20. Stand By (code: E2H or 96H): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

21. Stand By Immediate (code: E0H or 94H): This command causes the Card to set BSY, enter the Sleep mode(which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

22. Translate Sector (code: 87H): This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This controller has no counter, so this controller always responds with "00H".

23. Wear Level (code: F5H): This command effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00H indicating Wear Level is not needed.

24. Write Buffer (code: E8H): This command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired.

25. Write Long Sector (code: 32H or 33H): This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

26. Write Multiple (code: C5H): This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

27. Write Multiple without Erase (code: CDH): This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.

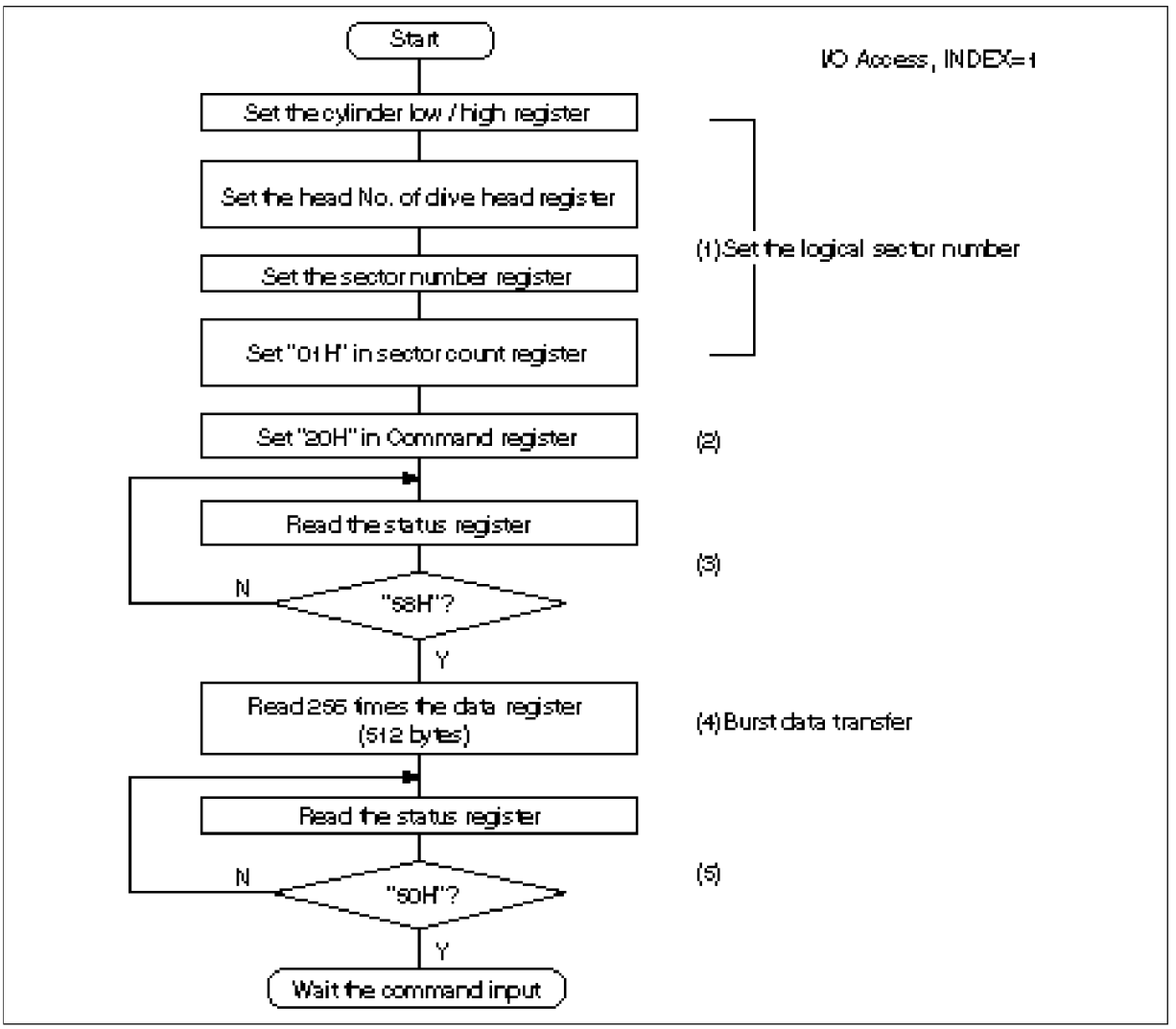
28. Write Sector(s) (code: 30H or 31H): This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

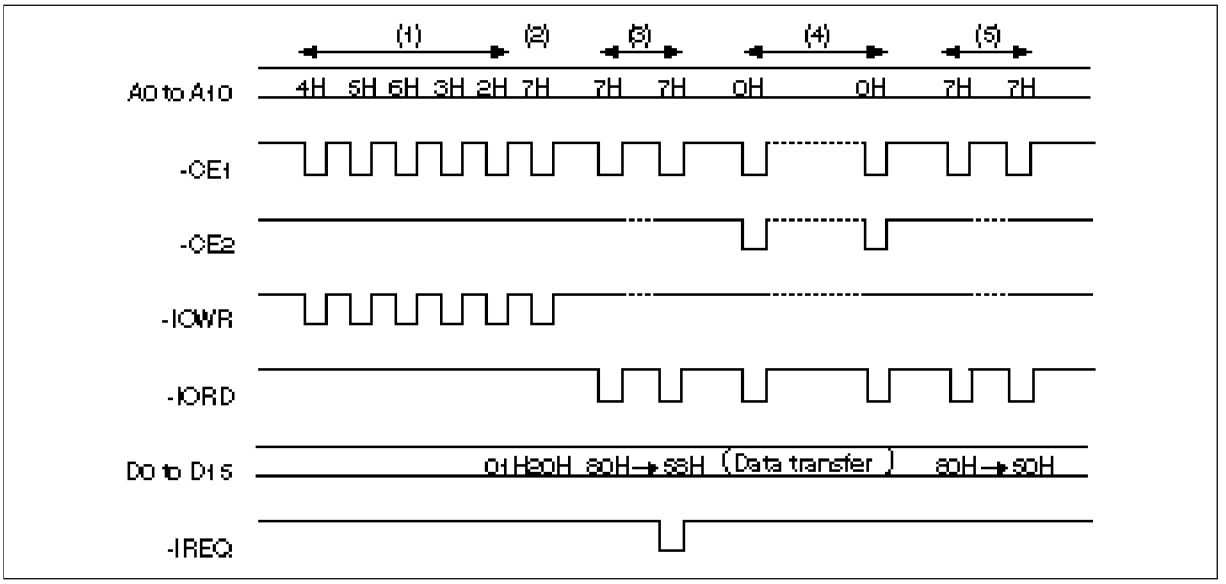
29. Write Sector(s) without Erase (code: 38H): This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.

30. Write Verify (code: 3CH): This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

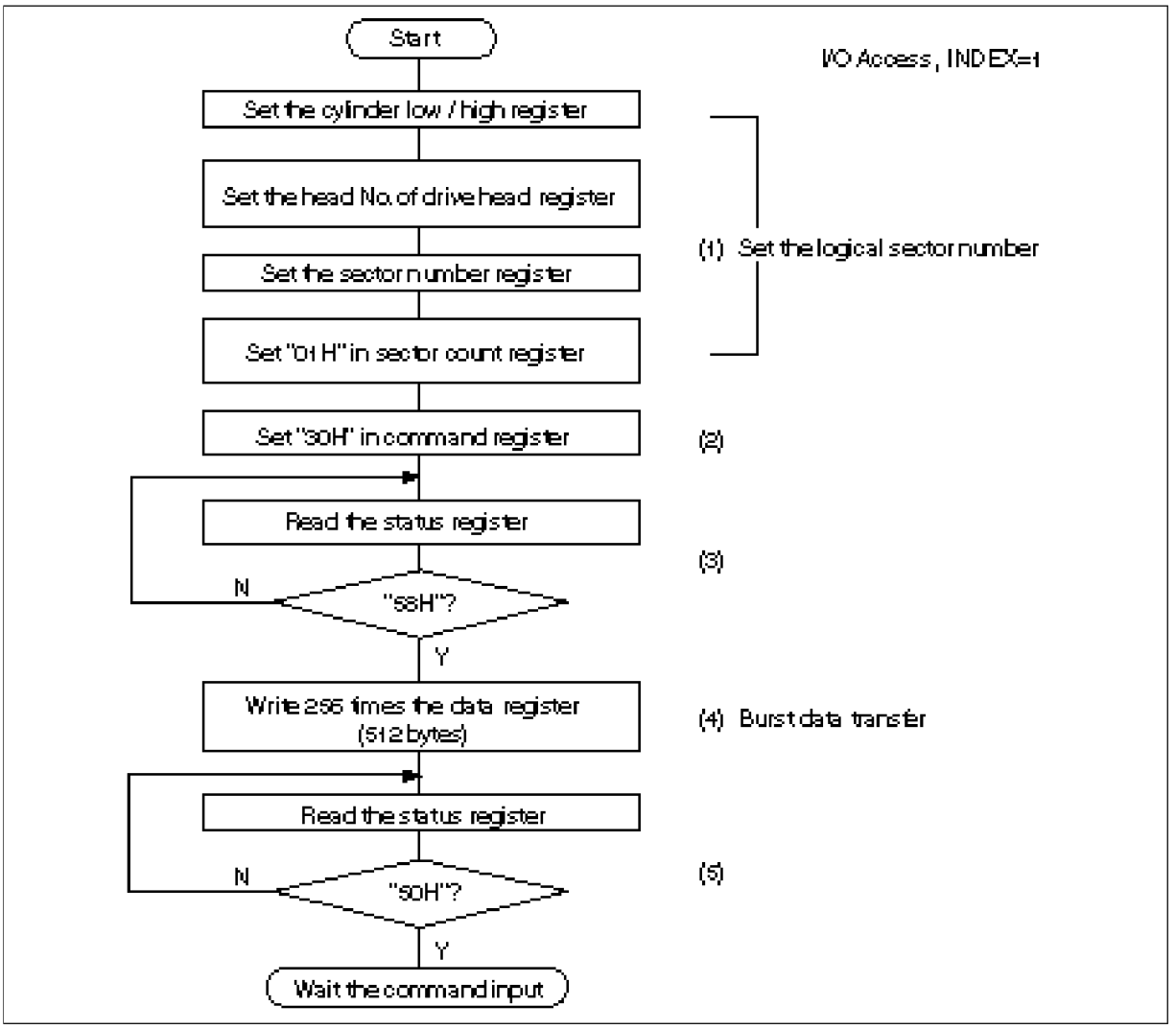
Sector Transfer Protocol

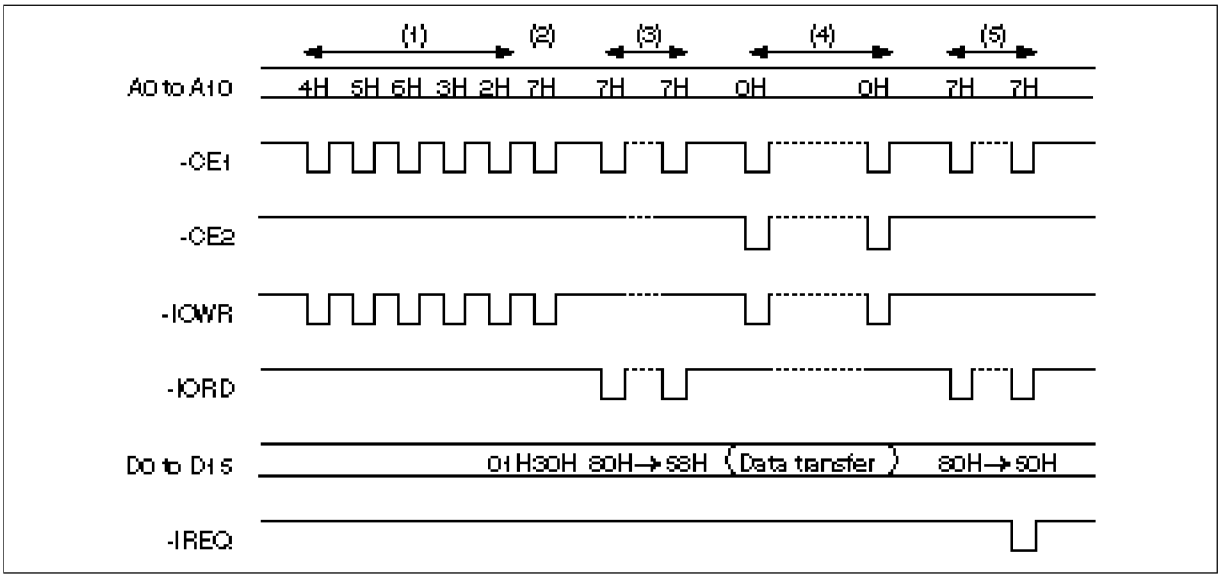
1. Sector read: 1 sector read procedure after the card configured I/O interface is shown as follows.




(1)
(2)
(3)
(4)
(5)
A0 to A10
4H 5H 6H 3H 2H 7H 7H 7H 0H 0H 7H 7H
-CE1
-CE2
-IOWR
-IORD
D0 to D15
01H→20H 80H→88H (Data transfer) 80H→80H
-IREQ

2. Sector write: 1 sector write procedure after the card configured I/O interface is shown as follows.




(1)
(2)
(3)
(4)
(5)
A0 to A10
4H 5H 6H 3H 2H 7H 7H 7H 0H 0H 7H 7H
-CE1
-CE2
-IOWR
-IORD
D0 to D15
01H 30H 80H→88H 〈Data transfer〉 80H→50H
-IREQ

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
All input/output voltages	Vin, Vout	–0.3 to V_{CC} + 0.3	V	1, 2
	Vin, Vout	–0.3 to V_{DD} + 0.3	V	1, 3
V_{CC}, V_{DD} voltage	V_{CC}, V_{DD}	–0.3 to +6.7	V	
Operating temperature range	Topr	–40 to +85	C	
Storage temperature range	Tstg	–55 to +125	C	

Notes: 1. Vin, Vout min = –2.0 V for pulse width 20 ns.
2. PT5xxxx, PV5xx: 5 V.
3. PC3xxxx, PV3x: 3.3 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature	Ta	0	25	70	C
V_{CC}, V_{DD} voltage	V_{CC}	4.5	5.0	5.5	V
	V_{CC}, V_{DD}	3.15	3.3	3.45	V

Capacitance (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	15	pF	Vin = 0 V	1
Output capacitance	Cout	—	—	15	pF	Vout = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

Card System performance

Item	Performance
Set up times (Reset to ready)	100 ms (max)
Set up times (Sleep to idle)	2 ms (max)
Data transfer rate to/from host	8 MB/s burst
Controller overhead (Command to DRQ)	2 ms (max)
Data transfer cycle end to ready (Sector write)	2 ms (typ)

DC Characteristics-1 (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 5%, V_{DD} = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage (CMOS level)	V_{IHC}	0.7 × V_{CC}	—	V_{CC} + 0.3	V	—
	V_{ILC}	–0.3	—	0.2 × V_{CC}	V	
Input voltage (TTL level)	V_{IHC}	2.0	—	V_{CC} + 0.3	V	—
	V_{ILC}	–0.3	—	0.6	V	
Schmitt circuit (CMOS level)*1	V_{TC+}	(1.6)	—	2.6	V	V_{CC} = 3.3 V
	V_{TC-}	0.7	—	(1.7)	V	
	V_{TC}*2	(0.3)	—	—	V	
Output voltage (CMOS) (1 mA)*3	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –0.5 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 1 mA
Output voltage (CMOS) (3 mA)*3	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –1 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
Output voltage (CMOS) (2 mA/3 mA)*3	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –2 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
Input leakage current*4	I_{LI}	—	—	1	µA	—
Output leakage current*4	I_{LO}	—	—	1	µA	V_{OUT} = high impedance
Pull-up current/(Resistivity)	$-I_{PU}$	15/(230)	80/(41)	230/(13.7)	µA/(kΩ)	V_{IN} = GND
Pull-up current/(Resistivity)*5	$-I_{PU}$	2/(1800)	16/(206)	36/(85)	µA/(kΩ)	V_{IN} = GND
Sleep/standby current*8	I_{SP1}	—	(0.2)	(0.5)	mA	CMOS level (control signal = V_{CC} – 0.2)
Sector read current*6, 8	I_{CCR}(DC)	—	(25)	(50)	mA	CMOS level (control signal = V_{CC} – 0.2)
	I_{CCR}(Peak)	—	(50)	(80)	mA	
Sector write current*7, 8	I_{CCW}(DC)	—	(25)	(50)	mA	CMOS level (control signal = V_{CC} – 0.2)
	I_{CCW}(Peak)	—	(50)	(80)	mA	

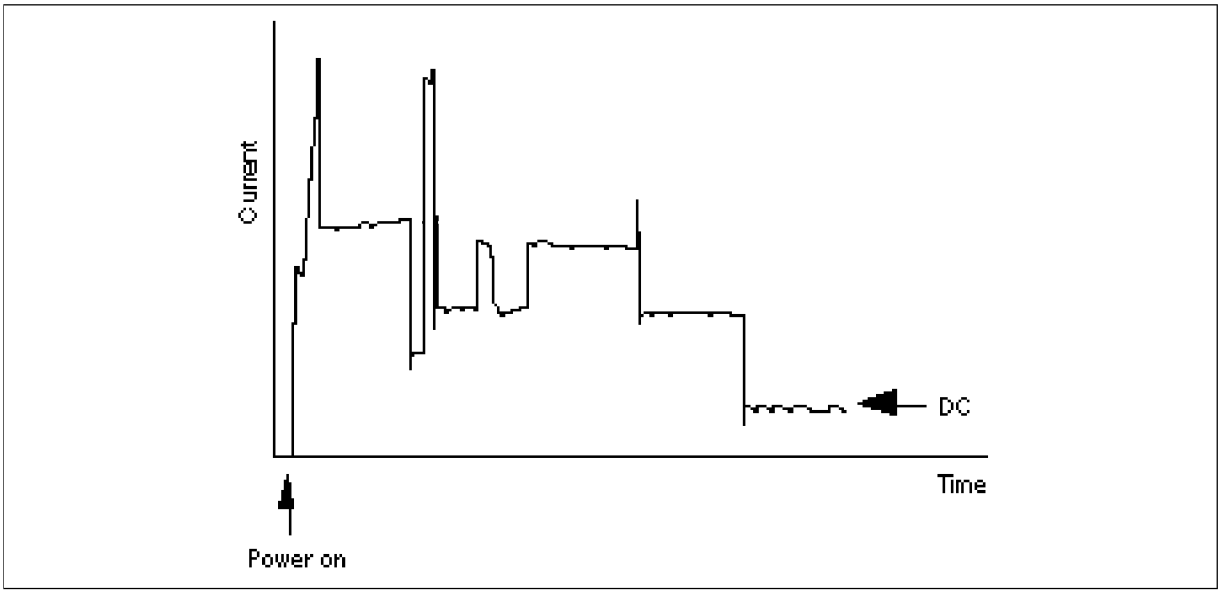
DC Characteristics-2 (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{DD} = 3.3 V ± 5%)*9

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage (CMOS level)	V_{IHC}	0.7 × V_{CC}	—	V_{CC} + 0.3	V	—
	V_{ILC}	–0.3	—	0.3 × V_{CC}	V	
Input voltage (TTL level)	V_{IHC}	2.4	—	V_{CC} + 0.3	V	—
	V_{ILC}	–0.3	—	0.6	V	
Schmitt circuit (CMOS level)*1	V_{TC+}	(2.8)	—	4.0	V	V_{CC} = 5 V
	V_{TC-}	1.1	—	(2.4)	V	
	V_{TC}*2	(0.3)	—	—	V	
Output voltage (CMOS) (3 mA)*3	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –2 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output voltage (CMOS) (2 mA/3 mA)*3	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –6 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Input leakage current*4	I_{LI}	—	—	1	µA	—
Output leakage current*4	I_{LO}	—	—	1	µA	V_{OUT} = high impedance
Pull-up current/(Resistivity)*5	$-I_{PU}$	10/(550)	45/(110)	90/(50)	µA/(kΩ)	V_{IN} = GND
Sleep/standby current*8	I_{SP1}	—	(0.5)	(1.0)	mA	CMOS level (control signal = V_{CC} – 0.2)
Sector read current*6, 8	I_{CCR}(DC)	—	(40)	(70)	mA	CMOS level (control signal = V_{CC} – 0.2)
	I_{CCR}(Peak)	—	(80)	(120)	mA	
Sector write current*7, 8	I_{CCW}(DC)	—	(45)	(75)	mA	CMOS level
	I_{CCW}(Peak)	—	(80)	(120)	mA	(control signal = V_{CC} – 0.2)

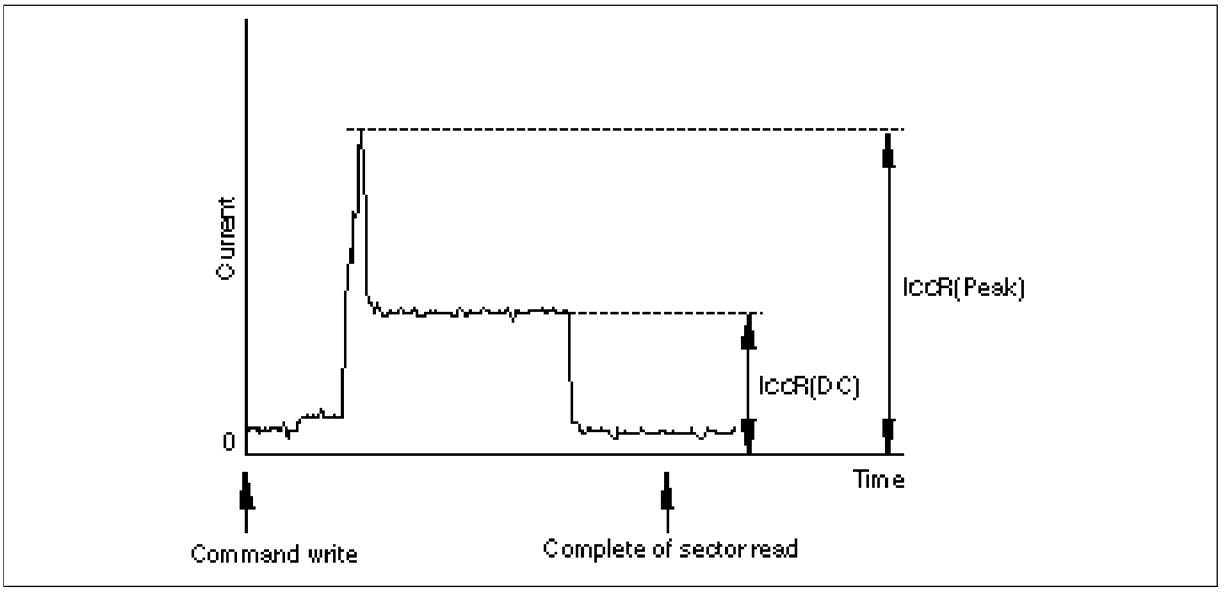
Notes : 1. CMOS schmitt input is measured at $V_{IH} = V_{TC+}$ max and $V_{IL} = V_{TC-}$ mim. ( ) is reference value.
2. V_{TC} is reference value.
3. Measured for static state.
4. Except pulled up input/output pin.
5. Pull-up resister is 100 kΩ.
6. Measured during sector read transfer.
7. Measured during sector write transfer.
8. Power dissipation is reference value on the assembled flash card, including the flash memory.
9. Except PC3O01C, PC3O03C and PC3B43UC buffer type. Refer to DC characteristics at V_{CC} = 3.3 V.

DC Current Waveform (V_{CC} = 5 V, Ta = 25 C)

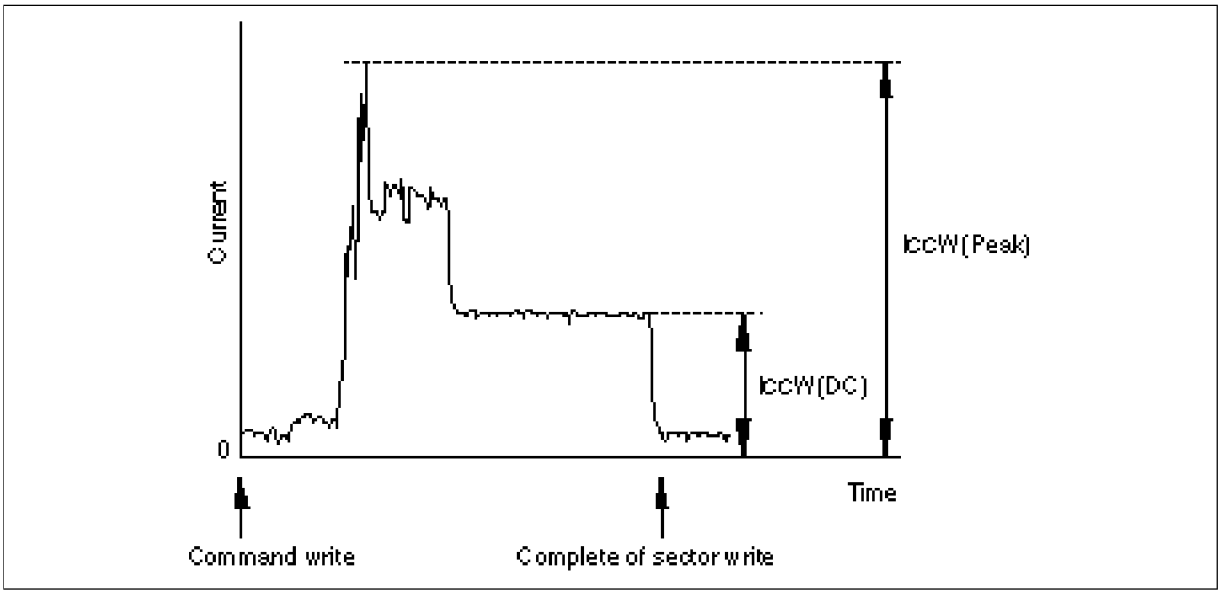
Power on Operation (Reference only)



Sector Read



Sector Write



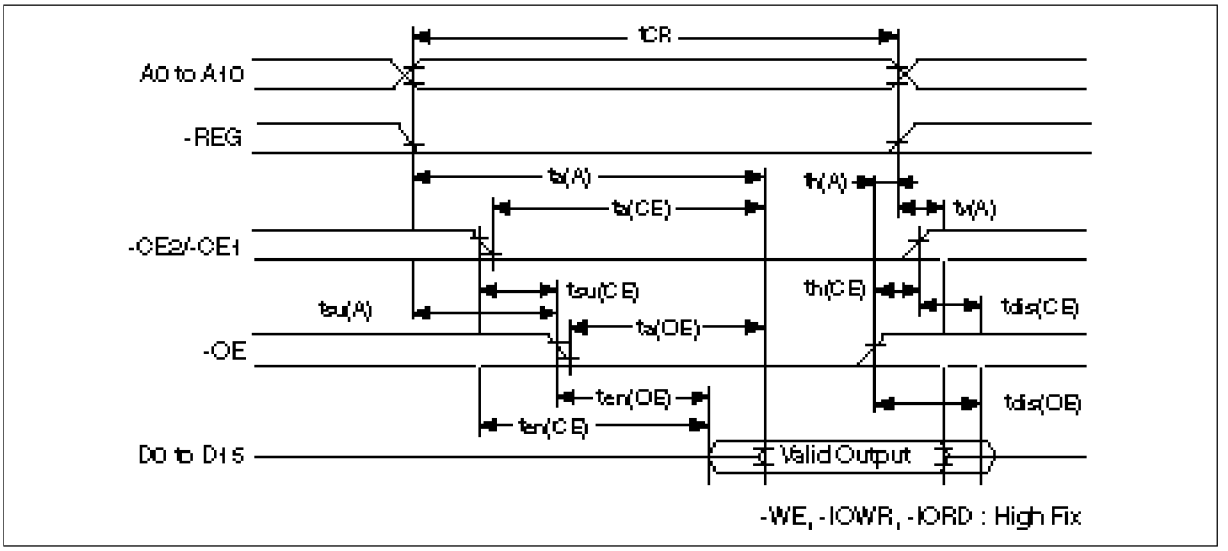
AC Characteristics

(Ta = 0 to +70 C, V_{CC} = 5 V ± 10%, V_{CC} = 3.3 V ±5%, V_{DD} = 3.3 V ± 5%)

Attribute Memory Read AC Characteristics

		250 ns			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Read cycle time	tCR	250	—	—	ns
Address access time	ta(A)	—	—	250	ns
-CE access time	ta(CE)	—	—	250	ns
-OE access time	ta(OE)	—	—	125	ns
Output disable time (-CE)	tdis(CE)	—	—	100	ns
Output disable time (-OE)	tdis(OE)	—	—	100	ns
Output enable time (-CE)	ten(CE)	5	—	—	ns
Output enable time (-OE)	ten(OE)	5	—	—	ns
Data valid time (A)	tv(A)	0	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
Address hold time	th(A)	20	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
-CE hold time	th(CE)	20	—	—	ns

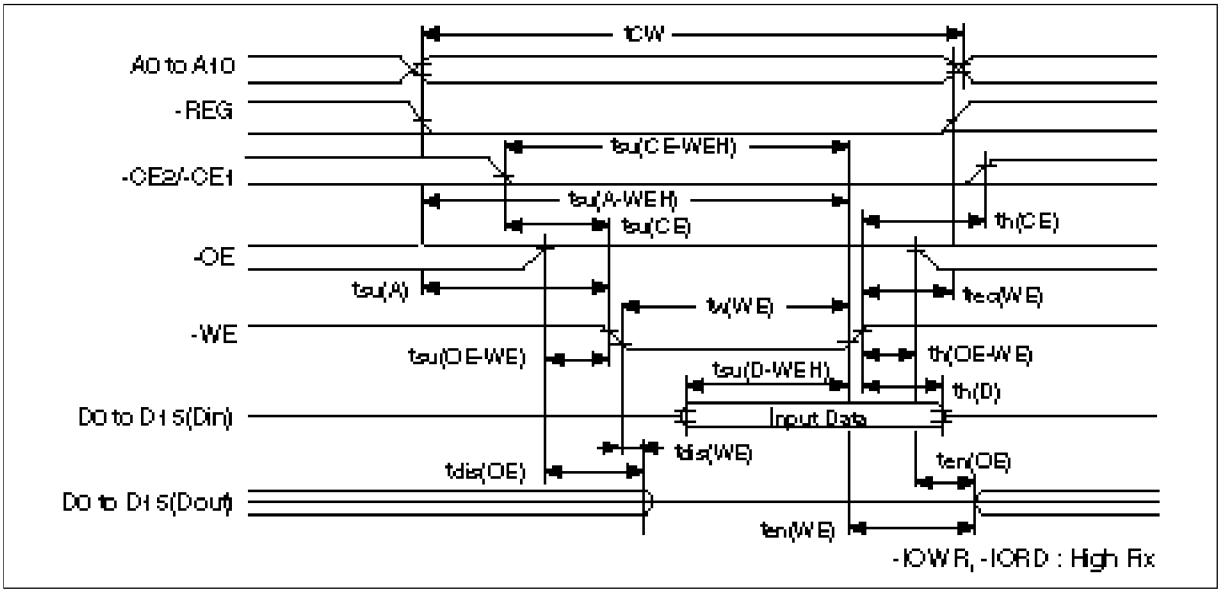
Attribute Memory Read Timing



Attribute Memory Write AC Characteristics

		250 ns			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Write cycle time	tCW	250	—	—	ns
Write pulse time	tw(WE)	150	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
Address setup time (-WE)	tsu(A-WEH)	180	—	—	ns
-CE setup time (-WE)	tsu(CE-WEH)	180	—	—	ns
Data setup time (-WE)	tsu(D-WEH)	80	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write recover time	trec(WE)	30	—	—	ns
Output disable time (-WE)	tdis(WE)	—	—	100	ns
Output disable time (-OE)	tdis(OE)	—	—	100	ns
Output enable time (-WE)	ten(WE)	5	—	—	ns
Output enable time (-OE)	ten(OE)	5	—	—	ns
Output enable setup time (-WE)	tsu(OE-WE)	10	—	—	ns
Output enable hold time (-WE)	th(OE-WE)	10	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
-CE hold time	th(CE)	20	—	—	ns

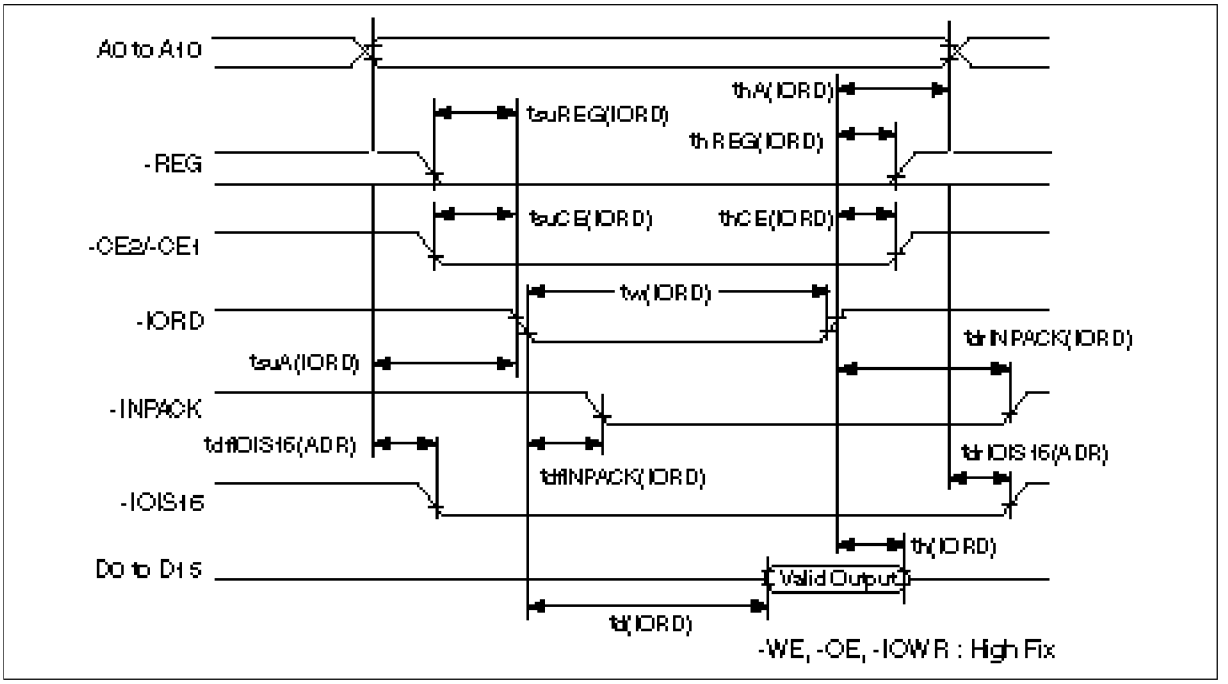
Attribute Memory Write Timing



I/O Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after -IORD	td(IORD)	—	—	100	ns
Data hold following -IORD	th(IORD)	0	—	—	ns
-IORD pulse width	tw(IORD)	165	—	—	ns
Address setup before -IORD	tsuA(IORD)	70	—	—	ns
Address hold following -IORD	thA(IORD)	20	—	—	ns
-CE setup before -IORD	tsuCE(IORD)	5	—	—	ns
-CE hold following -IORD	thCE(IORD)	20	—	—	ns
-REG setup before -IORD	tsuREG(IORD)	5	—	—	ns
-REG hold following -IORD	thREG(IORD)	0	—	—	ns
-INPACK delay falling from -IORD	tdfINPCAK(IORD)	0	—	45	ns
-INPACK delay rising from -IORD	tdrINPACK(IORD)	—	—	45	ns
-IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
-IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

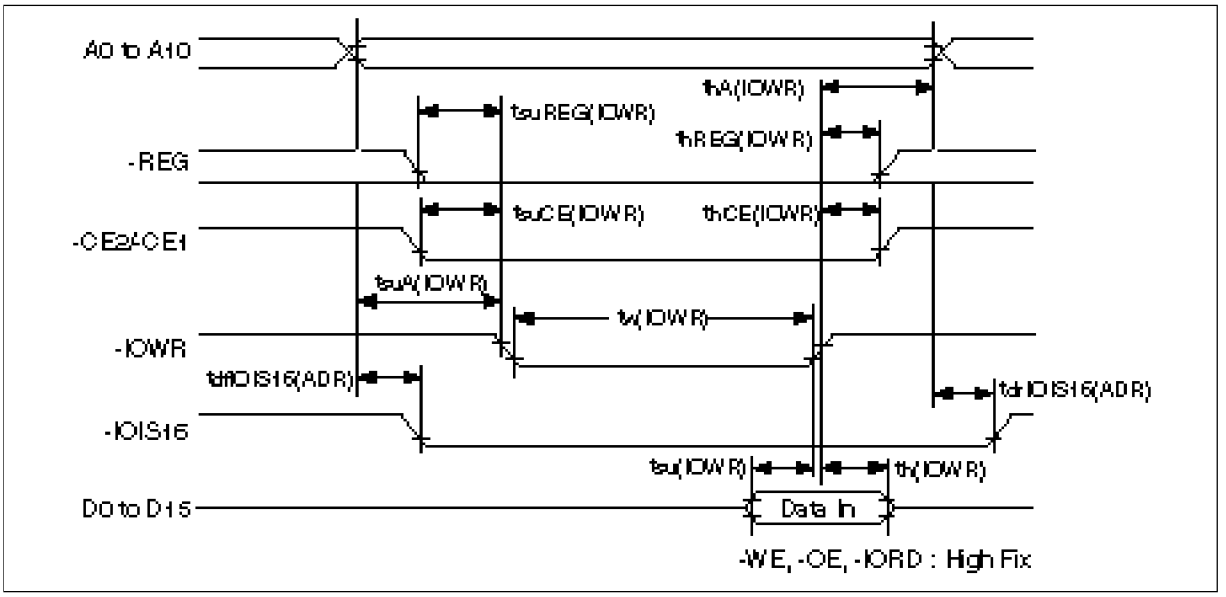
I/O Access Read Timing



I/O Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before -IOWR	tsu(IOWR)	60	—	—	ns
Data hold following -IOWR	th(IOWR)	30	—	—	ns
-IOWR pulse width	tw(IOWR)	165	—	—	ns
Address setup before -IOWR	tsuA(IOWR)	70	—	—	ns
Address hold following -IOWR	thA(IOWR)	20	—	—	ns
-CE setup before -IOWR	tsuCE(IOWR)	5	—	—	ns
-CE hold following -IOWR	thCE(IOWR)	20	—	—	ns
-REG setup before -IOWR	tsuREG(IOWR)	5	—	—	ns
-REG hold following -IOWR	thREG(IOWR)	0	—	—	ns
-IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
-IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

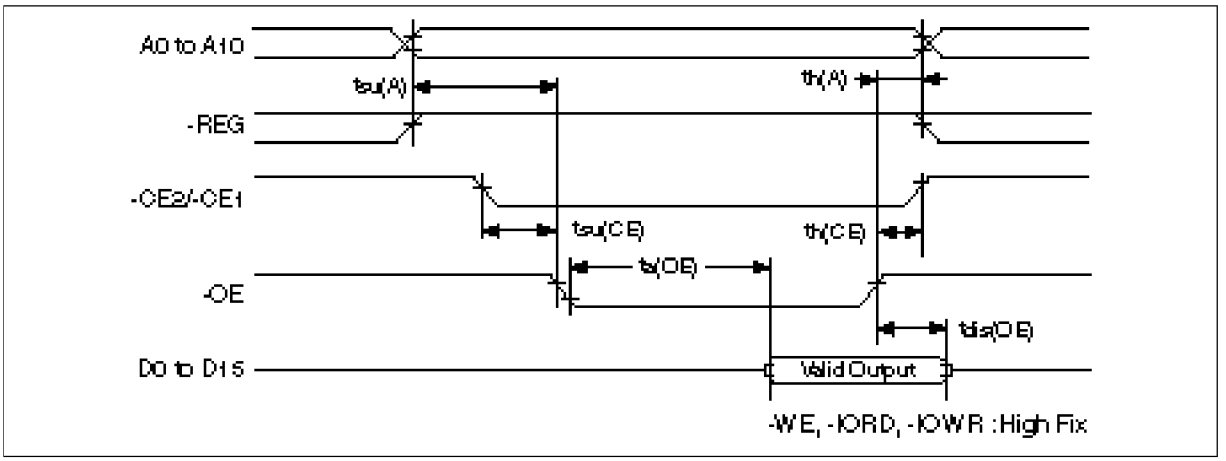
I/O Access Write Timing



Common Memory Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
-OE access time	ta(OE)	—	—	125	ns
Output disable time (-OE)	tdis(OE)	—	—	100	ns
Address setup time	tsu(A)	30	—	—	ns
Address hold time	th(A)	20	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
-CE hold time	th(CE)	20	—	—	ns

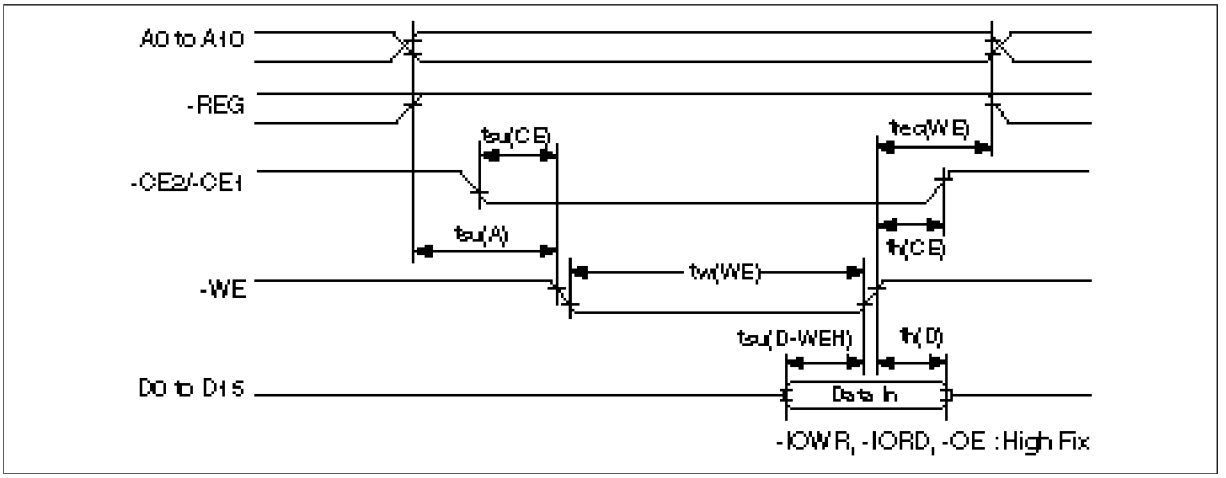
Common Access Read Timing



Common Memory Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup time (-WE)	tsu(D-WEH)	80	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write pulse time	tw(WE)	150	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
Write recover time	trec(WE)	30	—	—	ns
-CE hold following -WE	th(CE)	20	—	—	ns

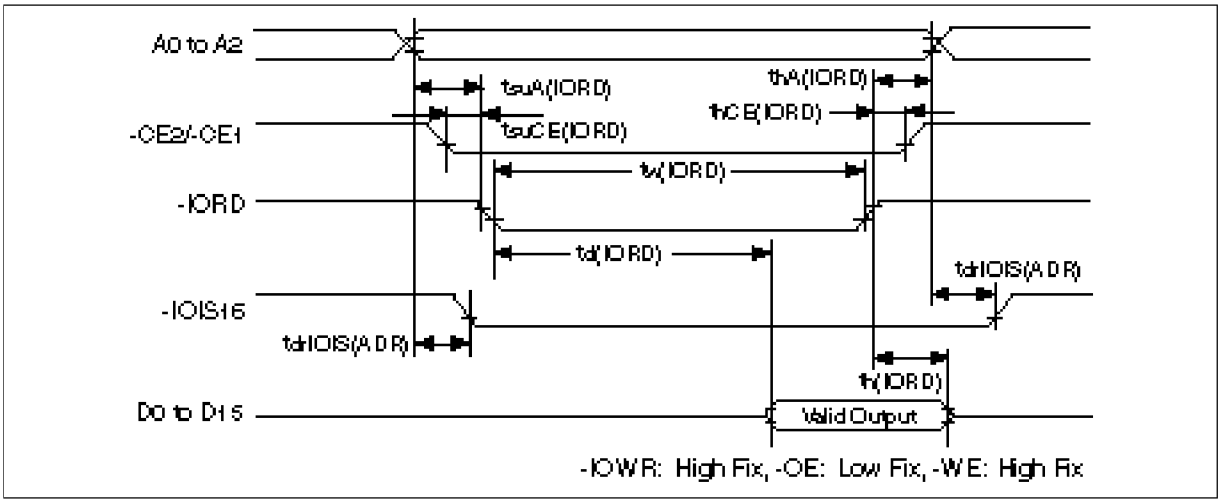
Common Access Write Timing



True IDE Mode Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
data delay after IORD	td(IORD)	—	—	100	ns
data hold following IORD	th(IORD)	0	—	—	ns
IORD width time	tw(IORD)	165	—	—	ns
address setup before IORD	tsuA(IORD)	70	—	—	ns
address hold following IORD	thA(IORD)	20	—	—	ns
CE setup before IORD	tsuCE(IORD)	5	—	—	ns
CE hold following IORD	thCE(IORD)	20	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tdfIOIS16(ADR)	—	—	35	ns

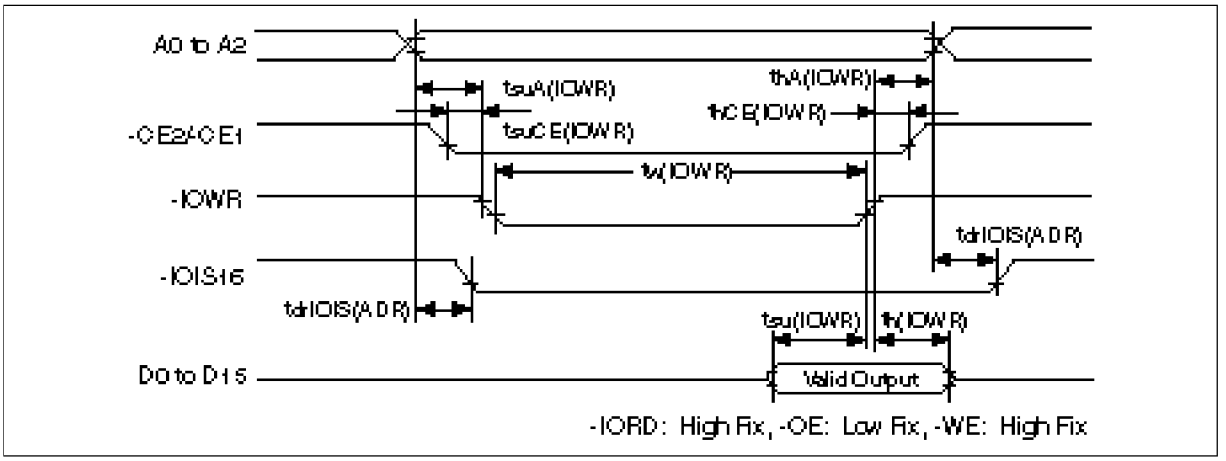
True IDE Mode Access Read Timing



True IDE Mode Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before IOWR	tsu(IOWR)	60	—	—	ns
data hold following IOWR	th(IOWR)	30	—	—	ns
IORD width time	tw(IOWR)	165	—	—	ns
address setup before IOWR	tsuA(IOWR)	70	—	—	ns
address hold following IOWR	thA(IOWR)	20	—	—	ns
CE setup before IOWR	tsuCE(IOWR)	5	—	—	ns
CE hold following IOWR	thCE(IOWR)	20	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tdfIOIS16(ADR)	—	—	35	ns

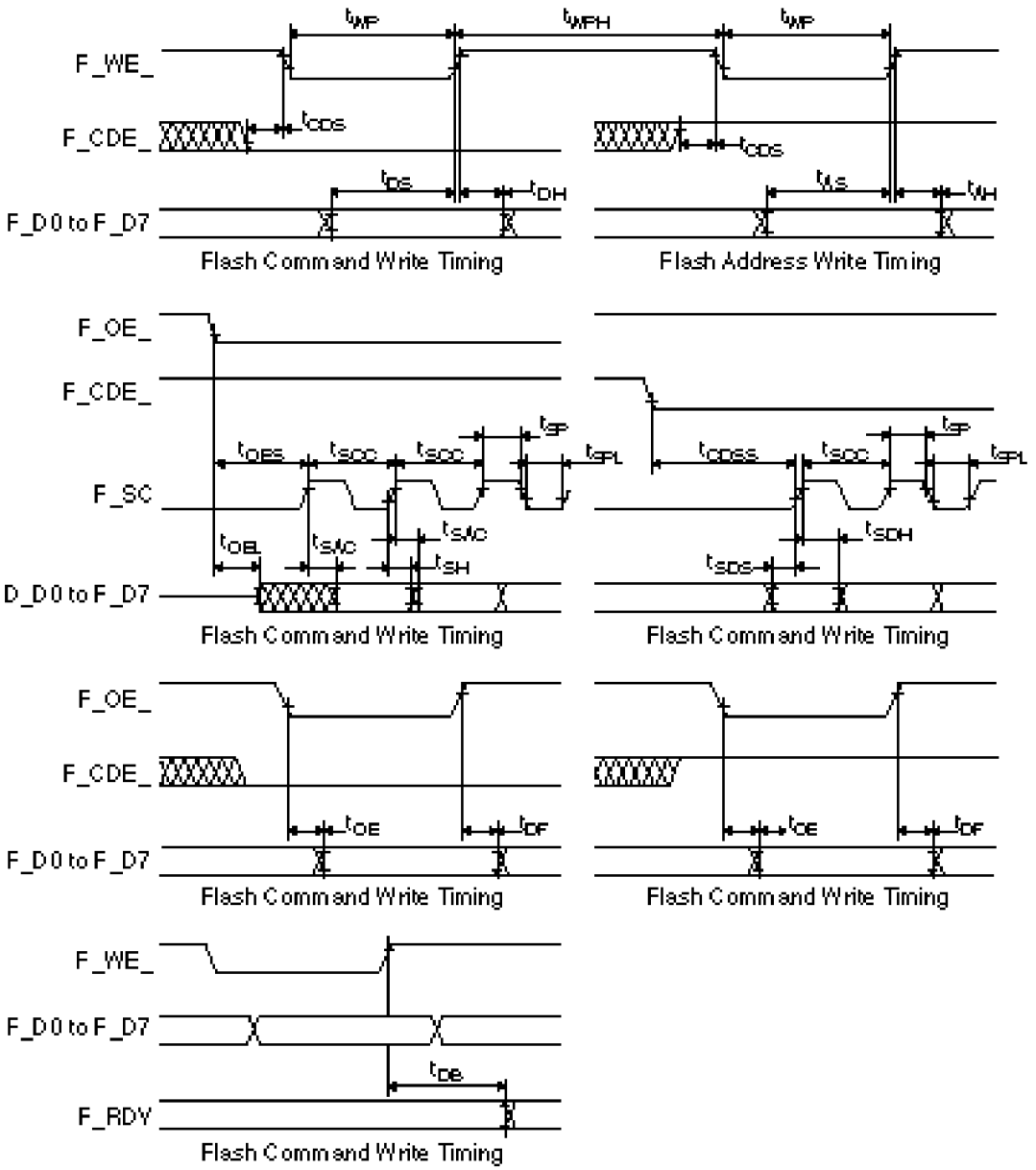
True IDE Mode Access Write Timing



Flash Memory Interface AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse time	t_{WP}	60	—	—	ns
Write pulse high time	t_{WPH}	40	—	—	ns
F_CDE_ setup time for F_WE_	t_{CDS}	0	—	—	ns
Data setup time	t_{DS}	50	—	—	ns
Data hold time	t_{DH}	10	—	—	ns
Address setup time	t_{AS}	50	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
F_OE_ setup time for F_SC	t_{OES}	0	—	—	ns
F_OE_ low to output low-z	t_{OEL}	0	—	—	ns
F_CDE_ setup time for F_SC	t_{CDSS}	1.5	—	—	µs
Serial clock cycle time	t_{SCC}	50	—	—	ns
F_SC pulse width	t_{SP}	20	—	—	ns
F_SC pulse low time	t_{SPL}	20	—	—	ns
F_SC to output delay	t_{SAC}	—	—	50	ns
F_SC to output hold	t_{SH}	15	—	—	ns
Data setup time for F_SC	t_{SDS}	0	—	—	ns
Data hold time for F_SC	t_{SDH}	30	—	—	ns
F_OE_ to output delay	t_{OE}	—	—	60	ns
F_OE_ high to output flat	t_{DF}	—	—	40	ns
Time to device busy	t_{DB}	—	—	150	ns

Flash Memory Interface timing



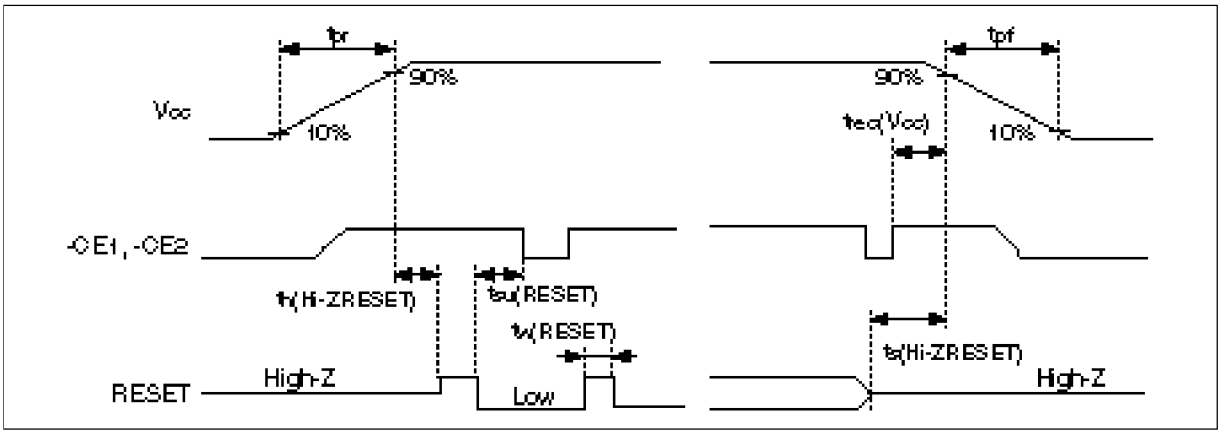
Note: F_OE_: Connect to F_OE_A0B, F_OE_A1B, F_OE_B0B and F_OE_B1B.
F_WE_: Connect to F_WE_A0B, F_WE_A1B, F_WE_B0B and F_WE_B1B.
F_CDE_: Connect to F_CDE_AB and F_CDE_BB.
F_SC: Connect to F_SC_A0, F_SC_A1, F_SC_B0 and F_SC_B1.
F_D0 to F_D7: Connect to F_D_A[0] to F_D_A[7] and F_D_B[0] to F_D_B[7].
F_RDY_: Connect to F_RDY.

Reset Characteristics (only Memory Card Mode or I/O Card Mode)

Hard Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reset setup time	tsu(RESET)	100	—	—	ms	
-CE recover time	trec(VCC)	1	—	—	µs	
VCC rising up time	tpr	0.1	—	100	ms	
VCC falling down time	tpf	3	—	300	ms	
Reset pulse width	tw(RESET)	10	—	—	µs	
	th(Hi-ZRESET)	1	—	—	ms	
	ts(Hi-ZRESET)	0	—	—	ms	

Hard Reset Timing

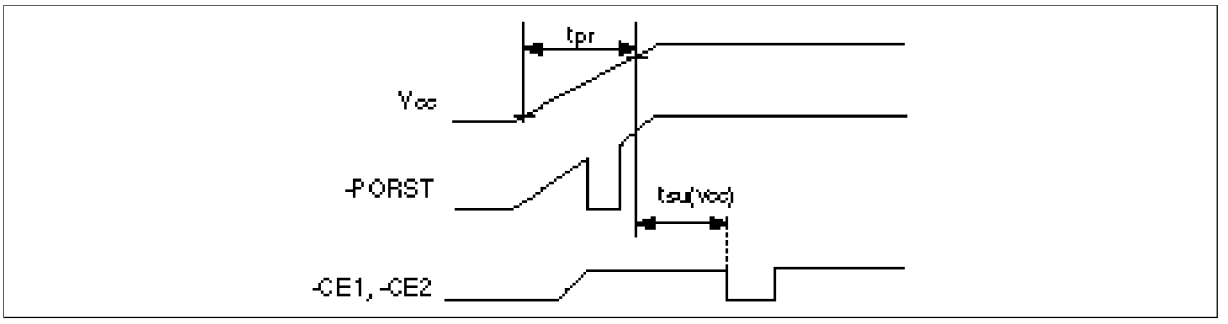


Power on Reset Characteristics

Power on reset sequence must need by -PORST at the rising of V_{CC}.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
-CE setup time	tsu(VCC)	100	—	—	ms	
VCC rising up time	tpr	0.1	—	100	ms	

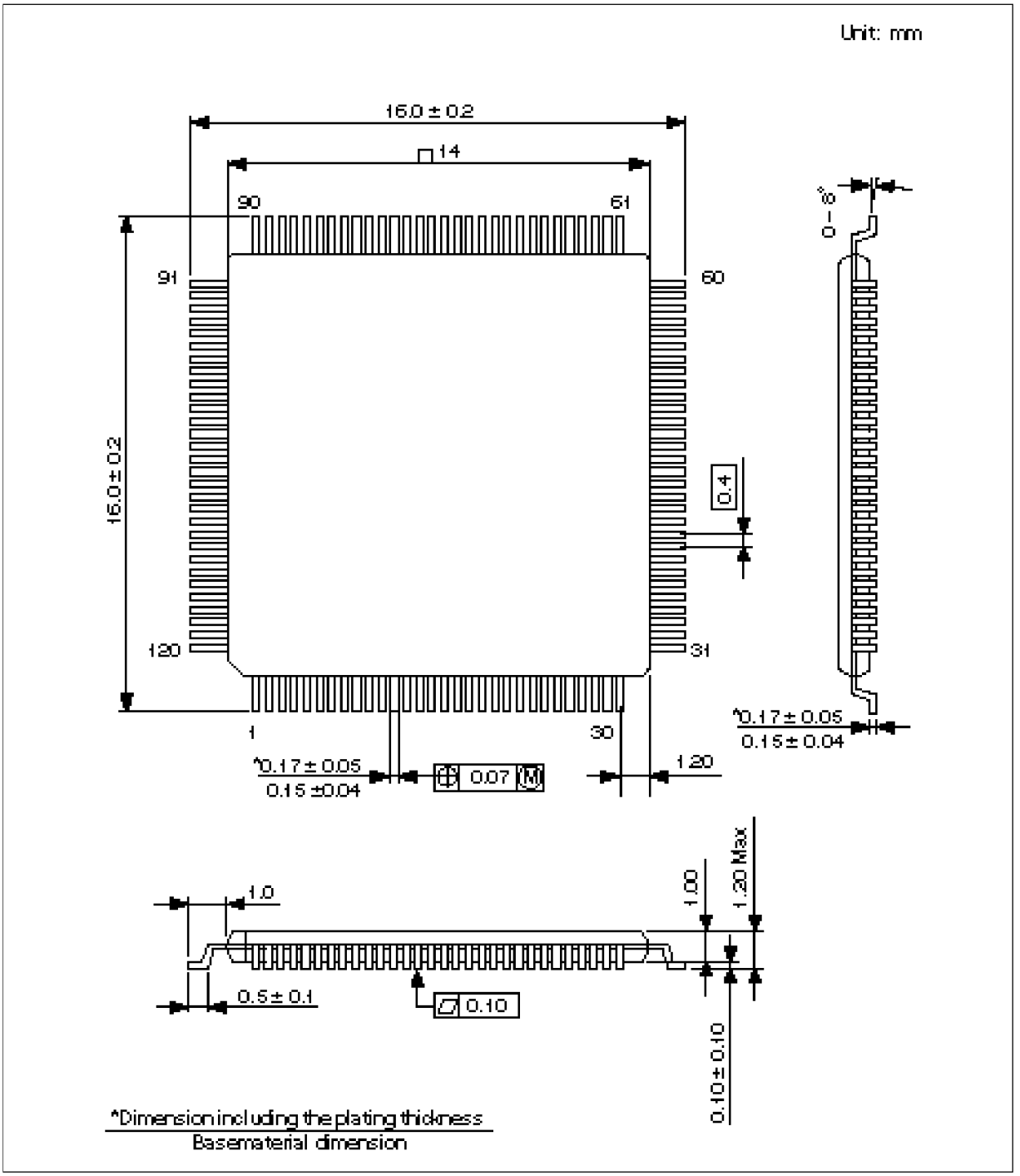
Power on Reset Timing



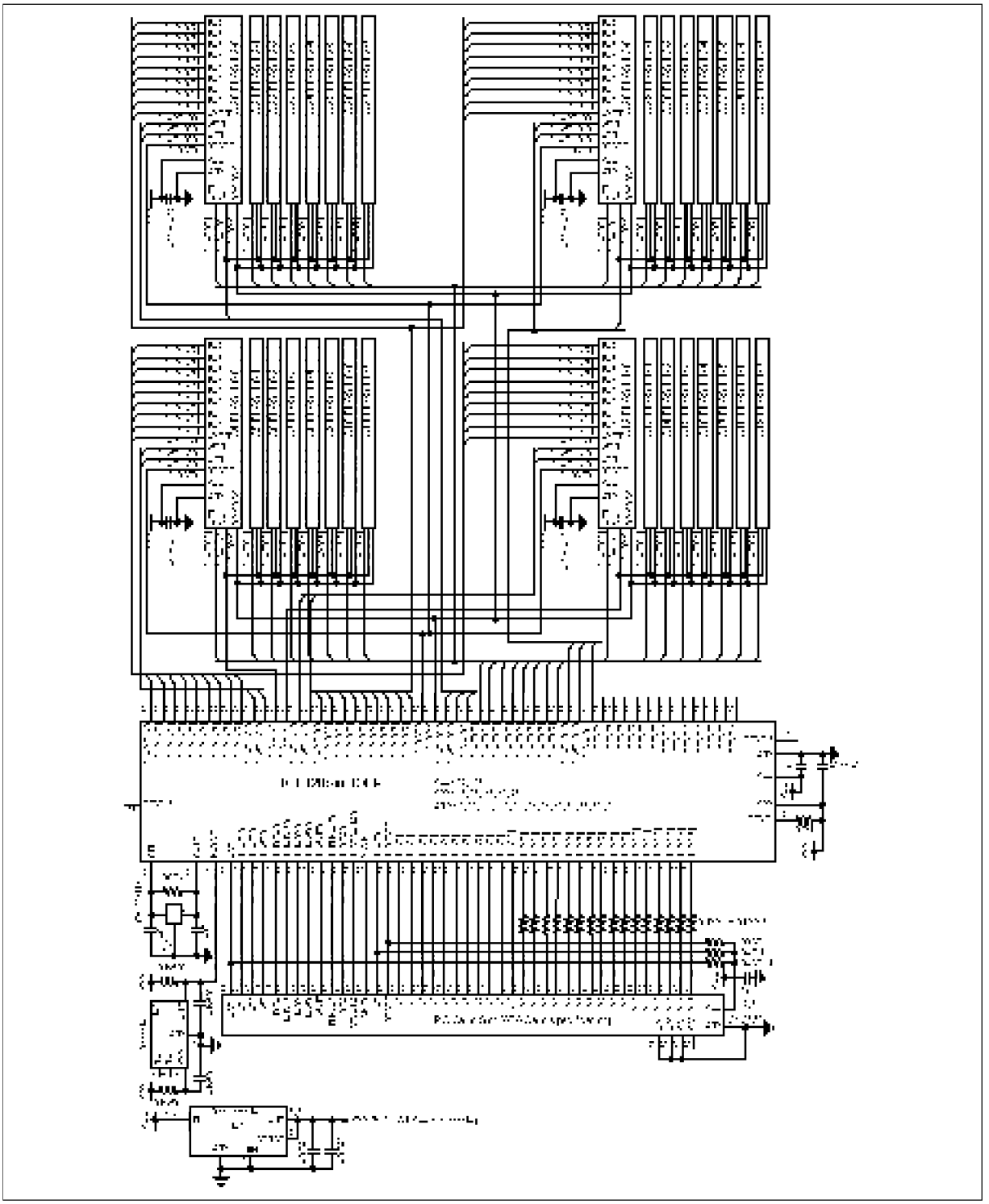
Attention for Card Use

- In the reset or power off, all register informations are cleared.
- Notice that the card insertion/removal should not be executed during host is active, if the card is used in True IDE mode.
- After the card hard reset, soft reset, or power on reset, ATA reset, command applied the card cannot access during +RDY/-BSY pin is "low" level. Flash card can't be operated in this case.
- Notice that the card removal should be executed after card internal operations completed.
- Before the card insertion V_{CC} can not be supplied to the card. After confirmation that -CD1, -CD2 pins are inserted, supply V_{CC} to the card.
- -OE must be kept at the V_{CC} level during power on reset in memory card mode and I/O card mode. -OE must be kept constantly at the GND level in True IDE mode.

Physical Outline



Schematic Flash Card (Reference only)



Equipped flash memory

Pieces of flash memory	Equipped flash memory
32	0–0 to 3–7
20	0–0 to 2–3
10	0–0 to 0–7, 1–0 to 1–1
6	0–0 to 0–5
4	0–0 to 0–3
2	0–0 to 0–1
1	0–0

Sample bill of materials

Item	Specification
IC1	Controller
IC2	Reset IC
IC3	Regulators
Xtal	20 MHz
RRST	100 kΩ
RPWR1	2 kΩ
RPWR2	100 kΩ
RXTAL	1 MΩ
RTM	2 kΩ
ROBU	100 kΩ
RCSBLU	100 kΩ
RHDD0 to RHDD15	0 Ω
CPWR1	1 µF
CPWR2	0.1 µF
CXI, CXO	10 pF
C0	1 µF
C1 to C35	0.1 µF
CRBG1 to CRBG2	4.7 µF

PC card slot pin

Signal name (I/O card mode)	ATA card specification	CompactFlash™ card specification
VCC	17, 51	13, 38
-SPKR	62	45
-CSEL	56	39
A0	29	20
A1	28	19
A2	27	18
A3	26	17
A4	25	16
A5	24	15
A6	23	14
A7	22	12
A8	12	11
A9	11	10
A10	8	8
D0	30	21
D1	31	22
D2	32	23
D3	2	2
D4	3	3
D5	4	4
D6	5	5
D7	6	6
D8	64	47
D9	65	48
D10	66	49
D11	37	27
D12	38	28
D13	39	29
D14	40	30
D15	41	31
-CE1	7	7
-OE	9	9
-WE	45	36
-IRQ	46	37
-IOIS16	33	24
-CE2	42	32
-IORD	44	34
-IOWR	45	35
RESET	58	41
-WAIT	59	42
-INPACK	60	43
-RBG	61	44
-STSCHG	63	46
GND	1, 34, 35, 68	1, 50
-CD1	36	25
-CD2	67	26
-VS1	43	33
-VS2	57	40

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Apr. 21, 1999	Initial issue	M. Shirai	Y. Nakamura
1.0	May. 21, 1999	Correct error: Other Pin Explanation Change of description for TEST1 22. Translater sector: Addition of description Absolute Maximum Ratings Addition of notes2 and 3 DC Characteristics and AC Characteristics Addition of conditions: V_{DD} = 3.3 V ± 5% DC Characteristics-1 V_{OH} (1 mA) test conditions: I_{OH} = –1 mA to I_{OH} = –0.5 mA V_{OH} (3 mA) test conditions: I_{OH} = –3 mA to I_{OH} = –1 mA DC Characteristics-2 V_{OH} (3 mA) test conditions: I_{OH} = –8 mA to I_{OH} = –2 mA		