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MB501SL

DATA SHEET

SUPER LOW POWER TWO MODULUS PRESCALER

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The Fujitsu MB501SL is a super low power version of the MB501 two modulus prescaler used with a frequency synthesizer to make a Phase Locked Loop (PLL). It divides the input frequency by the modulus of 64/65 or 128/129, respectively. The MB501SL achieves extremely small stray capacitance by the use of Fujitsu's Advanced Process Technology. High speed operation is achieved with low power supply current of 5mA which is about half of the current value of the MB501L.

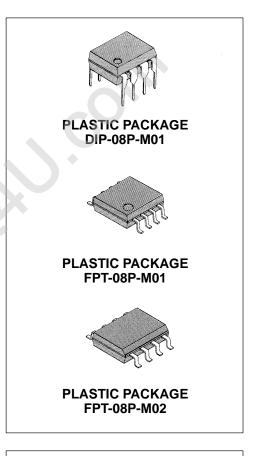
- High Frequency Operation: fmax = 1.1GH_Z max.(P_{IN} = -14bBm)
- Pulse Swallow Function: 64/65, 128/129
- Low Power Supply Current: 5.0mA typ.
- Stable Output Amplitude: V_O = 1.6Vp-p typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Dual-In-Line Package
- Plastic 8-pin Mini Flat Package
- Built-in Termination Resistor
- · Stable output amplitude is obtained up to output load capacitance of 8pF.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

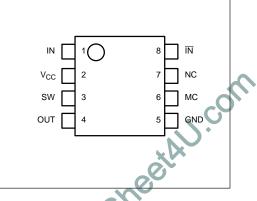
Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	-0.5 to +7.0	V
Input Voltage	V _{IN}	-0.5 to + V _{CC}	V
Output Voltage	Io	10	mA
Storage Temperature	T _{STG}	– 55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

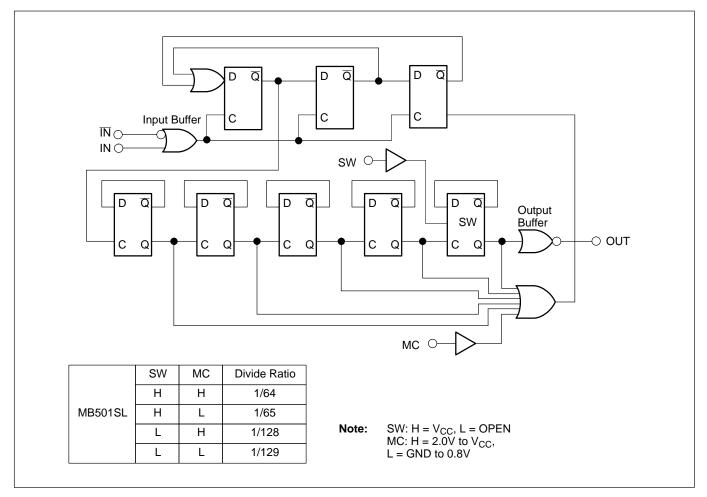


Figure 1. MB501SL Block Diagram

PIN DESCRIPTION

Pin Number	Symbol	Description	
1	IN	Input	
2	V _{CC}	Power Supply, +5V	
3	SW	Divide Ratio Control Input (See Divide Ratio Table)	
4	OUT	Output	
5	GND	Ground	
6	MC	Modulus Control Input (See Divide Ratio Table)	
7	NC	Non Connection	
8	ĪN	Complementary Input	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values			11	
		Min.	Тур.	Max.	Unit	
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V	
Operating Temperature	T _A	-40	_	+85	°C	
Load Capacitance	CL	_	_	8	pF	

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Denemator	0 milest	Condition	Values			
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Power Supply Current	I _{CC}	_	_	5.0	7.0	mA
Output Amplitude	Vo	Built-in a termination resistor. Load capacitance = 8pF	1.0	1.6	_	V _{P-P}
Input Frequency	fin	With input coupling capacitor 1000pF	10		1100	MNz
Input Signal Amplitude	P _{IN}	_	-14	_	0	dBm
High Level Input Voltage for MC	V _{IHM}	_	2.0	_	_	V
Low Level Input Voltage for MC	V _{ILM}	_	_	_	0.8	V
High Level Input Voltage for SW	V _{IHS} *	_	V _{CC} –0.1	V _{CC}	V _{CC} +0.1	V
Low Level Input Voltage for SW	V _{ILS}	_	OPEN		V	
High Level Input Current for MC	I _{IHM}	V _{IH} = 2.0V	_	_	0.4	mA
Low Level Input Current for MC	I _{ILM}	V _{IL} = 0.8V	-0.2	_	_	mA
Modulus Set-up Time MC to Output	t _{SET}	_	_	16	26	ns

Note: * Design Guarantee

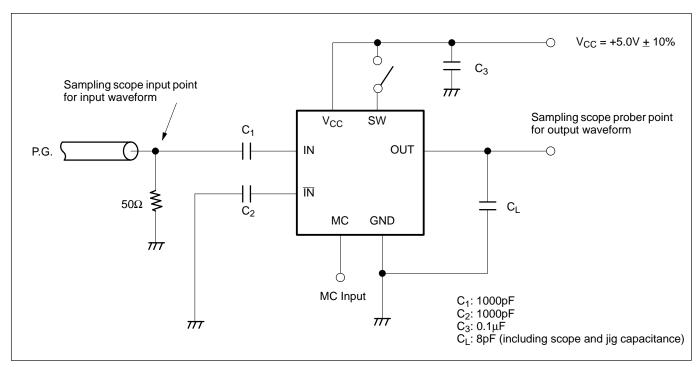
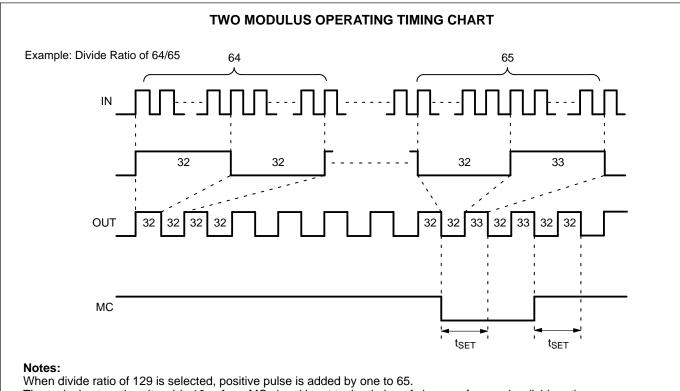


Figure 2. Test Circuit



The typical set up time (t_{SET}) is 16ns from MC signal input to the timing of change of prescaler divide ratio.

TYPICAL CHARACTERISTICS CURVES

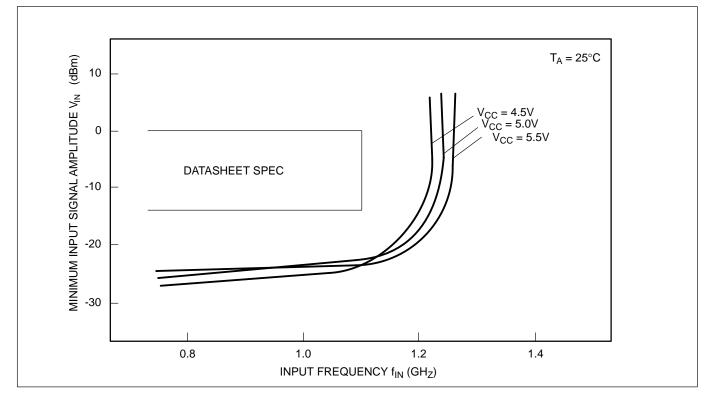


Figure 3. Input Signal Amplitude vs. Input Frequency

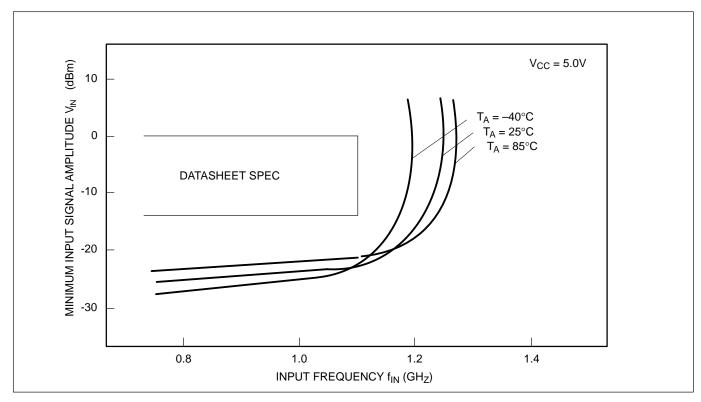


Figure 4. Input Signal Amplitude vs. Input Frequency

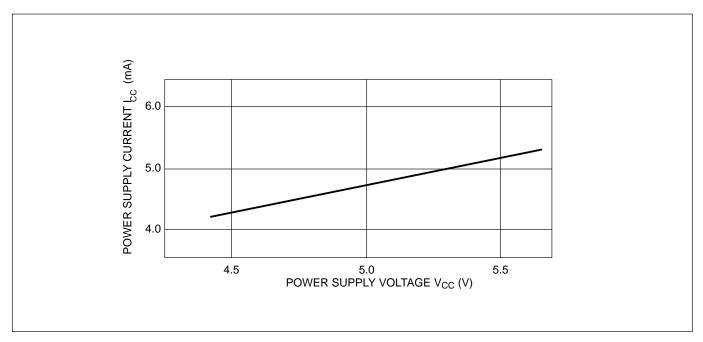


Figure 5. Power Supply Current vs. Power Supply Voltage

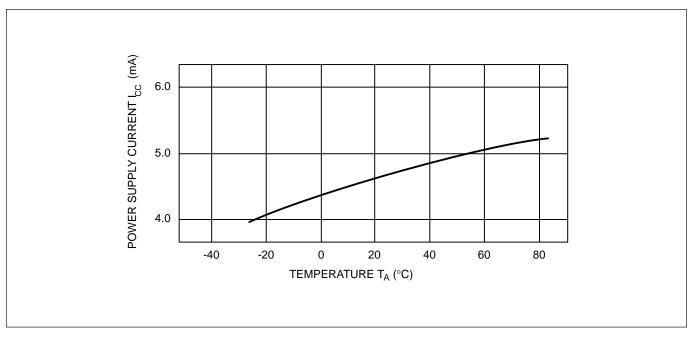


Figure 6. Power Supply Current vs. Temperature

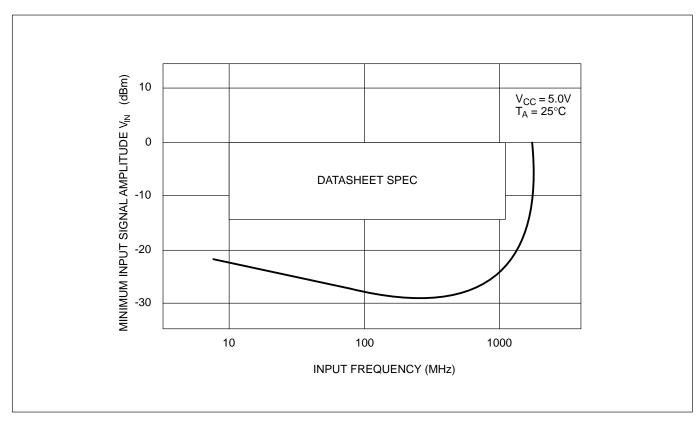


Figure 7. Input Signal vs. Input Frequency

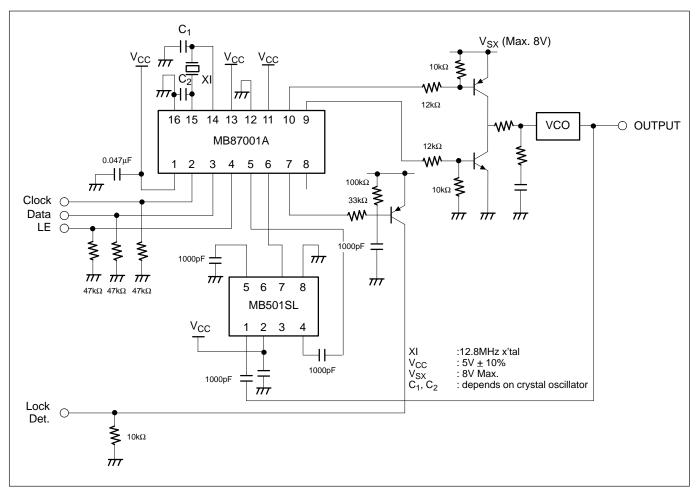
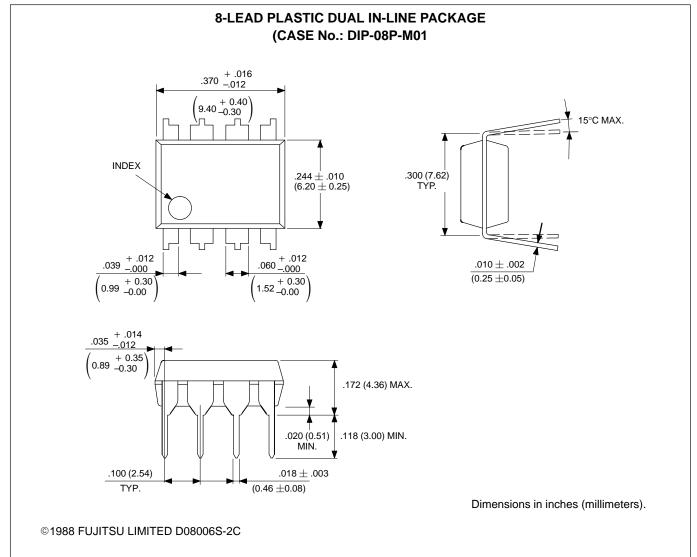
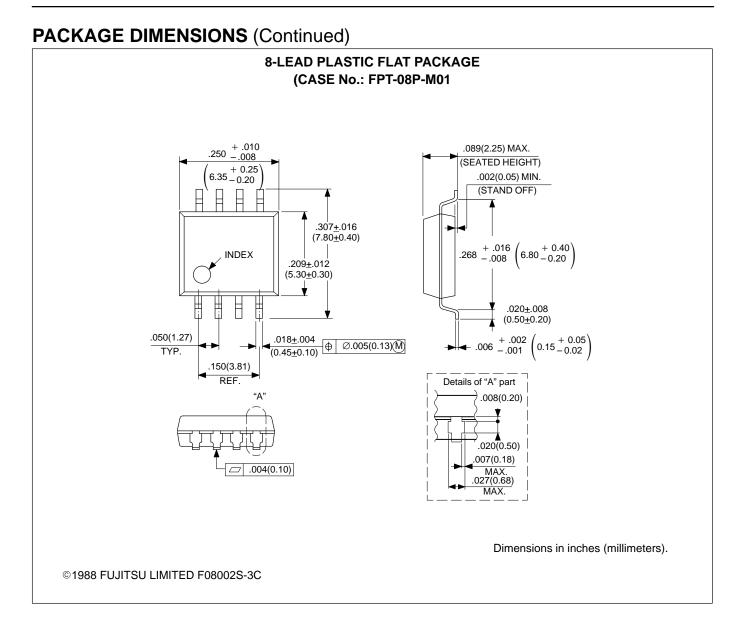
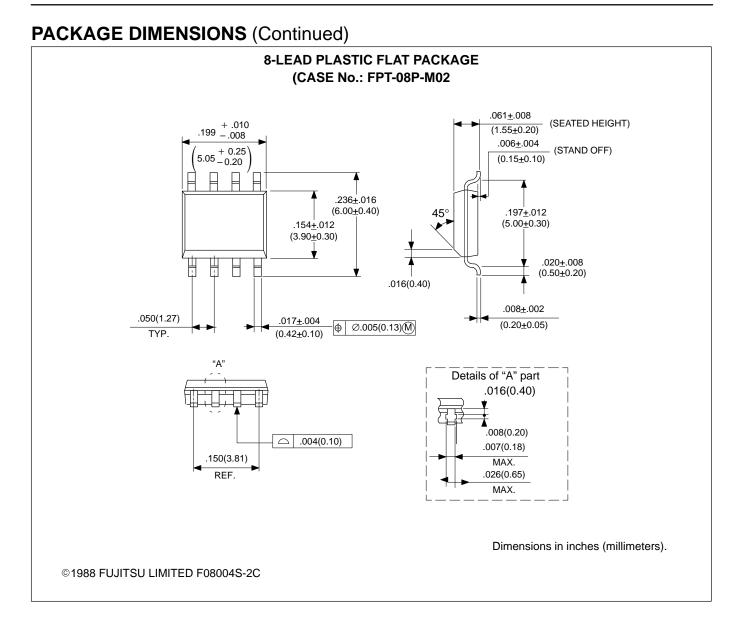


Figure 8. Typical Application Example

PACKAGE DIMENSIONS







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Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete information sufficient for construction purposes is not necessarily given.

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