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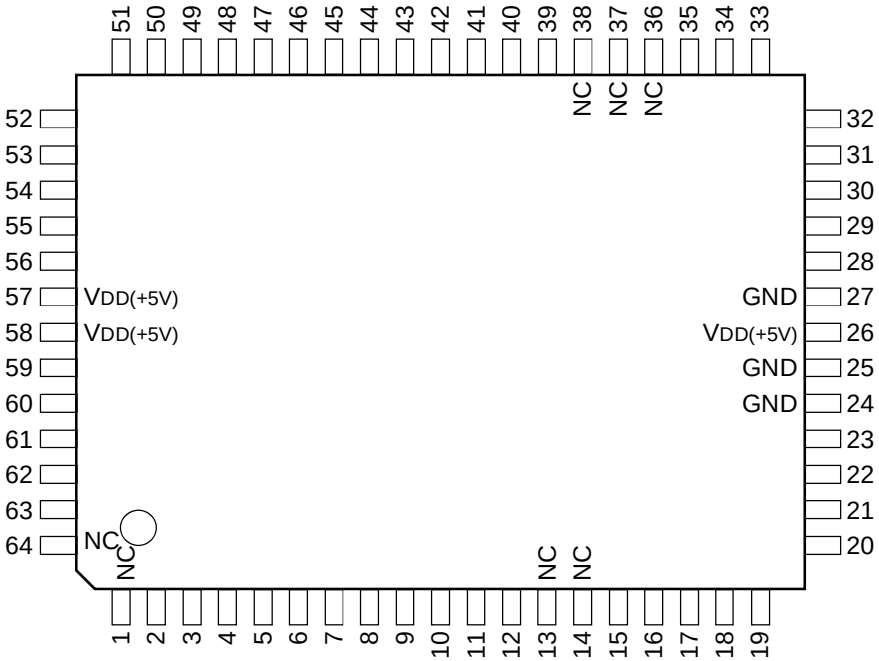
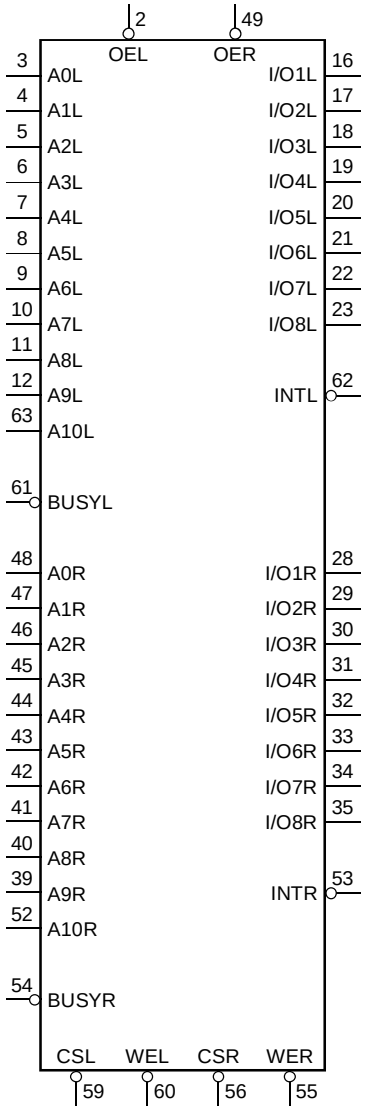
C-MOS 64K-BIT DUAL PORT STATIC RAM

–TOP VIEW–

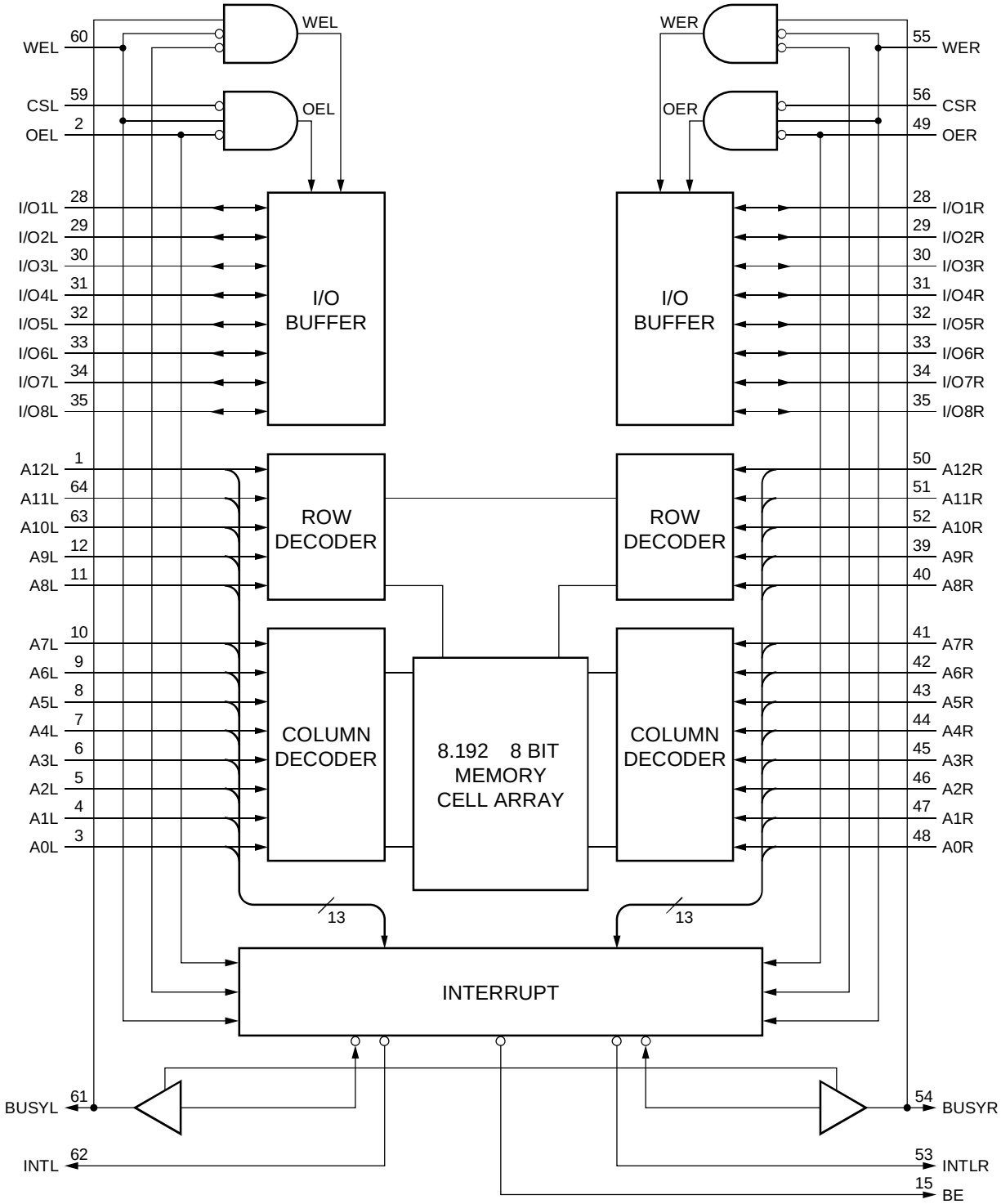


(VDD = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	A12L	17	I/O	I/O2L	33	I/O	I/O6R	49	I	$\overline{OER}$
2	I	OEL	18	I/O	I/O3L	34	I/O	I/O7R	50	I	A12R
3	I	A0L	19	I/O	I/O4L	35	I/O	I/O8R	51	I	A11R
4	I	A1L	20	I/O	I/O5L	36	—	NC	52	I	A10R
5	I	A2L	21	I/O	I/O6L	37	—	NC	53	O	$\overline{INTR}$
6	I	A3L	22	I/O	I/O7L	38	—	NC	54	I	$\overline{BUSYR}$
7	I	A4L	23	I/O	I/O8L	39	I	A9R	55	I	$\overline{WER}$
8	I	A5L	24	—	GND	40	I	A8R	56	I	$\overline{CSR}$
9	I	A6L	25	—	GND	41	I	A7R	57	—	VDD
10	I	A7L	26	—	VDD	42	I	A6R	58	—	VDD
11	I	A8L	27	—	GND	43	I	A5R	59	I	$\overline{CSL}$
12	I	A9L	28	I/O	I/O1R	44	I	A4R	60	I	$\overline{WEL}$
13	—	NC	29	I/O	I/O2R	45	I	A3R	61	I	$\overline{BUSYL}$
14	—	NC	30	I/O	I/O3R	46	I	A2R	62	O	$\overline{INTL}$
15	O	$\overline{BE}$	31	I/O	I/O4R	47	I	A1R	63	I	A10L
16	I/O	I/O1L	32	I/O	I/O5R	48	I	A0R	64	I	A11L



A0L - A10L,		
A0R - A10R	;	ADDRESS INPUTS
$\overline{BE}$	;	BUSY OUTPUT ENABLE
$\overline{BUSY}$L, $\overline{BUSY}$R	;	BUSY INPUTS
$\overline{CS}$L, $\overline{CS}$R	;	CHIP SELECT INPUTS
I/O0L - I/O10L,		
I/O0R - I/O10R	;	DATA INPUTS/OUTPUTS
$\overline{INT}$L, $\overline{INT}$R	;	INTERRUPT OUTPUTS
$\overline{OE}$L, $\overline{OE}$R	;	OUTPUT ENABLE INPUTS
$\overline{WE}$L, $\overline{WE}$R	;	WRITE ENABLE INPUTS


WEL
60
WEL
CSL
59
OEL
2
OEL
I/O1L
28
I/O2L
29
I/O3L
30
I/O4L
31
I/O5L
32
I/O6L
33
I/O7L
34
I/O8L
35
I/O BUFFER
A12L
1
A11L
64
A10L
63
A9L
12
A8L
11
ROW DECODER
A7L
10
A6L
9
A5L
8
A4L
7
A3L
6
A2L
5
A1L
4
A0L
3
COLUMN DECODER
8.192 8 BIT MEMORY CELL ARRAY
13
INTERRUPT
BUSYL
61
INTL
62
WER
55
WER
OER
56
CSR
49
OER
I/O1R
28
I/O2R
29
I/O3R
30
I/O4R
31
I/O5R
32
I/O6R
33
I/O7R
34
I/O8R
35
I/O BUFFER
A12R
50
A11R
51
A10R
52
A9R
39
A8R
40
ROW DECODER
A7R
41
A6R
42
A5R
43
A4R
44
A3R
45
A2R
46
A1R
47
A0R
48
COLUMN DECODER
13
BUSYR
54
INTLR
53
BE
15