MB89351
SCSI Protocol Controller

Edition 1.0
June 1990

AC CHARACTERISTICS

The Fujitsu MB89351 is a Small Computer System Interface (SCSI) Protocol Controller (SPC) specifically designed to implement a SCSI-bus to CPU/DMAC interface. Except for SCSI synchronous mode transfers, the MB89351 can handle virtually all interface control procedures of the SCSI bus laid down by SCSI-I specification (ANSI X3.131-1986) and is adaptable to either an 8-bit or a 16-bit CPU. To optimize efficiency and reduce CPU overhead, the MB89351 uses an 8-byte FIFO data buffer register and a 24-bit transfer byte counter. The SPC can serve in a wide range of applications acting as an INITIATOR or TARGET device for the SCSI. Thus, the device can be used as an I/O controller or as a host adapter.

The MB89351 SPC is fabricated in silicon-gate CMOS and housed in a 64-pin plastic shrink DIP or a 64-pin plastic flat package.

SCSI Compatibility

- Serves as either an INITIATOR or a TARGET
- DMA interface and parity check

Data Transfer Rate/Byte Counter

- Up to 3.0 Megabytes per second
- 8-byte FIFO Data Buffer
- 24-Bit transfer byte counter

Drive Options

- Single-ended
- Differential

Selectable Transfer Mode

- DMA transfer
- Program transfer
- Manual transfer

Clock Requirements

- 8 MHz clock with 33%-to-66% duty cycle

Technology/Power Requirements

- Silicon-Gate CMOS
- Single +5 V power supply

Available Packaging

- 64-pin plastic shrink DIP (suffix -PSH)
- 64-pin plastic flat package (suffix -PF)

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Designator	Values		Unit
		Min.	Max.	
Supply Voltage	V_{CC}	V_{SS} – .05	V_{SS} + 7.0	V
Input Voltage[2]	V_{IN}	V_{SS} – .05	V_{SS} + 7.0	V
Output Voltage[2]	V_{OUT}	V_{SS} – 0.3	V_{SS} + 7.0	V
Operating Ambient Temperature	T_A	0	+70	°C
Storage Temperature	T_{STG}	–55	+150	°C

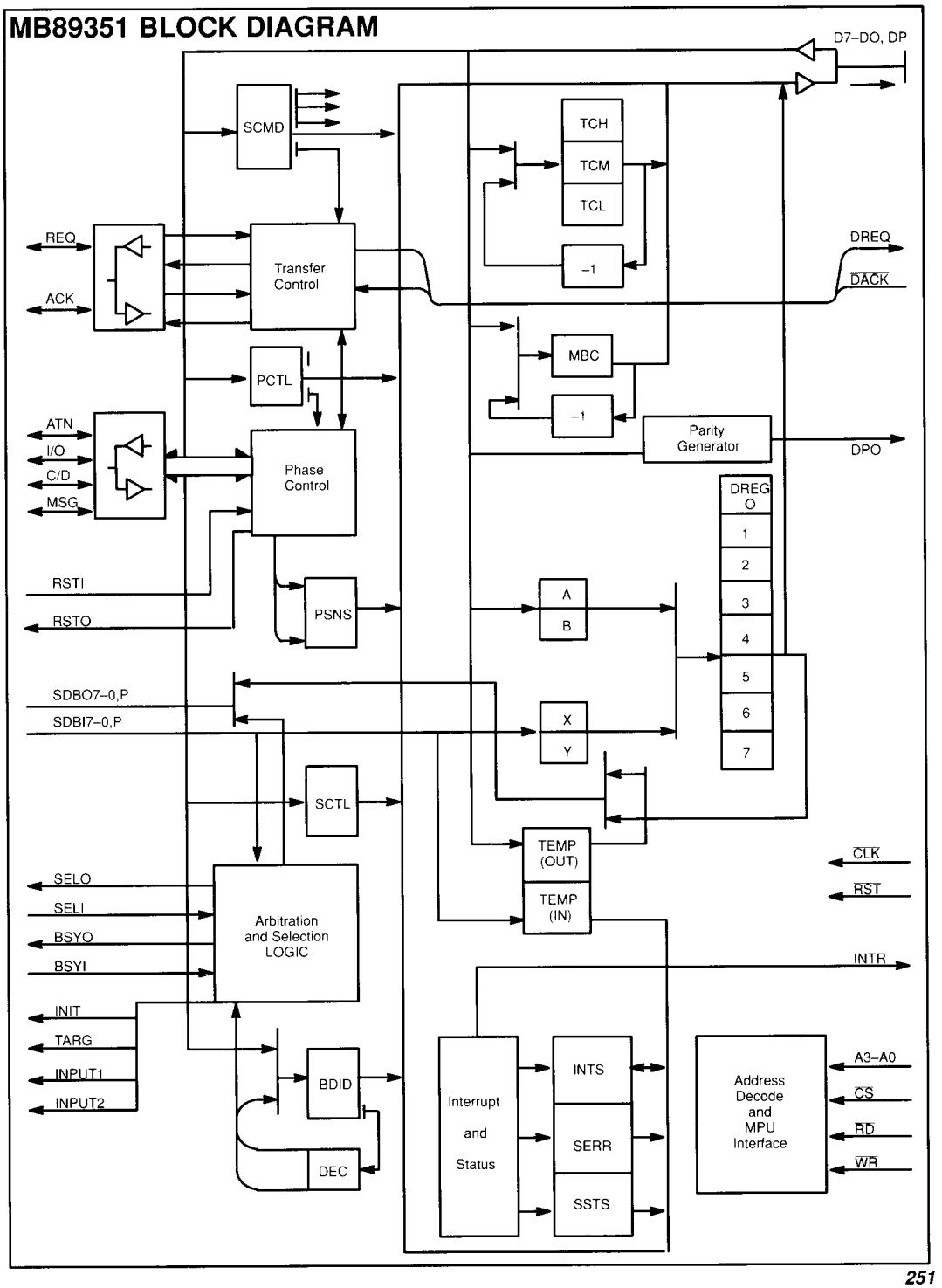
Notes: 1 Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2 Should not exceed V_{CC} + 0.5V.

RECOMMENDED OPERATING CONDITIONS

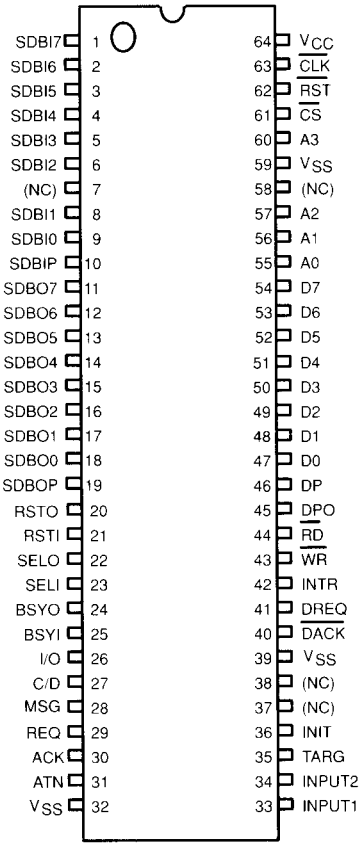
Parameter	Designator	Values			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.50	5.0	5.50	V	
	V_{SS}		0		V	
Operating Ambient Temperature	T_A	0		+70	°C	

MB89351 BLOCK DIAGRAM

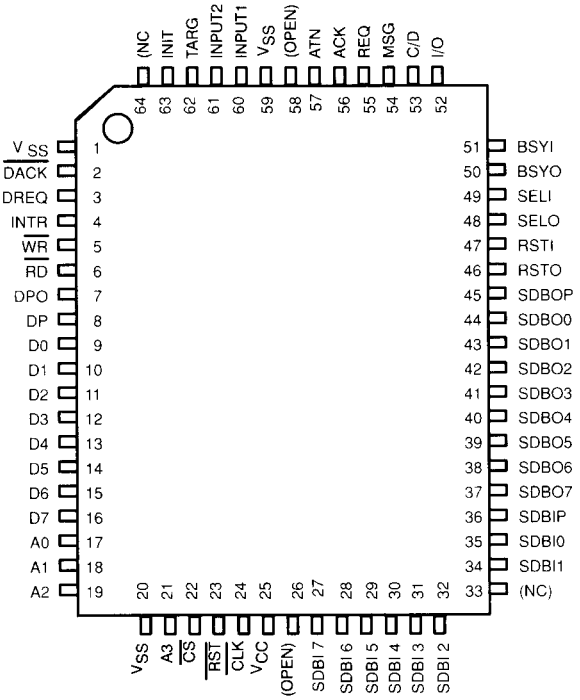


PIN ASSIGNMENTS AND INTERFACE DIAGRAM

(TOP VIEW)

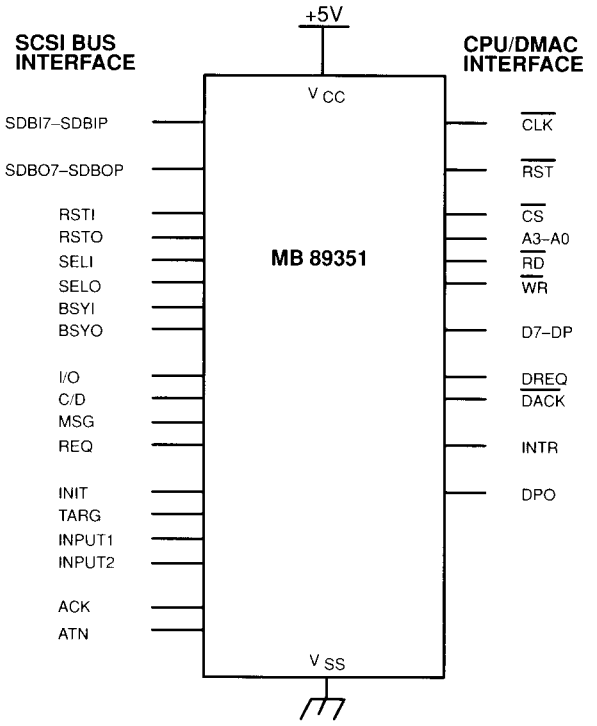


DIP–64P–M01



FPT – 64P – M01

PIN ASSIGNMENTS AND INTERFACE DIAGRAM



PIN DESCRIPTIONS

Designator	Pin No.		Function
	DIP	FPT	
V_{CC}	64	25	+5V power supply.
V_{SS}	32,39,59	1,20,59	Circuit ground.
$\overline{CLK}$	63	24	Clock input for controlling internal operation and data transfer speed of the SPC.
$\overline{RST}$	62	23	Asynchronous reset signal used to clear all internal circuits of the SPC.
$\overline{CS}$	61	22	Input selection enable signal for accessing an internal register. When active low, the following input/output signals are valid: RD, WR, A0–A3, DP0–DP7 and DP.
A3 A2 A1 A0	60 57 56 55	21 19 18 17	Address input signals for selecting an internal register in SPC. MSB is A3; LSB is A0. When $\overline{CS}$ is active low, read/ write is enabled for an internal register selected by these address inputs via data bus lines D0–D7 and DP.
$\overline{RD}$	44	6	The read strobe ($\overline{RD}$) input is used to readout the contents of an internal SPC register and is asserted only if $\overline{CS}$ is active low. The register to be read is specified by A0–A3; the input address data is input via D0–D7 and DP. In the program transfer mode, the falling edge of $\overline{RD}$ terminates the data read cycle.
$\overline{WR}$	43	5	The write strobe ($\overline{WR}$) input is used to write into an internal SPC register and is asserted only if $\overline{CS}$ is active low. On the falling edge of $\overline{WR}$, the data present on D0–D7 and DP is loaded into the internal register specified by A0–A3 (except when A0 = A1 = A2 = A3 = H). In the program transfer mode, the falling edge of $\overline{WR}$ indicates a data–ready condition to the MPU.

Continued on following page

PIN DESCRIPTIONS

Designator	Pin No.		Function
	DIP	FPT	
D7 – DP	54 – 46	16 – 8	Used to write/read data to/from an internal register in the SPC. The data bus is 3–state and bidirectional.The MSB is D7 and the LSB is D0; DP is an odd parity bit. When both $\overline{CS}$ and RDG inputs are active low (read operation), the contents of a selected internal register are output to the data bus. In operations other than read, the data bus is kept at a high–impedance level.
DPO	45	7	Outputs an odd parity for D0–D7. If parity bit is not generated for external memory, DPO can be used as an input parity bit for DP.
INTR	42	4	The INTR output signal is issued by the SPC and requests an interrupt to indicate completion of an internal operation or the occurrence of an error. Except for an interrupt caused by the RSTI input (reset condition in SCSI), interrupt masking is allowed. When an interrupt request is granted, the INTR signal remains active until the interrupt is cleared. In the program transfer mode, the INTR signal can be used as a data request signal instead of reading internal registers of the SPC; the data–request function is enabled by proper settings of the appropriate registers. The INTR signal is automatically disabled when interrupt conditions are not present.
DREQ	41	3	When the MB89351 is operating in the DMA mode and the data request (DREQ) output signal is active high, data is transferred between external memory and the SPC or vice–versa. During output operations, DREQ is active when the data buffers in the SPC are not full. During input operations, DREQ is active when valid data is present in the buffers. In either case, DMA transfers can occur and DREQ is asserted.
$\overline{DACK}$	40	2	An active low response signal to the DREQ which request data transfer between SPC and the external memory in the DMA mode. This signal, in DMA mode, functions similarly to the signal combination of $\overline{CS}$=low, A3=high, A2=low, A1=high, and A0=low (selection of DREG) in the program transfer mode. Since the DREG is selected by this $\overline{DACK}$ signal in the DMA mode instead of the address input from A3–A0, data transfer between DREG of SPC and external memory is possible.

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PIN DESCRIPTIONS

Designator	Pin No.		Function
	DIP	FPT	
SDBI7,SDBI6 SDBI5,SDBI4 SDBI3,SDBI2 SDBI1,SDBI0 SDBIP	1,2 3,4 5,6 8,9 10	27,28 29,30 31,32 34,35 36	Inputs from the SCSI data bus. The MSB is SDBI7; the LSB is SDBI0. SDBIP is an odd parity bit. Parity checking for the SCSI data bus is programmable.
SDBO7 SDBO6 SDBO5 SDBO4 SDBO3 SDBO2 SDBO1 SDBO0 SDBOP	11 12 13 14 15 16 17 18 19	37 38 39 40 41 42 43 44 45	Outputs to the SCSI data bus. The MSB is SDBO7; the LSB is SDBO0. SDBOP is an odd parity bit. An open-collector bus driver is used to connect the SCSI bus. **(Note: For the SDBI and SDBO pin groupings, only one pin is used for output and the other pins are used for input during arbitration. During selection, reselection, and normal data transfers, all pins are used for outputs. Typical system connections are shown in the Pin Assignments and Interface Diagram).**
RSTO,RSTI	20,21	46,47	RSTI is a reset input from other SCSI devices; RSTO is a reset output to other SCSI devices. Both signals are active high and can be masked.
SELO,SELI	22,23	48,49	SELO is an output that corresponds to the INITIATOR or TARGET device; SELI inputs the response to the SPC during the selection or reselection phase. Both signals are active high.
BSYO,BSYI	24,25	50,51	BSYO indicates the SCSI bus is in the output mode of operation, whereas, BSYI indicates the bus is operating in the input mode. One or the other of these signals is active high during arbitration and in the "connected status" mode of operation.
I/O	26	52	During the data transfer phase, the I/O signal indicates the transfer direction. When I/O is high, data is transferred from the TARGET to the INITIATOR. When I/O is low, data is transferred from the INITIATOR to the TARGET.
C/D	27	53	During the data transfer phase, the C/D signal is set high during the command-, status-, and message-phases of operation.
MSG	28	54	In the data transfer phase, the MSG signal is set high only during the message phase.

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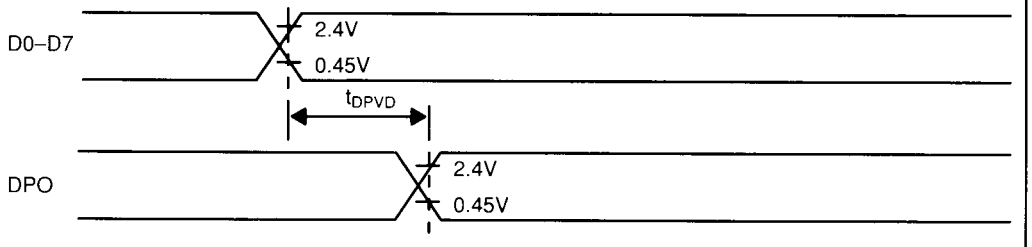
AC CHARACTERISTICS (Continued)

DPO (Data Parity Output)						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
DPO Valid Time (from D7–D0 to DPO (Valid)	t_{DPVD}	CL = 30 pF			60	ns

DPO Output Timing



AC CHARACTERISTICS (Continued)

SPC has internal registers consisting of 17 bytes that are accessible from an external circuit. These internal registers are used for controlling SPC internal operation and indicating SPC processing status/result status. A unique address is assigned to each internal register, and a particular register is identified by address bits A3 to A0. The following table shows internal register addressing:

Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select ($\overline{CS}$)	Address Bits A3	A2	A1	A0
Bus Device ID	BDID	R	0	0	0	0	0
		W					
SPC Control	SCTL	R	0	0	0	0	1
		W					
Command	SCMD	R	0	0	0	1	0
		W					
Open	—	—	0	0	0	1	1
Interrupt Sense	INTS	R	0	0	1	0	0
Reset Interrupt		W					
Phase Sense	PSNS	R	0	0	1	0	1
SPC Diagnostic Control	SDGC	W					
SPC Status	SSTS	R	0	0	1	1	0
—		W					
SPC Error Status	SERR	R	0	0	1	1	1
—		W					
Phase Control	PCTL	R	0	1	0	0	0
		W					
Modified Byte Counter	MBC	R	0	1	0	0	1
—		W					

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Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select ($\overline{CS}$)	Address Bits A3	A2	A1	A0
Data Register	DREG	R	0	1	0	1	0
		W					
Temporary Register	TEMP	R	0	1	0	1	1
		W					
Transfer Counter High	TCH	R	0	1	1	0	0
		W					
Transfer Counter Middle	TCM	R	0	1	1	0	1
		W					
Transfer Counter Low	TCL	R	0	1	1	1	0
		W					

BIT ASSIGNMENTS

The following table shows the bit assignments to each internal register. When accessing an internal register (in read/write), remember the following:

(1) The internal register block includes the read-only/write-only register and those having different meanings in read and write operations.

(2) A write command to a read-only register is ignored.

(3) If the write-only register is read out, the data and parity bit are undefined.

(4) At bit positions indicating "_" for a write in Table 3.2.2, either 1 of 0, or may be written.

Table 2. Bit Assignments for Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
0	Bus Device ID (BDID)	R	#7	#6	#5	#4	#3	#2	#1	#0	0
		W	SCSI Bus Device ID					ID4	ID2	ID1	—
1	SPC Control (SCTL)	R	Reset & Disable	Control Reset	Diag Mode	ARBIT Enable	Parity Enable	Select Enable	Reselect Enable	INT Enable	P
		W									
2	Command (SCMD)	R	Command Code			RST Out	Intercept Xfer	Transfer Modifer PRG Xfer	0	Term Mode	P
		W									
4	Interrupt Sense (INTS)	R	Selected	Reselected	Disconnect	Command Complete	Service Required	Time Out	SPC Hard Error	Reset Condition	P
		W	Reset Interrupt								—
5	Phase Sense (PSNS)	R	REQ	ACK	ATN	SEL	BSY	MSG	C/D	I/O	P
	SPC Diag Control (SDGC)	W	Diag. REQ	Diag. ACK	XFER Enable		Diag. BSY	Diag. MSG	Diag. C/D	Diag. I/O	—
6	SPC Status (SSTS)	R	Connected INIT	TARG	SPC BSY	XFER In Progress	SCSI RST	TC=0	DREG Status Full	Empty	P
		W	—								—

Continued on following page

Table 2. Bit Assignments For Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
7	SPC Error Status (SERR)	R	Data Error SCSI	Data Error SPC	XFER Out	0	TC Parity Error	0	Short XFER Period	0	P
		W	—								—
8	Phase Control (PCTL)	R	Bus Free Interrupt Enable	0				Transfer Phase MSG Out	Transfer Phase C/D Out	Transfer Phase I/O Out	P
		W									
9	Modified Byte Counter (MBC)	R	0				MBC Bit 3	MBC Bit 2	MBC Bit 1	MBC Bit 0	P
		W	—							—	P
A	Data Register (DREG)	R	Internal Data Register (8 Byte FIFO)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
B	Temporary Register (TEMP)	R	Temporary Data (Input: From SCSI)								
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
		W	Temporary Data (Output: To SCSI)								
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
C	Transfer Counter High (TCH)	R	Transfer Counter High (MSB)								
		W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	P
D	Transfer Counter Mid (TCM)	R	Transfer Counter Middle (2nd Byte)								
		W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	P
E	Transfer Counter LOW (TCL)	R	Transfer Counter Low (LSB)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise specified)

Parameter	Designator	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH}= −0.4 mA	4.0			V
Output Low Voltage	V_{0L}	I_{OL} = +3.2 mA			0.4	V
Input Leakage Current	I_{IL}	V_{IN} = 0 V to 5.25 V	−10		20	µA
Output Leakage Current	I_{IZ}	V_{IN} = 0 V to 5.25 V	−40		40	µA
Active Supply Current	I_{CC}	fc = 8MHz, All outputs open			10	mA
Standby Supply Current	I_{CS}	fc = 8 MHz, All outputs open, inputs fixed, $\overline{RST}$ active			40	µA

AC CHARACTERISTICS

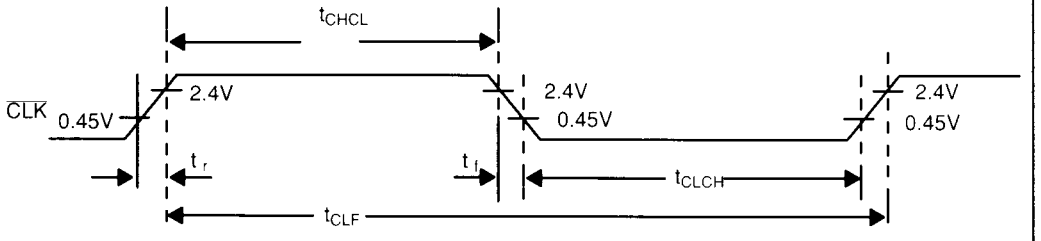
(Recommended operating conditions unless otherwise noted)

CPU/DMAC Interface

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C)

$\overline{CLK}$ Input					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{CLK}$ Cycle Time	t_{CLF}	125		200	ns
$\overline{CLK}$ High Time	t_{CHCL}	44			ns
$\overline{CLK}$ Low Time	t_{CLCH}	44			ns
$\overline{CLK}$ Rise Time	t_r			10	ns
$\overline{CLK}$ Fall Time	t_f			10	ns

$\overline{CLK}$ Input Timing

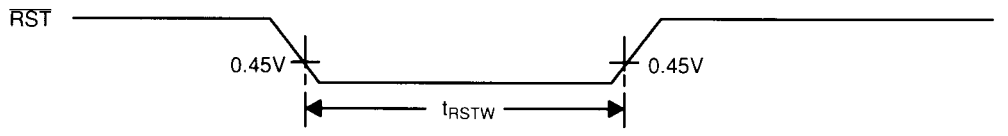


AC CHARACTERISTICS (Continued)

$\overline{\text{RST}}$ Input

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{\text{RST}}$ Pulse Width	t_{RSTW}	100			ns

$\overline{\text{RST}}$ Input Timing

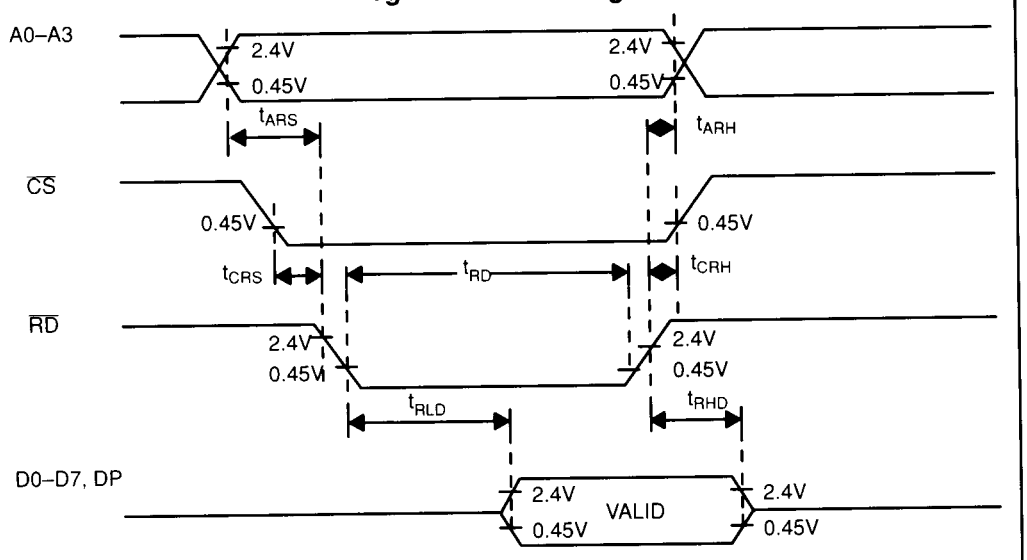


AC CHARACTERISTICS (Continued)

Register Read

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{ARS}		40			ns
Address Hold Time	t_{ARH}		10			ns
$\overline{CS}$ Setup Time	t_{CRS}		25			ns
$\overline{CS}$ Hold Time	t_{CRH}		10			ns
Data Valid Time (from $\overline{RD}$ Low)	t_{RLD}	CL = 80 pF			90	ns
Data Hold Time (from $\overline{RD}$ High)	t_{RHD}	CL = 20 pF	10		60	ns
$\overline{RD}$ Pulse Width	t_{RD}		120			ns

Register Read Timing

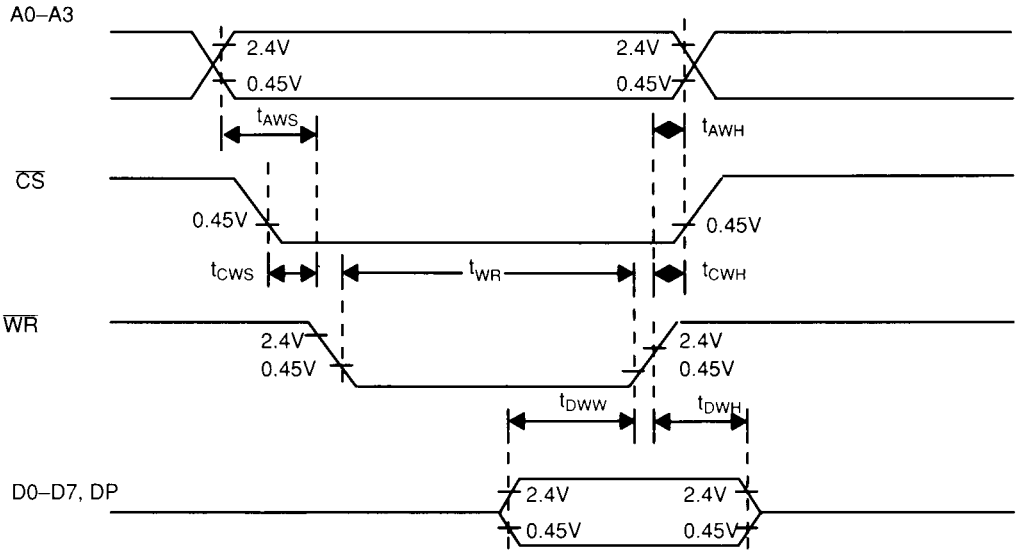


AC CHARACTERISTICS (Continued)

Register Write

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{AWS}		40			ns
Address Hold Time	t_{AWH}		10			ns
$\overline{CS}$ Setup Time	t_{CWS}		25			ns
$\overline{CS}$ Hold Time	t_{CWH}		10			ns
Data Valid Time (from $\overline{WR}$ Low)	t_{DWS}		30			ns
Data Hold Time (from $\overline{WR}$ High)	t_{DWH}		20			ns
$\overline{WR}$ Pulse Width	t_{WR}		100			ns

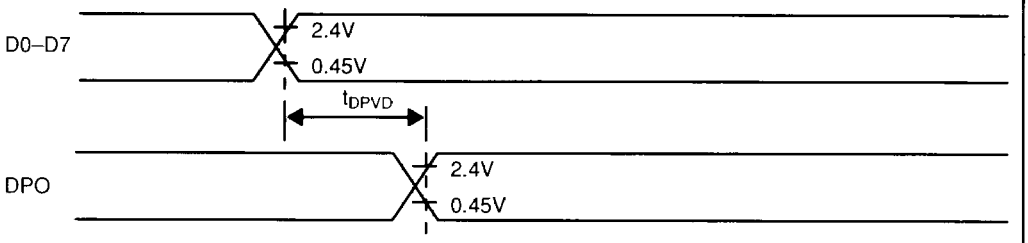
Register Write Timing



AC CHARACTERISTICS (Continued)

DPO (Data Parity Output)						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
DPO Valid Time (from D7–D0 to DPO (Valid)	t_{DPVD}	CL = 30 pF			60	ns

DPO Output Timing



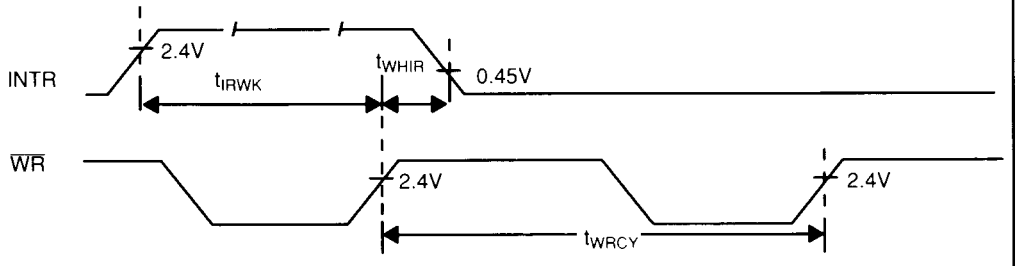
AC CHARACTERISTICS (Continued)

INTR (Interrupt Request) Output

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$\overline{WR}$ Service Time (from INTR High to $\overline{WR}$ High)	t_{IRWL}		0			ns
INTR Release Time (from $\overline{WR}$ High to INTER Low)	t_{WHIR}	CL = 10pf	t_{CLF}		$2t_{CLF}$ +100	ns
INTR Reset Cycle Time[1]	t_{WRCY}		$4t_{CLF}$			ns

Note: 1 Applicable only when interrupt reset is executed.

INTR Output Timing



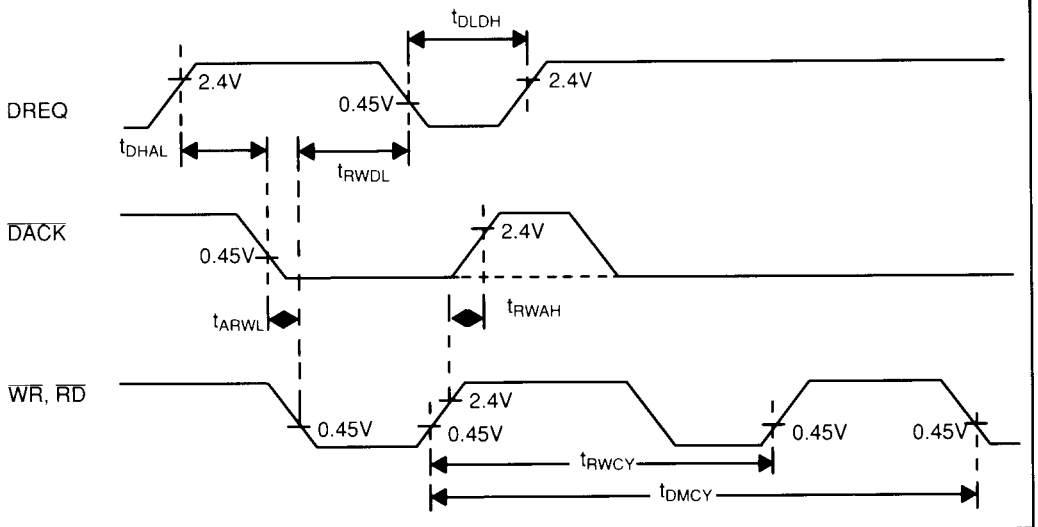
AC CHARACTERISTICS (Continued)

DMA Access

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
DACK Service Time (from DREQ High to $\overline{DACK}$ Low)	t_{DHAL}		0			ns
$\overline{WR}$[1] and $\overline{RD}$ Service Time (from $\overline{DACK}$ Low to $\overline{WR}$ or $\overline{RD}$ Low)	t_{ARWL}		40			ns
DREQ Release Time (from $\overline{WR}$[1] or $\overline{RD}$ Low to DREQ Low)	t_{RWDL}	CL = 30 pF	35		150	ns
$\overline{DACK}$ Hold Time (from $\overline{WR}$[1] or $\overline{RD}$ High to $\overline{DACK}$ High)	t_{RWAH}		10			ns
DREQ Interval (from DREQ Low to DREQ High)	t_{DLDH}		0			ns
DREG Access Cycle Time (1)	t_{RWCY}		$2t_{CLF}$			ns
DREG Access Cycle Time (2)	t_{DMCY}		$3t_{CLF}$			ns

Note: 1 The $\overline{WR}$ parameter is applicable when data buffer register will be full; the $\overline{RD}$ parameter is applicable when the data buffer register will be empty.

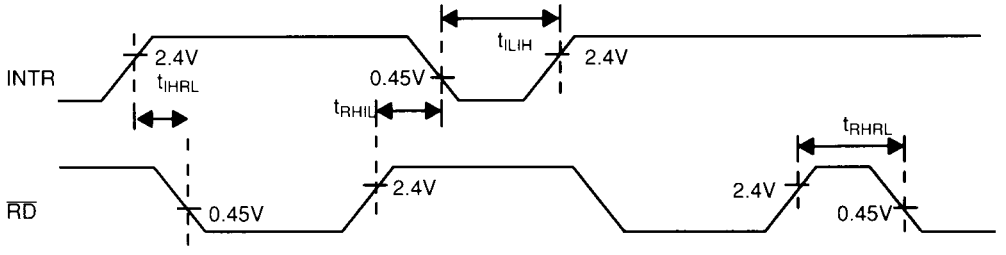
DMA Access Timing



AC CHARACTERISTICS (Continued)

DREG Access – Program Transfer with INTR (Input Operation)						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$\overline{RD}$ Service Time (From INTR High to $\overline{RD}$ Low)	t_{IHRL}		0			ns
INTR Release Time (From $\overline{RD}$ High to INTR Low)	t_{RHIL}	CL = 20pF	35		150	ns
INTR Recovery Time (From INTR Low to INTR High)	t_{ILIH}		0			ns
$\overline{RD}$ Recovery Time (From $\overline{RD}$ High to $\overline{RD}$ Low)	t_{RHRL}		50			ns

DREG Access – Input

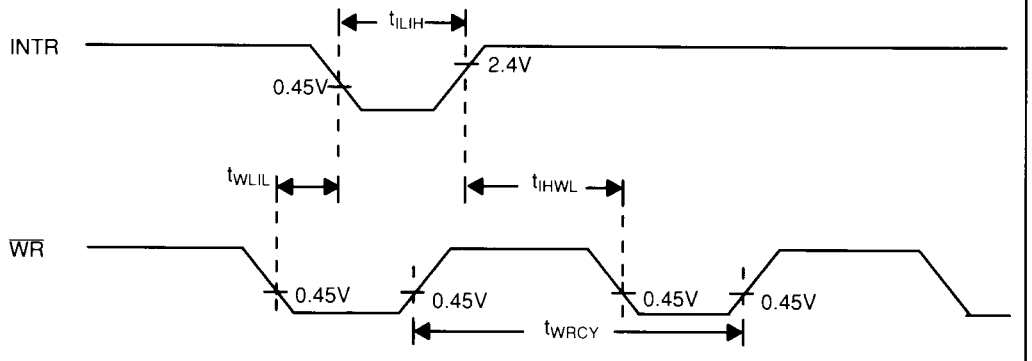


AC CHARACTERISTICS (Continued)

DREG Access – Program Transfer with INTR (Output Operation)

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$\overline{WR}$ Service Time (from INTR High to $\overline{WR}$ Low)	t_{IHWL}		0			ns
INTR Release Time (from $\overline{WR}$ Low to INTR Low)	t_{WLIL}	CL = 20pF	35		150	ns
INTR Recovery Time (from INTR Low to INTR High)	t_{ILIH}		0			ns
$\overline{WR}$ Cycle Time	t_{WRCY}		$2t_{CLF}$			ns

DREG Access – Output



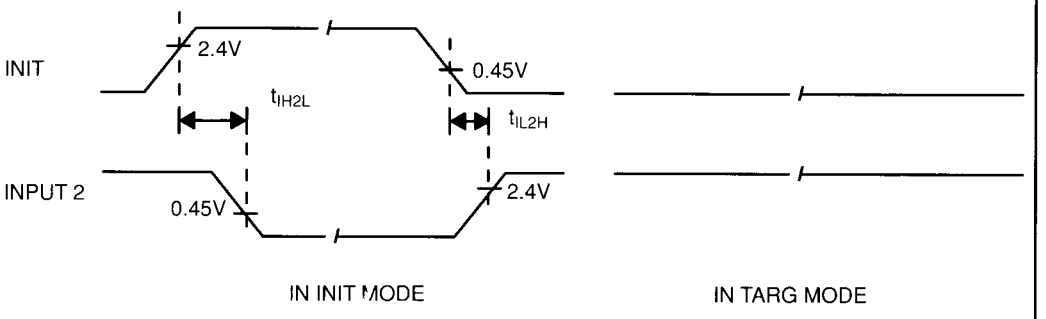
AC CHARACTERISTICS (Continued)

INIT/TARG and INPUT1/INPUT2 Output						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
INPUT2 Valid Time (From INIT High to INPUT2 Low)	t_{IH2L}	CL = 30pF	0		20	ns
INPUT2 Invalid Time (From INIT Low to INPUT2 High)	t_{IL2H}	CL = 30pF	–20		20	ns
INPUT1 Valid Time (From TARG High to INPUT1 Low)	t_{TH1L}	CL = 40pF	0		20	ns
INPUT1 Invalid Time (From TARG Low to INPU12 High)	t_{TL1H}	CL = 40pF	–20		20	ns

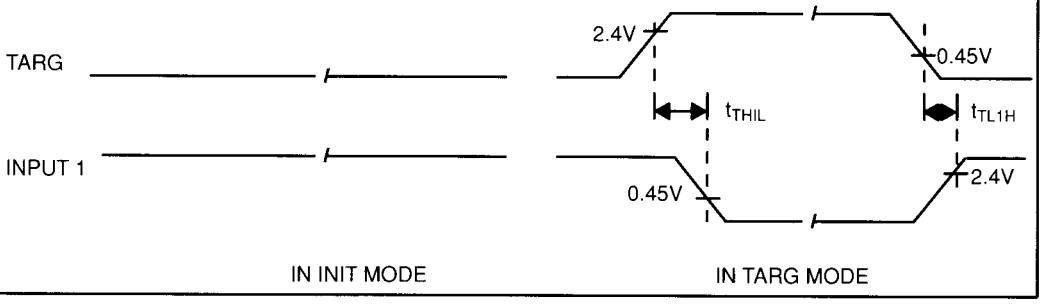
AC CHARACTERISTICS (Continued)

INIT/TARG and INPUT1/INPUT2 Output Timing

INIT and INPUT2 Output Timing:



TARG and INPUT1 Output Timing:



AC CHARACTERISTICS (Continued)

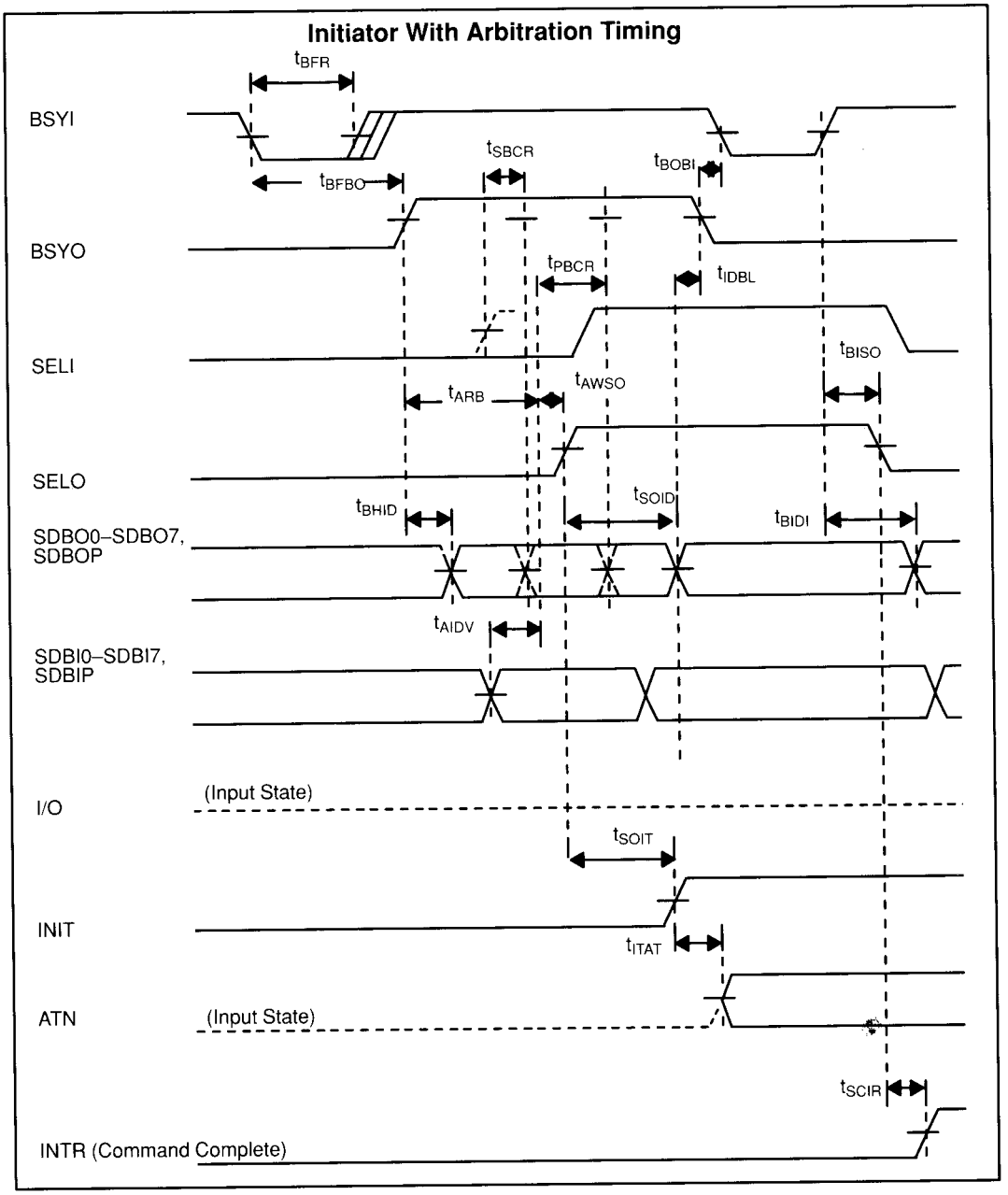
SCSI Bus Interface – Selection Phase Timing

Initiator with Arbitration

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
Bus Free Time[2]	t_{BFR}		$4t_{CLF}+50$			ns
From BSYI Low to BSYO High	t_{BFBO}	CL = 10pF	(6 + n) x t_{CLF}[1]		(7 + n) x $t_{CLF}+60$	ns
From BSYO High to Device ID Out	t_{BHID}	CL = 30pF	0		60	ns
From BSYO High to Prioritize	t_{ARB}		$32t_{CLF}-60$			ns
From Data Bus Valid to Prioritize	t_{AIDV}		100			ns
From Bus Usage Permission Granted SELO High	t_{AWSO}	CL = 10pF	0		50	ns
From SELO High to SELECT ID Output	t_{SOID}	CL = 30pF	$11t_{CLF}-30$			ns
From SELO High to INIT High	t_{SOIT}	CL = 10pF	$11t_{CLF}$			ns
From INIT High to ANT High	t_{ITAT}	CL = 10pF	0		60	ns
From SELECT ID Output to BSYO Low	t_{IDBL}	CL = 10pF	$2t_{CLF}-80$			ns
From BSYO Low to BSYI Low	t_{BOBI}	CL = 10pF	0			ns
From BSYI High to BSYO Low	t_{BISO}	CL = 10pF	$2t_{CLF}$		$3t_{CLF}+60$	ns
From BSYI High to SELO Low	t_{BIDH}	CL = 10pF	$2t_{CLF}$			ns
From SELO Low to INTR High	t_{SCIR}	CL = 30pF			60	ns
From SELI High to BSYO Low, ID Bit Low	t_{SBCR}	CL = 30pF (BSYO) CL = 30pF (SDBO0–SDBO7, SDBOP)			$3t_{CLF}+100$	ns
From Priority Judge to BSYO and ID Bit Low	t_{PBCR}	CL = 30pF (BSYO) CL = 30pF (SDBO0–SDBO7, SDBOP)			80	ns

Notes: 1 n = value of TCL register.
2 The bus free time is the minimum time interval until the booked select command is executed.

AC CHARACTERISTICS (Continued)

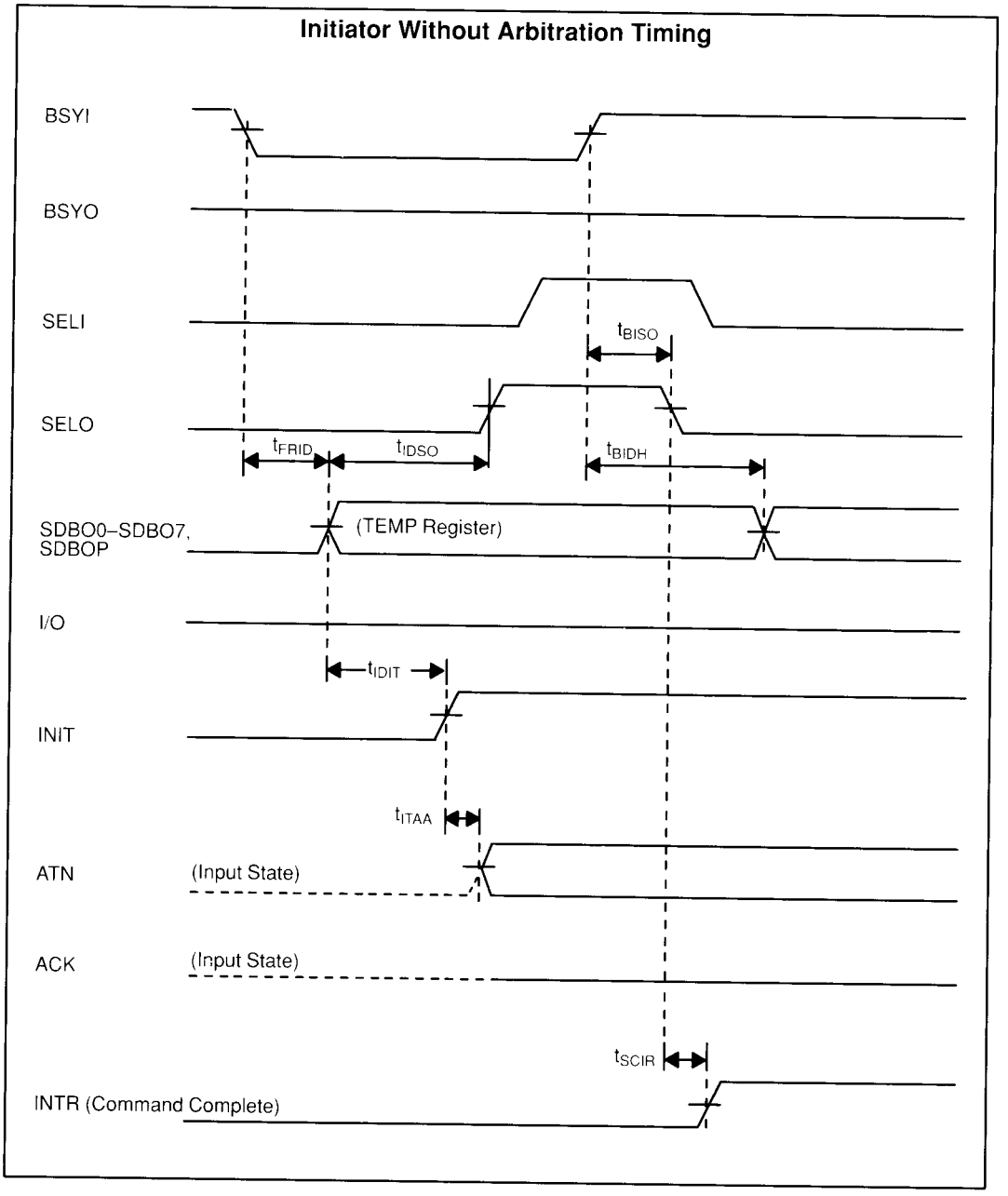


AC CHARACTERISTICS (Continued)

Initiator Without Arbitration						
Parameter	Designator	Test Conditions	Values (Note)			Unit
			Min.	Typ.	Max.	
From BSYI Low to SELECT ID Output	t_{FRID}	CL = 30pF	$(6 + n)^1 \times t_{CLF}$		$(7 + n) \times t_{CLF}+60$	ns
From ID Output to SELO High	t_{IDSO}	CL = 10pF	$11t_{CLF}-80$			ns
From ID Output to INIT High	t_{IDIT}	CL = 10pF	$11t_{CLF}-80$			ns
From INIT High to ATN High	t_{ITAA}	CL = 10pF	0		60	ns
From BSYI High to SELO Low	t_{BISO}	CL = 10pF	$2t_{CLF}$			ns
From BSYI High to SELECT ID Hold	t_{BIDh}		$2t_{CLF}$			ns
From SELO Low to INTR High	t_{SCIR}	CL = 30pF			60	ns

Note: 1 n = value of TCL register.

AC CHARACTERISTICS (Continued)

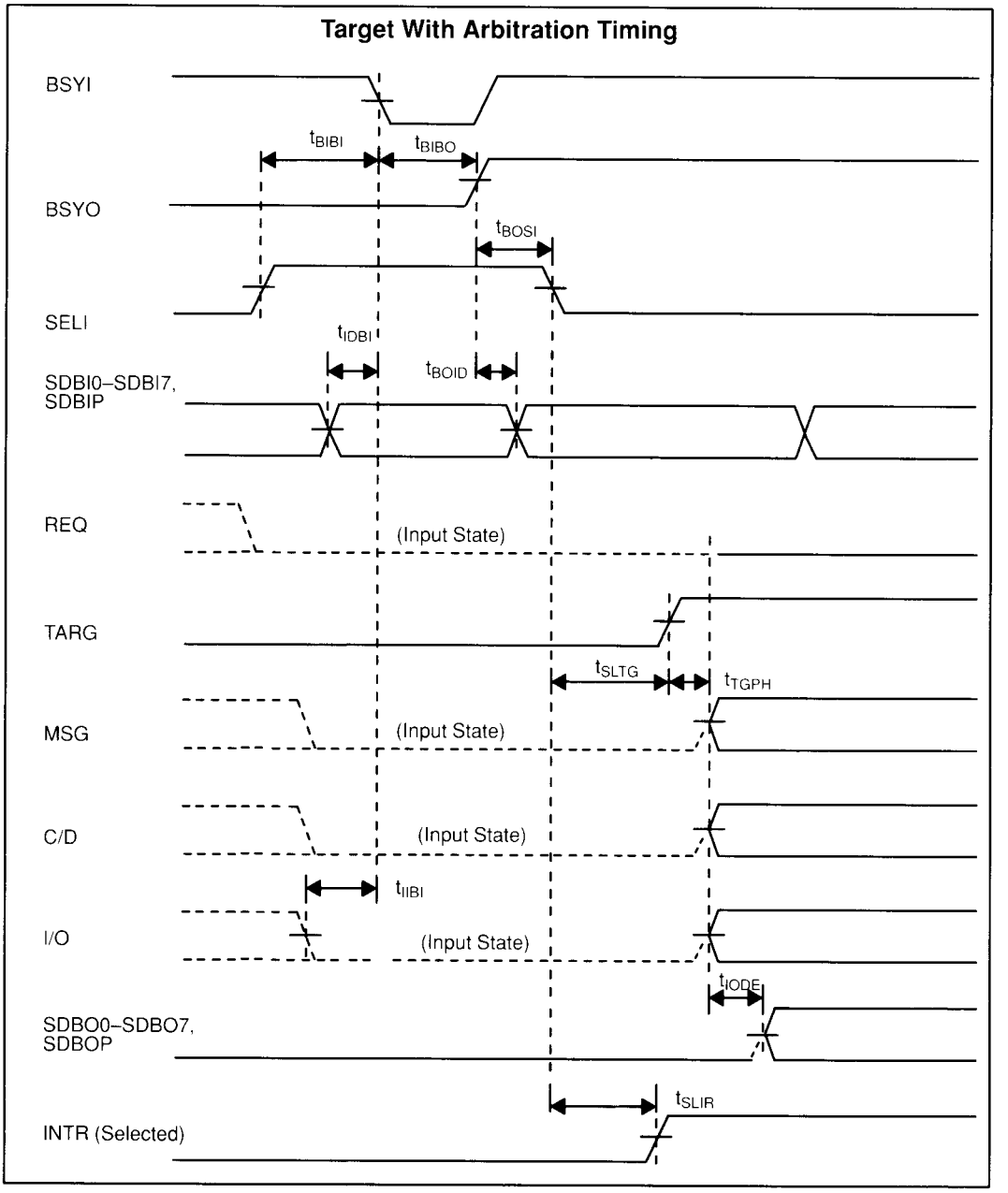


AC CHARACTERISTICS (Continued)

Target With Arbitration

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From SELI High to BSYI Low	t_{SIBI}		0			ns
From Data Bus (ID) Valid to BSYI Low	t_{IDBI}		0			ns
From I/O Low to BSYI Low	t_{IIBI}		0			ns
From BSYI to BSYO High	t_{BIBO}	CL = 30pF	$4t_{CLF}$		$5t_{CLF}+60$	ns
From BSYO High to ID Hold	t_{BOID}		60			ns
From BSYO High to SELI Low	t_{BOSI}		0			ns
From SELI Low to TARG High	t_{SLTG}	CL = 30pF	$3t_{CLF}$		$4t_{CLF}+80$	ns
From TARG High to Phase Signal Output	t_{TGPH}	CL = 10pF	0		50	ns
From I/O High to Data Bus Enable	t_{IODE}	CL = 10pF	$7t_{CLF}$			ns
From SELI Low to INTR High	t_{SLIR}	CL = 30pF			$3t_{CLF}+80$	ns

AC CHARACTERISTICS (Continued)

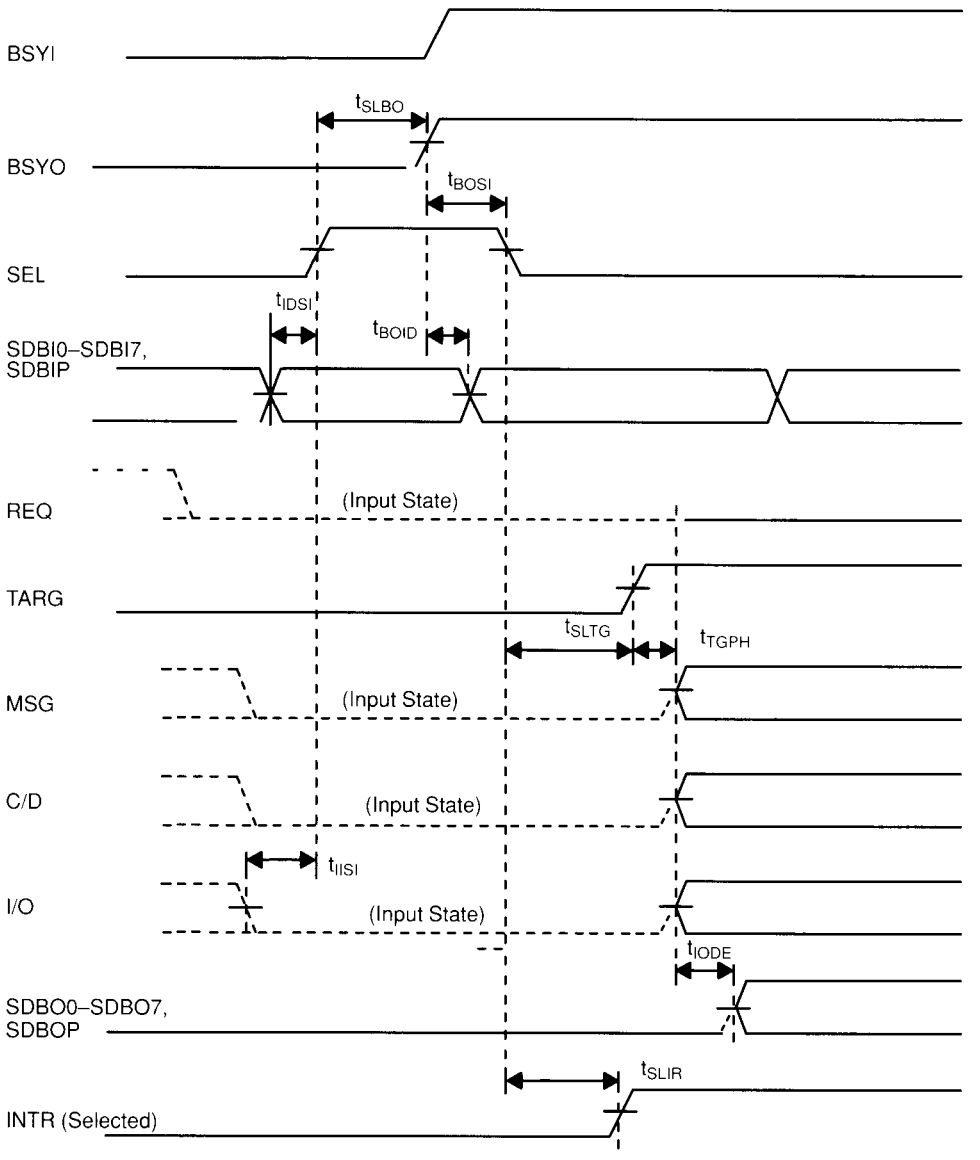


AC CHARACTERISTICS (Continued)

Target Without Arbitration						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From Data Bus (ID) Valid to SELI High	t_{IDSI}		0			ns
From I/O Low to SELI High	t_{IISI}		0			ns
From SELI High to BSYO High	t_{SLBO}	CL = 30pF	$2t_{CLF}$		$3t_{CLF}+50$	ns
From BSYO High to ID Hold	t_{BOID}		60			ns
From BSYO High to SELI Low	t_{BOSI}		0			ns
From SELI Low to TARG High	t_{SLTG}	CL = 30pF	$3t_{CLF}$		$4t_{CLF}+80$	ns
From TARG High to Phase Signal Output	t_{TGPH}	CL = 10pF	0		50	ns
From I/O High to Data Bus Enable	t_{IODE}	CL = 10pF	$7t_{CLF}$			ns
From SELI Low to INTR High	t_{SLIR}	CL = 30pF			$3t_{CLF}+80$	ns

AC CHARACTERISTICS (Continued)

Target Without Arbitration Timing



AC CHARACTERISTICS (Continued)

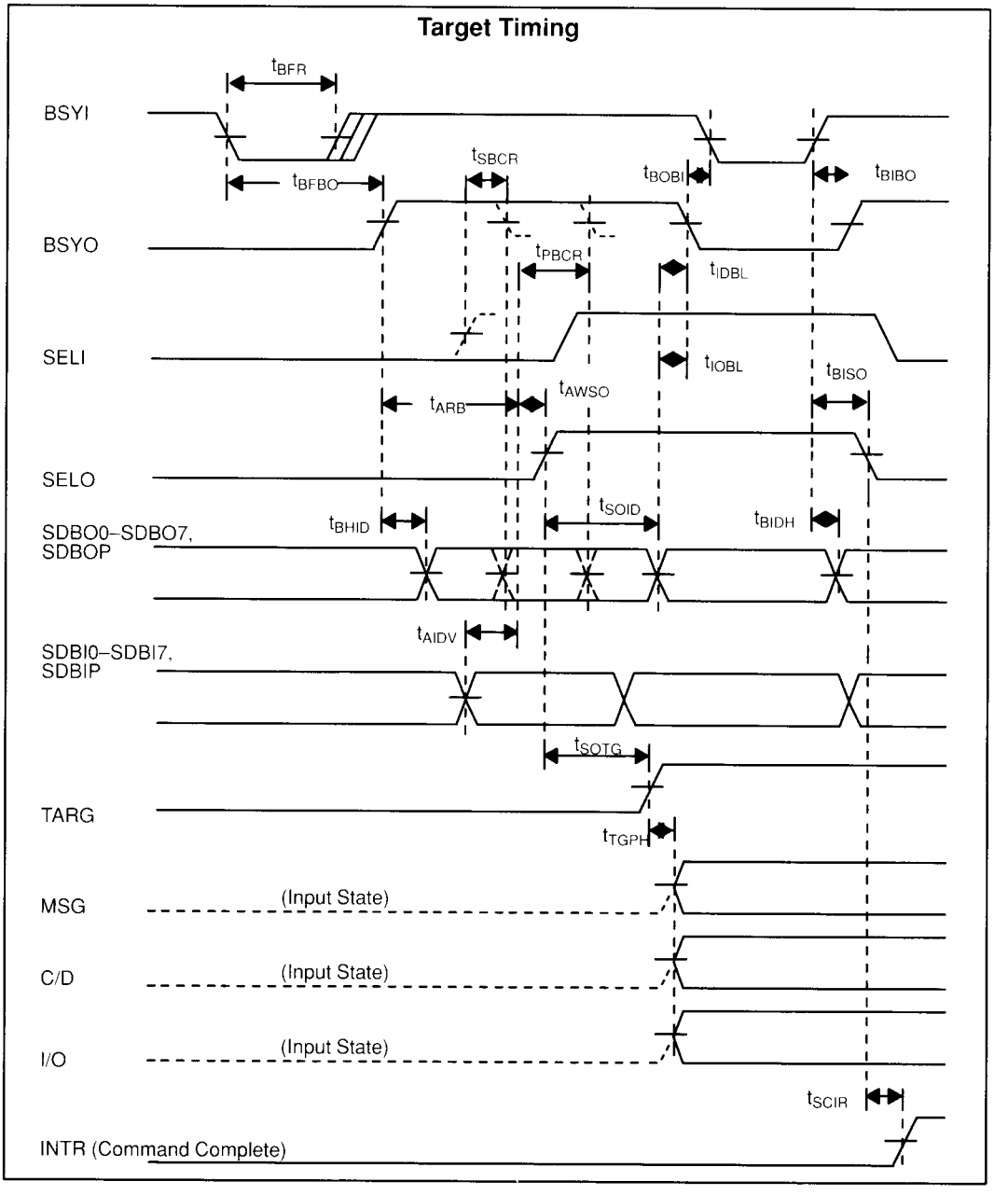
SCSI Bus Interface – Reselection Phase Timing

Target

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
Bus Free time[2]	t_{BFR}					ns
From BSYI Low to BSYO High	t_{BFBO}	CL = 10pF	(6 + n)[1] x t_{CLF}		(7 + n) x t_{CLF}+60	ns
From BSYO High to Device ID Out	t_{BHID}	CL = 30pF	0		60	ns
From BSYO High to Prioritize	t_{ARB}		32t_{CLF}–60			ns
From Data Bus Valid to Prioritize	t_{AIDV}		100			ns
From Bus Usage Permission Granted to SELO High	t_{AWSO}	CL = 10pF	0		50	ns
From SELO High to RESELECT ID Output	t_{SOID}	CL = 30pF	11t_{CLF}–30			ns
From SELO High to TARG High	t_{SOTG}	CL = 10pF	11t_{CLF}–50			ns
From TARG High to Phase Signal Output	t_{TGPH}	CL = 30pF	0		50	ns
From I/O High to BSYO Low	t_{IOBL}	CL = 10pF	2t_{CLF}–80			ns
From RESELECT ID Output to BSYO Low	t_{IDBL}	CL = 10pF	2t_{CLF}–80			ns
From BSYO Low to BSYI Low	t_{BOBI}	CL = 10pF	0		t_{CLF}	ns
From BSYI High to SELO Low	t_{BISO}	CL = 10pF	3t_{CLF}			ns
From BSYI High to RESELECT ID Hold	t_{BIDh}	CL = 10pF	2t_{CLF}			ns
From SELO Low to INTR High	t_{SCIR}	CL = 30pF			80	ns
From SELI High to BSYO and ID Bit Low	t_{SBCR}	CL = 30pF (BSYO) CL = 30pF (SDBO0–SDBO7 SDBOP)			3t_{CLF}+80	ns
From Prioritize to BSYO and ID Bit Low	t_{PBCR}	CL = 30pF (BSYO) CL = 30pF (SDBO0–SDBO7, SDBOP)			60	ns
From BSYI High to BSYI High	t_{BIBO}	CL = 10pF	2t_{CLF}+20		3t_{CLF}+60	ns

Notes: [1]n = value of TCL register.
[2]The bus free time is the minimum time interval until the booked select command is executed.

AC CHARACTERISTICS (Continued)

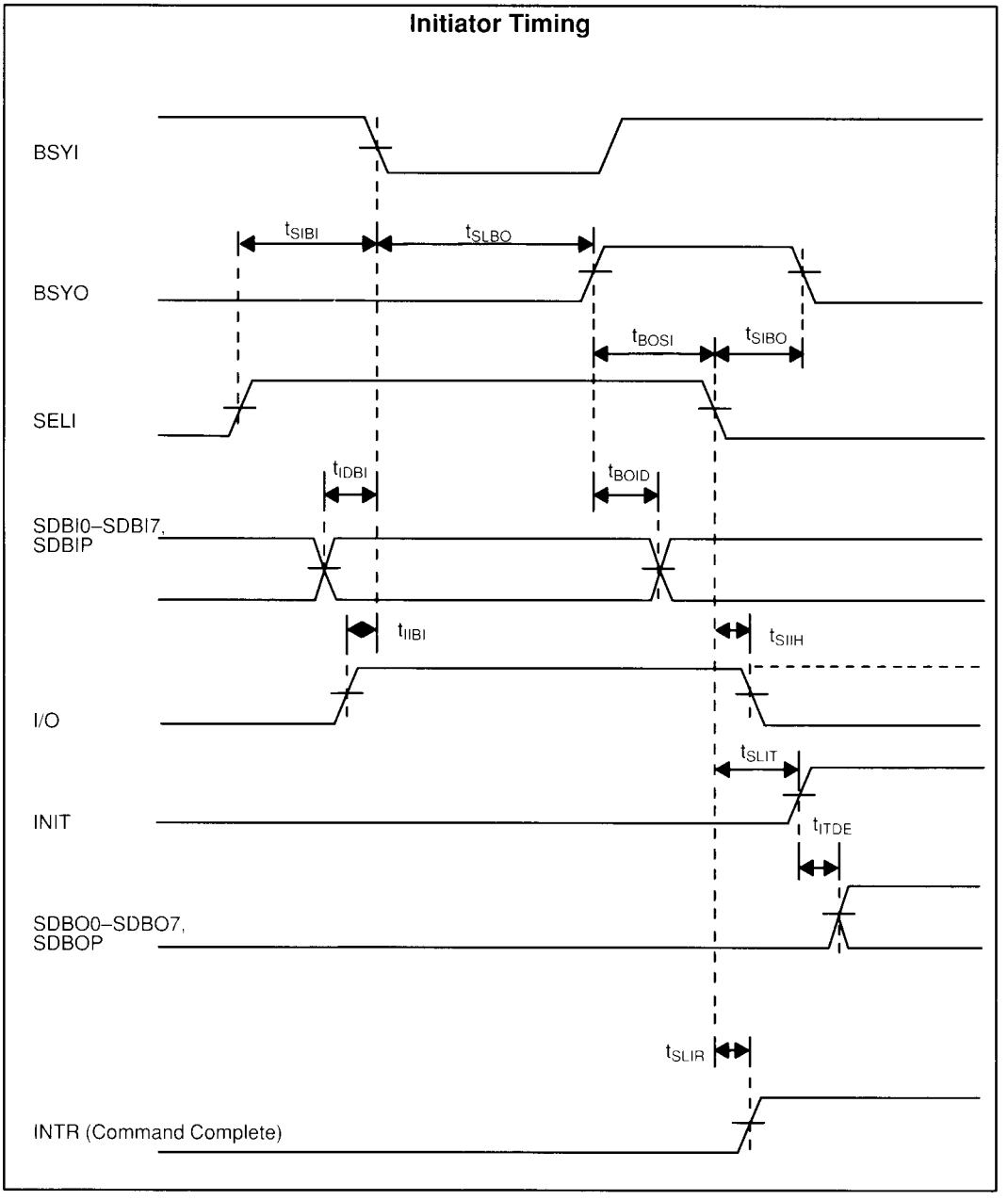


AC CHARACTERISTICS (Continued)

Initiator

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From SELI High to BSYI Low	t_{SIBI}		0			ns
From Data Bus (ID) Valid to BSYI Low	t_{IDBI}		0			ns
From I/O High to BSYI Low	t_{IIBI}		0			ns
From BSYI Low to BSYO High	t_{SLBO}	CL = 30pF	$4t_{CLF}$		$5t_{CLF+60}$	ns
From BSYO High to ID Hold	t_{BOID}		60			ns
From BSYO High to SELI Low	t_{BOSI}		0			ns
From SELI Low to BSYO Low	t_{SIBO}	CL = 30pF	$2t_{CLF}$		$3t_{CLF+60}$	ns
From SELI Low to I/O Hold	t_{SIIH}		100			ns
From SELI Low to INTR High	t_{SLIR}	CL = 30pF			$3t_{CLF+80}$	ns
From SELI Low to INIT High	t_{SLIT}	CL = 30pF	$3t_{CLF}+30$		$4t_{CLF+80}$	ns
From INIT High to Data Bus Enable when I/O is Low	t_{ITDE}	CL = 10pF			50	ns

AC CHARACTERISTICS (Continued)



AC CHARACTERISTICS (Continued)

SCSI Bus Interface – Transfer Phase Timing

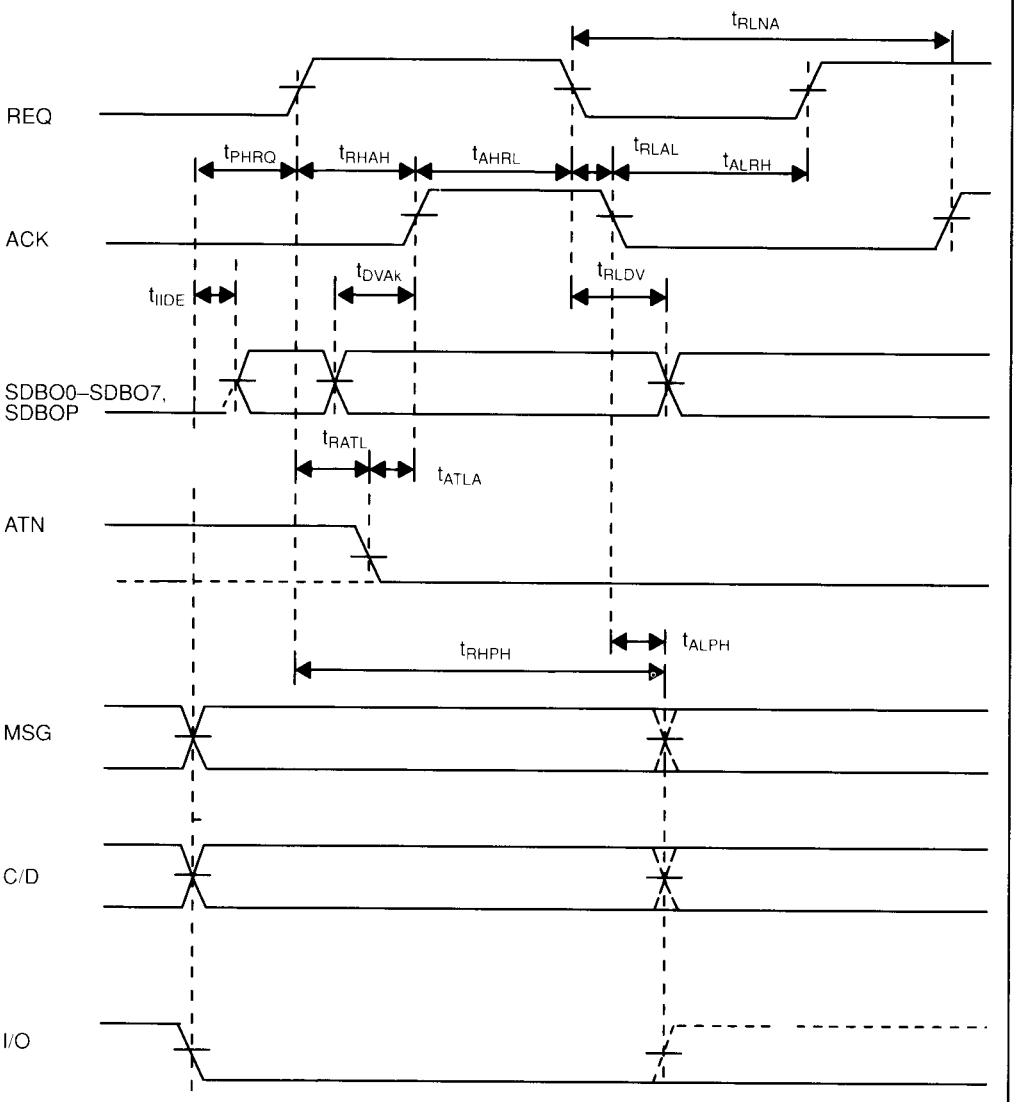
Asynchronous Transfer Output (Initiator)

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From I/O Low to Data Bus Enable	t_{IIDE}	CL = 10pF	10			ns
From Phase Specify to REQ High	t_{PHRQ}		100			ns
From ACK Low to Phase Change	t_{ALPH}[1]	CL = 10pF	10			ns
From REQ High to ATN Low	t_{RATL}[2]	CL = 10pF	$2t_{CLF}$			ns
From ATN Low to ACK High	t_{ATLA}[2]	CL = 10pF	t_{CLF}–20			ns
From Data Bus Valid to ACK High	t_{DVAK}	CL = 10pF	$2t_{CLF}$–80			ns
From REQ Low to Data Bus Hold	t_{RLDV}	CL = 10pF	15			ns
From REQ High to ACK High	t_{RHAH}	CL = 10pF	20			ns
From ACK High to REQ Low	t_{AHRL}		0			ns
From REQ Low to ACK Low	t_{RLAl}	CL = 10pF	10			ns
From ACK Low to REQ High	t_{ALRH}		10			ns
From REQ Low to ACK High	t_{RLNA}	CL = 10pF	$2t_{CLF}$			ns
From REQ High to Phase Change	t_{RHPH}[1]		$3t_{CLF}$			ns

Notes: 1 Phase change must satisfy both t_{ALPH} and t_{RHPH} specifications.
2 This specification is applicable only when the last byte of the message transfer phase is transferred using the hardware transfer mode.

AC CHARACTERISTICS (Continued)

Asynchronous Transfer Output (Initiator) Timing

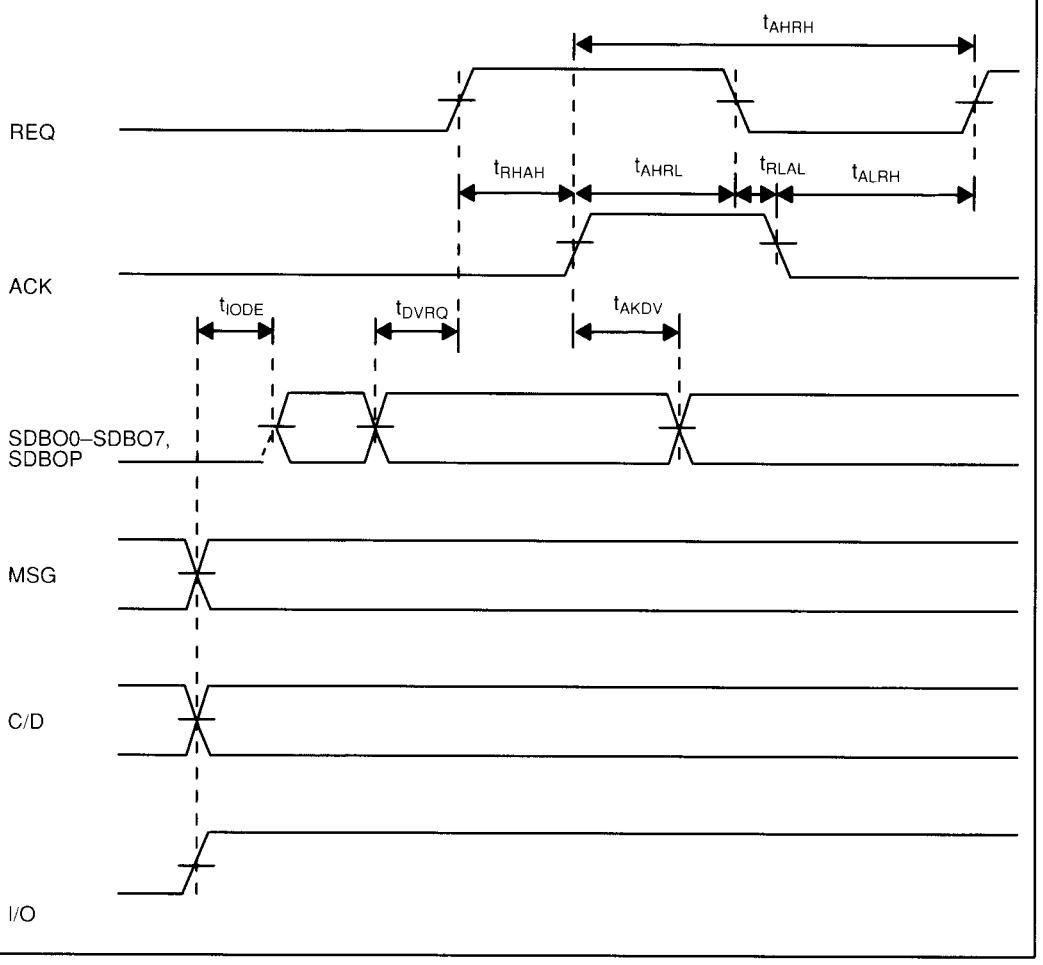


AC CHARACTERISTICS (Continued)

Asynchronous Transfer Output (Target)						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From I/O High to Data Bus Enable	t_{IODE}	CL = 10pF	$7t_{CLF}$			ns
From Data Bus Valid to REQ High	t_{DVPQ}	CL = 10pF	$2t_{CLF}$–80			ns
From ACK High to Data Bus Hold	t_{AKDV}	CL = 10pF	15			ns
From REQ High to ACK High	t_{RHAH}		20			ns
From ACK High to REQ Low	t_{AHRL}	CL = 30pF	10		100	ns
From REQ Low to ACK Low	t_{RLAL}		0			ns
From ACK Low to REQ High	t_{ALRH}	CL = 10pF	10			ns
From ACK High to REQ High	t_{AHRH}	CL = 10pF	$2t_{CLF}$			ns

AC CHARACTERISTICS (Continued)

Asynchronous Transfer Output (Target) Timing

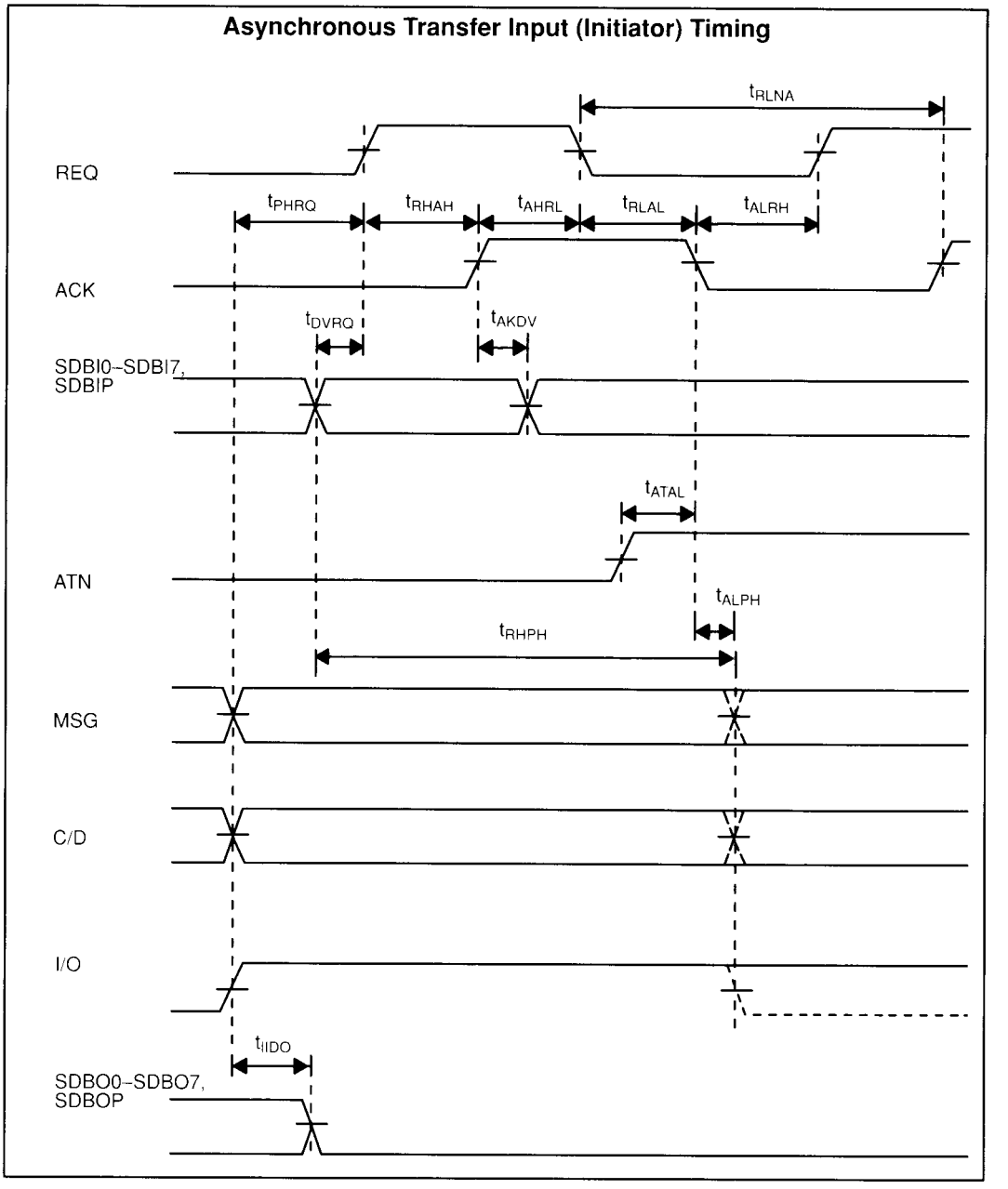


AC CHARACTERISTICS (Continued)

Asynchronous Transfer Input (Initiator)						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From I/O High to Data Bus Disable	t_{IIDD}	CL = 30pF			60	ns
From Phase Specify to REQ High	t_{PHRQ}		100			ns
From ACK Low to Phase Change	t_{ALPH}[1]		10			ns
From Data Bus Valid to REQ High	t_{DVRQ}		10			ns
From ACK High to Data Bus Hold	t_{AKDV}		15			ns
From REQ High to ACK High	t_{RHAH}	CL = 10pF	20			ns
From ACK High to REQ Low	t_{AHRL}		0			ns
From REQ Low to ACK Low	t_{RLAL}	CL = 10pF	20			ns
From ACK Low to REQ High	t_{ALRH}		10			ns
From REQ Low to ACK High	t_{RLNA}	CL = 10pF	t_{CLF}			ns
From ATN High to ACK Low	t_{ATAL}[2]	CL = 10pF	t_{CLF}–20			ns
From REQ High to Phase Change	t_{RHPH}[1]		$3t_{CLF}$			ns

Notes: 1 Phase change must satisfy both t_{ALPH} and t_{RHPH} specifications.
2 Based on this timing parameter, the ATN signal is transferred only when parity check function is enabled and a parity error is detected on the input data.

AC CHARACTERISTICS (Continued)

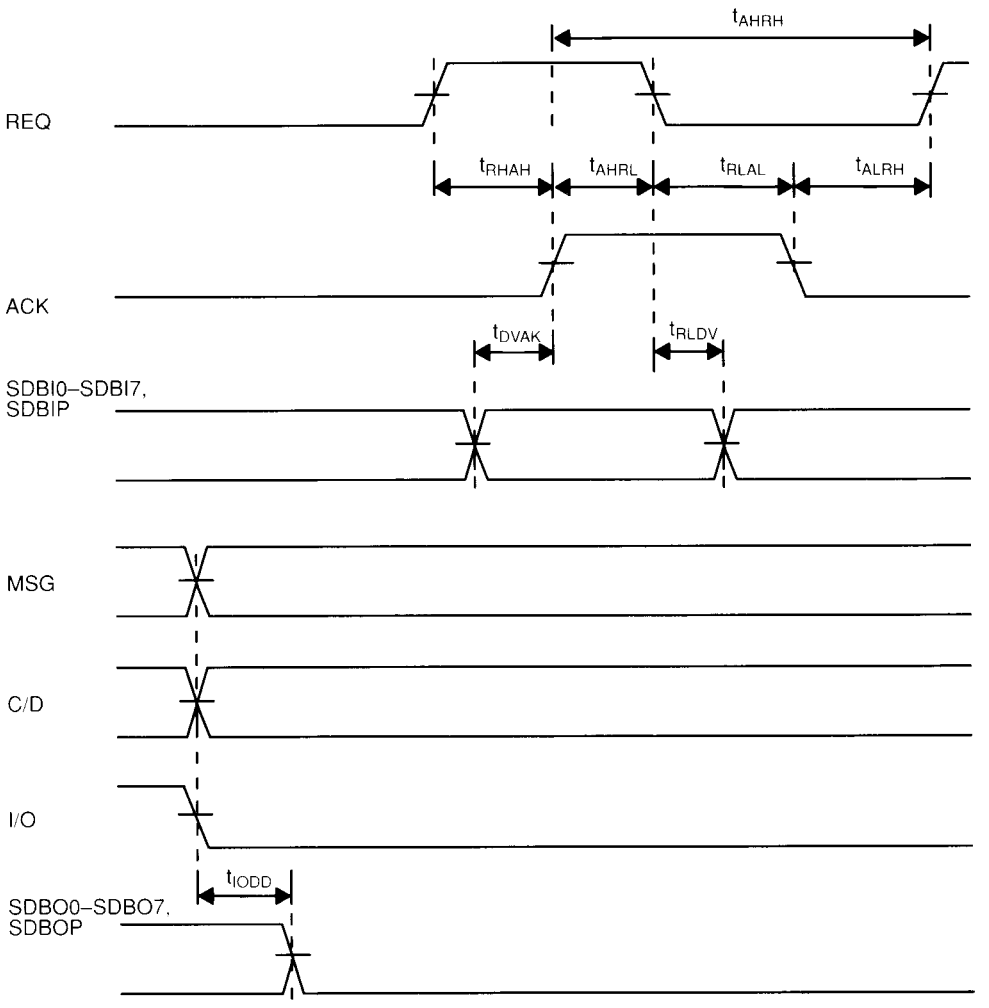


AC CHARACTERISTICS (Continued)

Asynchronous Transfer Input (Target)						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From I/O Low to Data Bus Disable	t_{IODD}	CL = 30pF			30	ns
From Data Bus Valid to ACK High	t_{DVAK}		10			ns
From REQ Low to Data Bus Hold	t_{RLDV}	CL = 10pF	15			ns
From REQ High to ACK High	t_{RHAH}		20			ns
From ACK High to REQ Low	t_{AHRL}	CL = 30pF	10		100	ns
From REQ Low to ACK Low	t_{RLAL}		0			ns
From ACK Low to REQ High	t_{ALRH}	CL = 10pF	10			ns
From ACK High to REQ High	t_{AHRH}	CL = 10pF	$2t_{CLF}$			ns

AC CHARACTERISTICS (Continued)

Asynchronous Transfer Input (Target) Timing

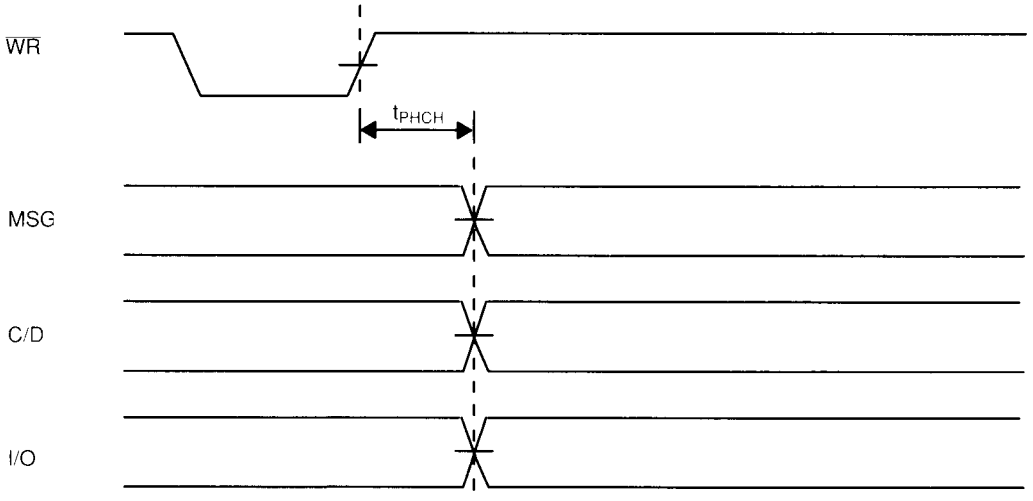


AC CHARACTERISTICS (Continued)

Transfer Phase Change (Target)

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From WR High to MSG, C/D, I/O	t_{PHCH}	CL = 30pF	10		100	ns

Transfer Phase Change (Target) Timing



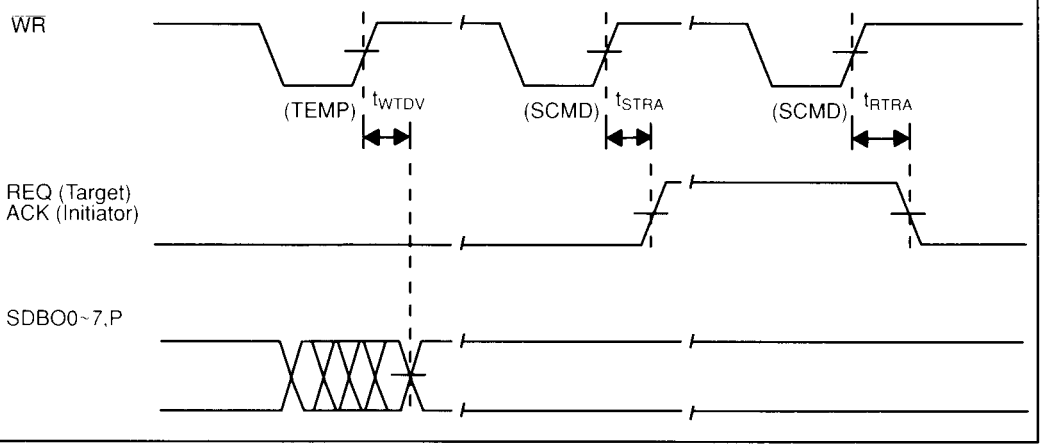
AC CHARACTERISTICS (Continued)

Manual Transfer (Note)[1]

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From $\overline{WR}$ High to Data Bus Valid forTEMP Register	t_{WTDV}	CL = 30pF			100	ns
From $\overline{WR}$ High to REQ High, ACK High for SET ACK/REQ Command	t_{STRA}	CL = 30pF	$2t_{CLF}$		$3t_{CLF}+60$	ns
From $\overline{WR}$ High to REQ Low, ACK Low for RESET ACK/REQ Command	t_{RTRA}	CL = 30pF	$2t_{CLF}$		$3t_{CLF}+60$	ns

Note: 1 Timing sequences not shown are the same as those for asynchronous transfers.

Manual Transfer Timing



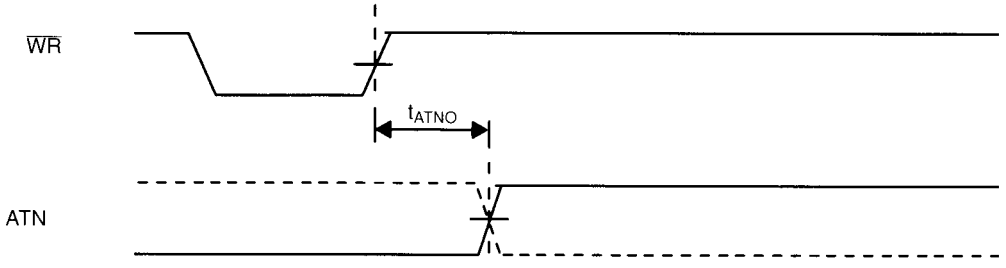
AC CHARACTERISTICS (Continued)

SCSI Bus Interface – Attention Condition

Initiator

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From $\overline{WR}$ high to ATN High, ATN Low for SET/RESET ATN Command	t_{ATNO}	CL = 30pF	$2t_{CLF}$		$3t_{CLF}+60$	ns

Attention Condition (Initiator) Timing



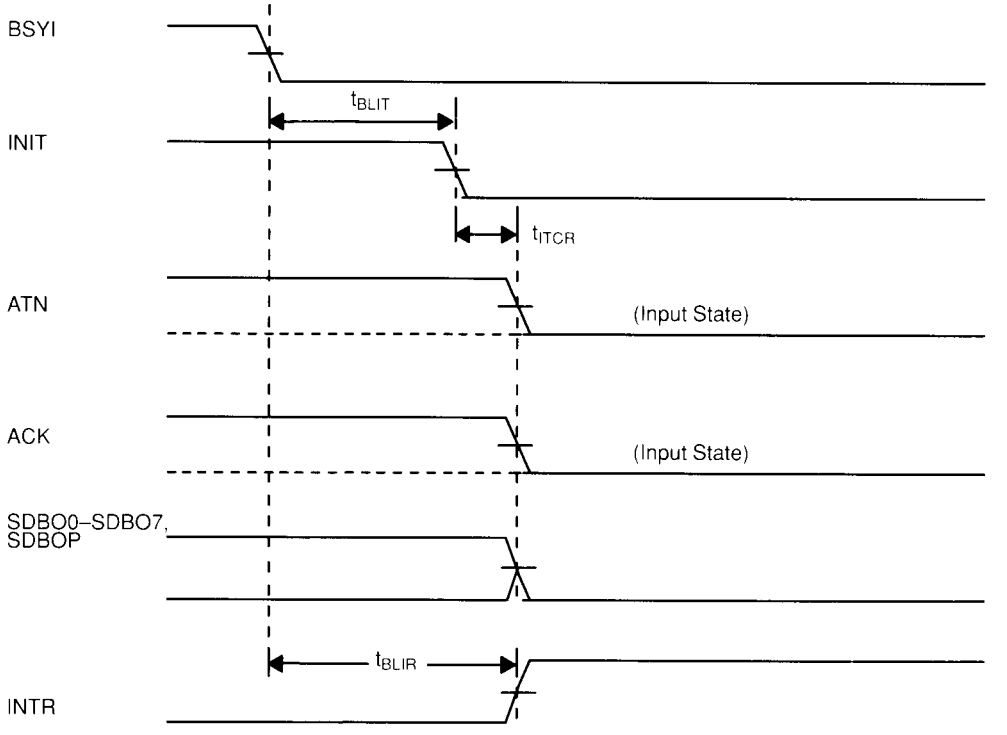
AC CHARACTERISTICS (Continued)

SCSI Bus Interface – Bus Free

Initiator (Disconnected)

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From BSYI Low to INIT Low	t_{BLIT}	CL = 30pF			$5t_{CLF}+60$	ns
From INIT Low to Bus Clear	t_{ITCR}	CL = 30pF			80	ns
From BSYI Low to INTR High	t_{BLIR}	CL = 30pF			$6t_{CLF}+80$	ns

Initiator (Disconnected) Timing

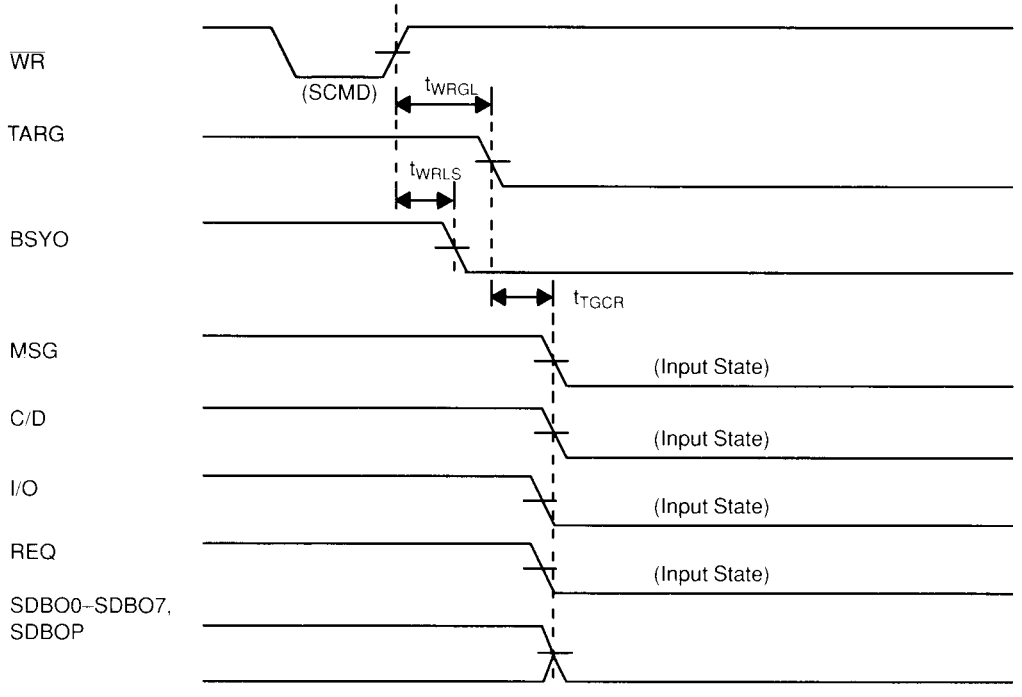


AC CHARACTERISTICS (Continued)

Target (Bus Release Command)

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From $\overline{WR}$ High (SCMD Register) to BSYO Low	t_{WRLS}	CL = 30pF			$3t_{CLF}+60$	ns
From $\overline{WR}$ High (SCMD Register) to TARG Low	t_{WRGL}	CL = 40pF			$3t_{CLF}+60$	ns
From TARG Low to Bus Clear	t_{TGCR}	CL = 30pF			80	ns

Target (Bus Release Command) Timing

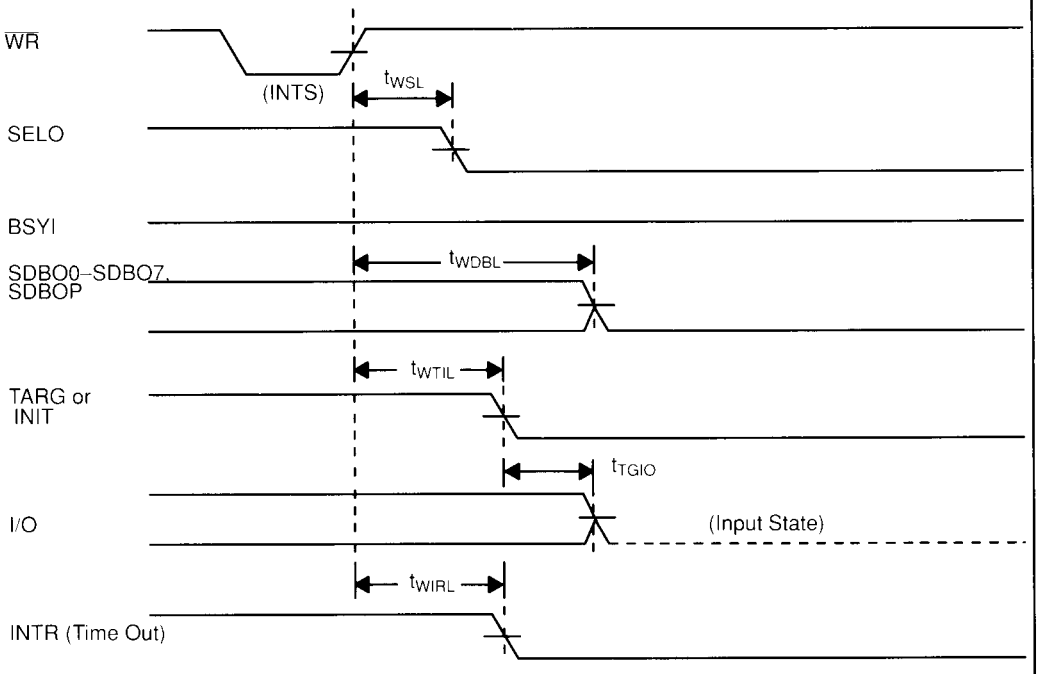


AC CHARACTERISTICS (Continued)

Termination (Time Out) – Selection and Reselection Phases

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From $\overline{WR}$ High (INTS Register) to SELO low	t_{WSL}	CL = 30pF			$3t_{CLF}$+60	ns
From $\overline{WR}$ High (INTS Register) to Data Bus Disable	t_{WDBL}	CL = 30pF			$3t_{CLF}$+100	ns
From $\overline{WR}$ High (INTS Register) to TARG Low or INIT Low	t_{WTIL}	CL = 40pF			$3t_{CLF}$+60	ns
From TARG Low to I/O High-Z	t_{TGIO}	CL = 30pF			50	ns
From $\overline{WR}$ High (INTS Register) to Data Bus Disable	t_{WIRL}	CL = 30pF			$3t_{CLF}$+60	ns

Termination (Time Out) Selection and Reselection Phases Timing



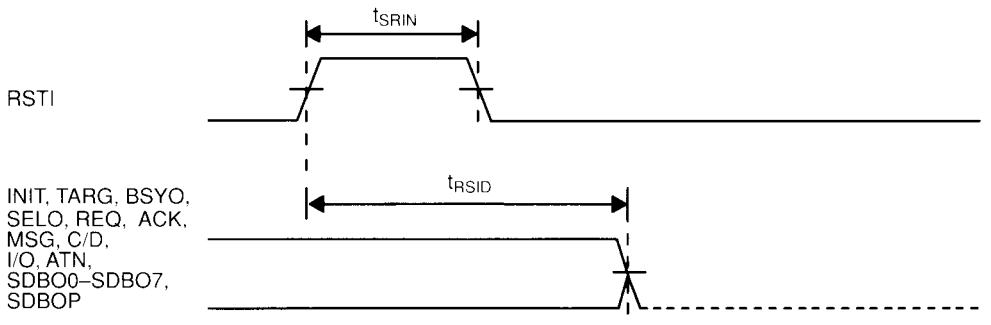
AC CHARACTERISTICS (Continued)

SCSI Bus Interface – Reset Condition

RST INPUT

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
RSTI Pulse Width	t_{SRIN}		$3t_{CLF}$			ns
Reset Delay	t_{RSID}	CL = 30pF			$4t_{CLF}+110$	ns

RSTI Input Timing

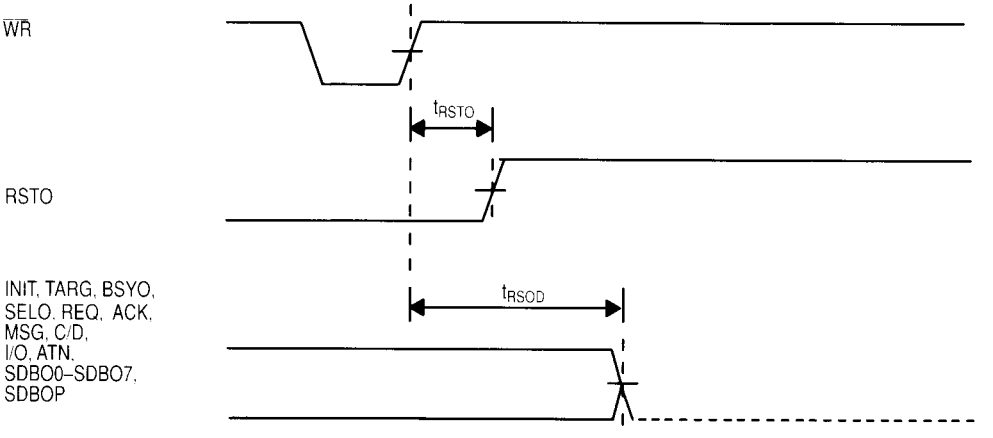


AC CHARACTERISTICS (Continued)

RST Output

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
From $\overline{WR}$ High (SCMD Register's Bit 4) to RSTO High	t_{RSTO}	CL = 30pF	10		80	ns
Reset Delay	t_{RSOD}	CL = 30pF			110	ns

RSTO Output Timing



AC CHARACTERISTICS (Continued)

AC Test Conditions (Input)

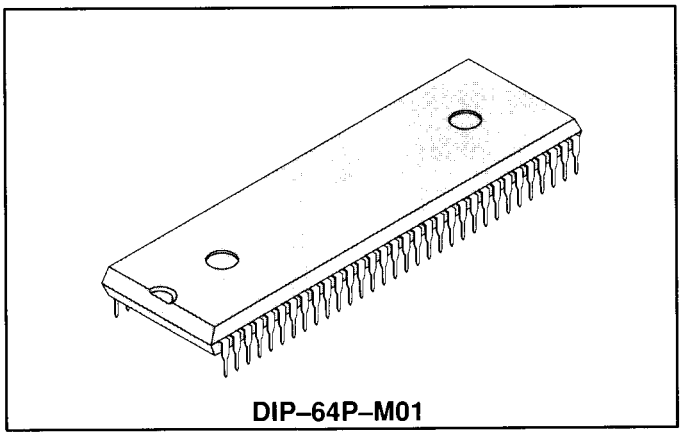
Timing Reference Levels for CPU/DMAC Interface
Logical 1 = 2.4 V_{DC} Logical 0 = 0.45 V_{DC}

AC Test Conditions (Output)

Timing Reference Levels for SCSI Bus Interface
Logical 1 = 2.4 V_{DC} Logical 0 = 0.45 V_{DC}

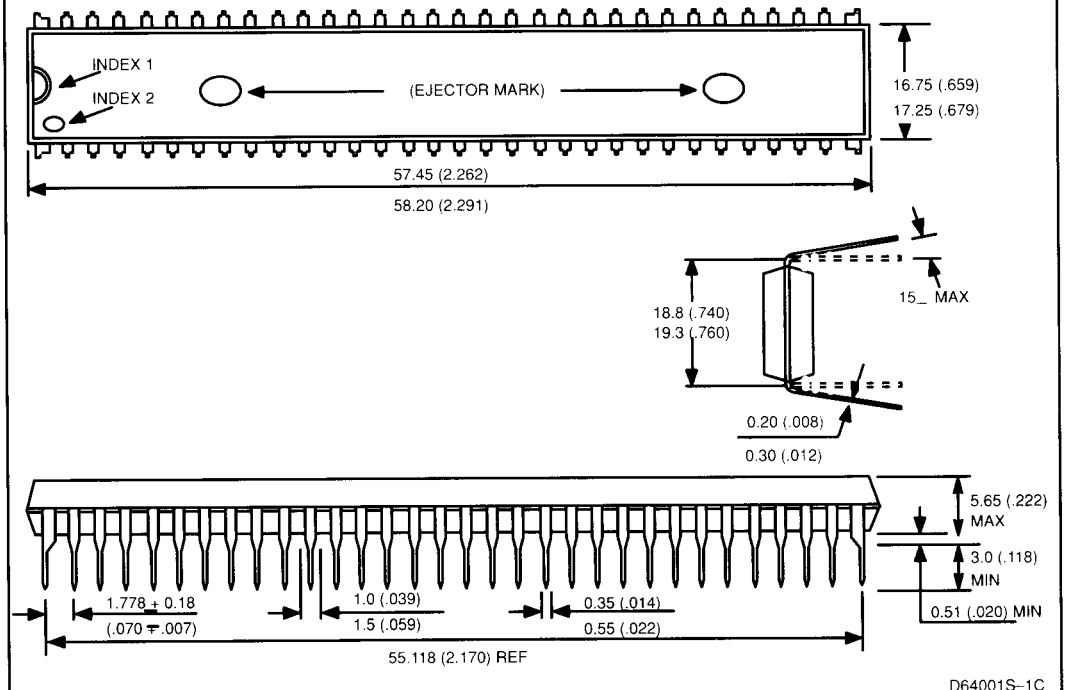
Capacitive Output Loading

Input/Output Pins	Values			Unit
	Min.	Typ.	Max.	
D0 – D7, DP		—	80	pF
DPO		10	30	pF
INTR		10	30	pF
DREQ		10	30	pF
TARG, INPUT1		20	40	pF
INIT, INPUT2		10	30	pF
SDBO0 – SDBO7, SDBOP		10	30	pF
RSTO, SELO, BSYO		10	30	pF
MSG, C/D, I/O		10	30	pF
REQ, ACK, ANT		10	30	pF



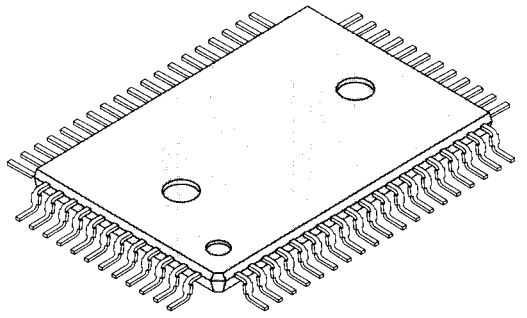
DIP–64P–M01

64–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE NO.: DIP–64P–M01)



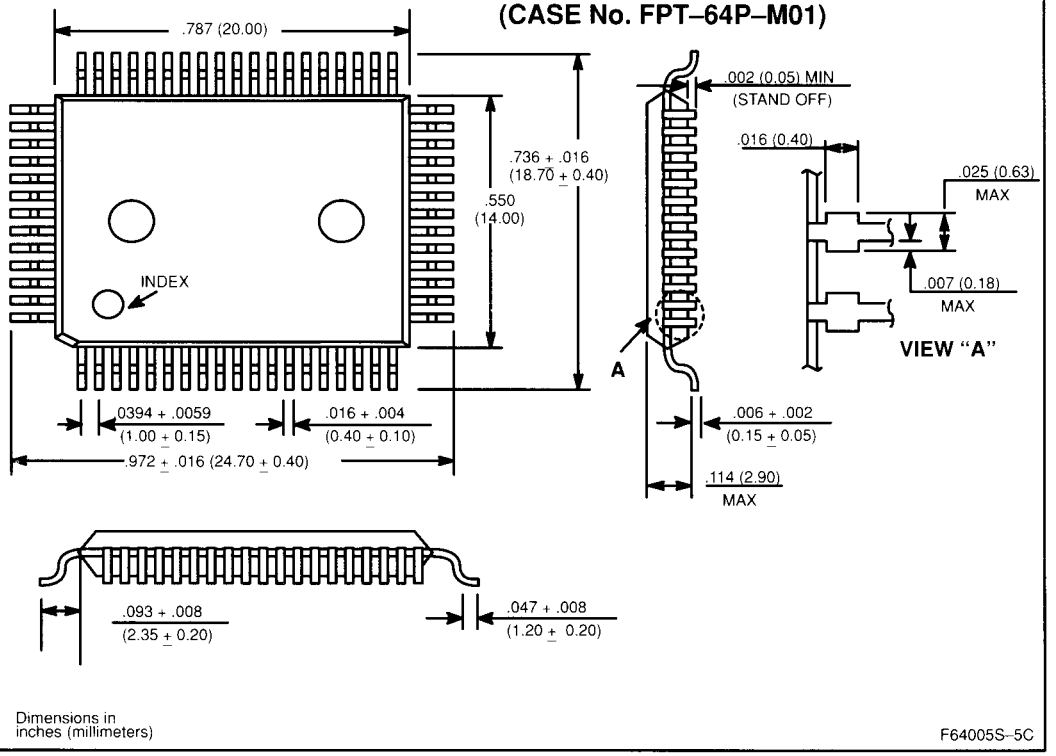
D64001S–1C

Dimensions in
millimeters (inches)



FPT–64P–M01

64–LEAD PLASTIC FLAT PACKAGE (CASE No. FPT–64P–M01)



Dimensions in inches (millimeters)

F64005S–5C