MSM6949

ANALOG FRONT END LSI

www.DataSheet4U.com

GENERAL DESCRIPTION

The MSM6949 is an analog front end LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology. The MSM6949 is used to implement an analog front end function required in the modem set based on CCITT V. 26, V. 27 and V. 29 recommendations.

The MSM6949 performs all basic analog signal processing functions such as transmit and receive filters, selectable amplitude equalizers, transmit signal level attenuator, fast carrier detector, AD and DA converter with 8-bit parallel input/output.

In addition to it, the MSM6949 performs analog loop test, the detection of call progress tones, 75 bps backward channel transmitter and automatic gain control (AGC). AGC circuit is digitally controlled by the digital signal processor which performs the demodulating function.

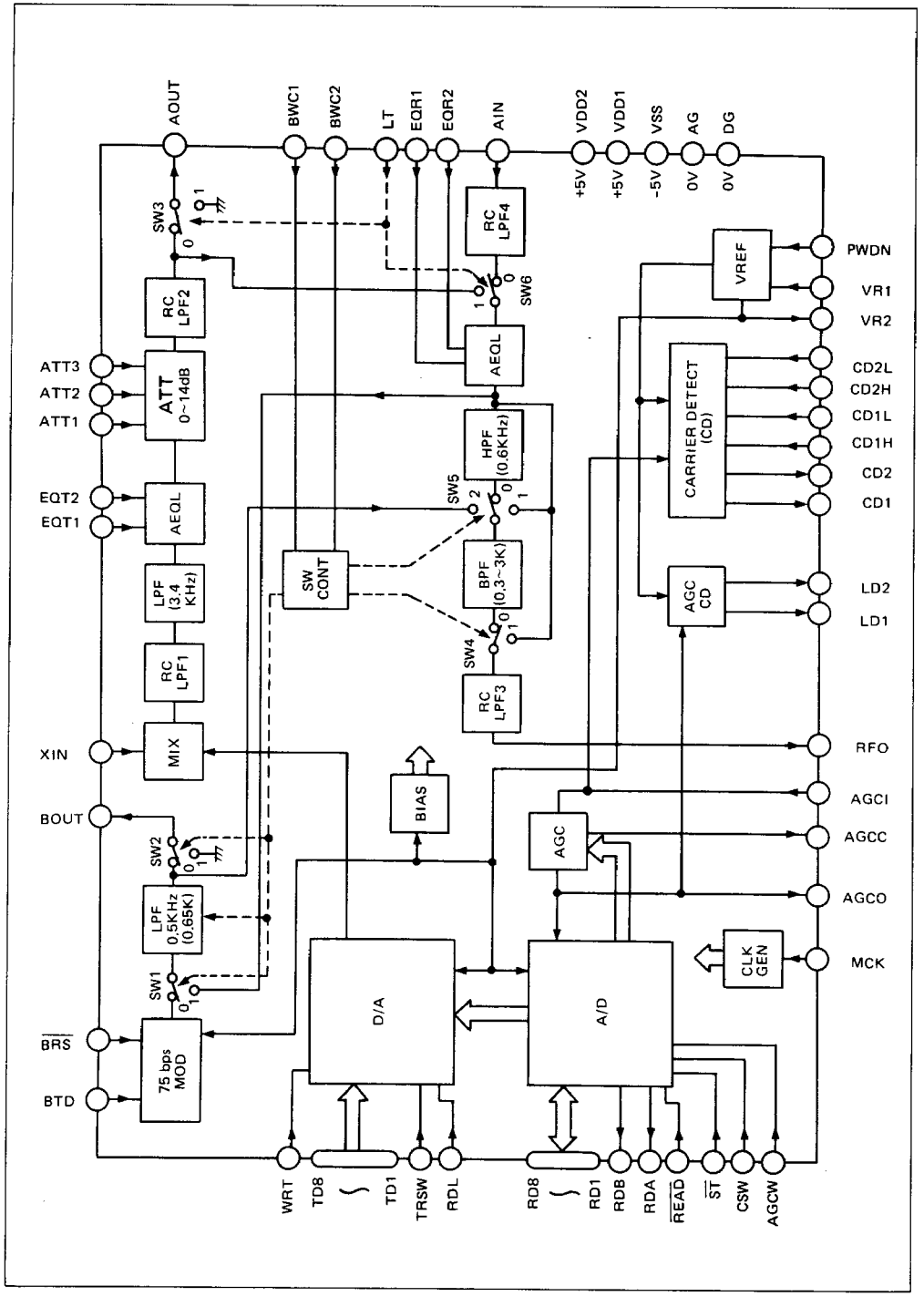
By utilizing the MSM6949 together with OKI's digital signal processors, a cost effective modem can be designed easily.

FEATURES

- Performs all analog signal processing functions required for CCITT V. 26, V. 27 and V. 29.
- 75 bps backward channel FSK transmitter.
- Interfaces to digital signal processors with receive and transmit parallel data bus.
- Call progress tone monitoring.
- An chip AGC circuit controlled by external digital signals, over the received signal level range of 51 dB with 0.2 dB step.
- Analog loop test: A transmitting analog signal can be looped back as a receive analog signal within the chip.
- A set of carrier detection circuits, the on/off levels of which, are fixed at each of the compromised values within the chip, and also can be adjusted by external resistors.
- Two CD circuits are useful for Fall-Back operation and so forth.
- 3.456 MHz external clock for operation.
- On-chip voltage reference.
- Few external components required.
- Supply voltage, ±5V.
- Low power dissipation: 140 mW typical.
- Power stand by mode available.
- 64 pin mini-size DIP. MSM6949SS
  68 pin PLCC. MSM6949JS
  64 pin FLAT MSM6949GS-V1K

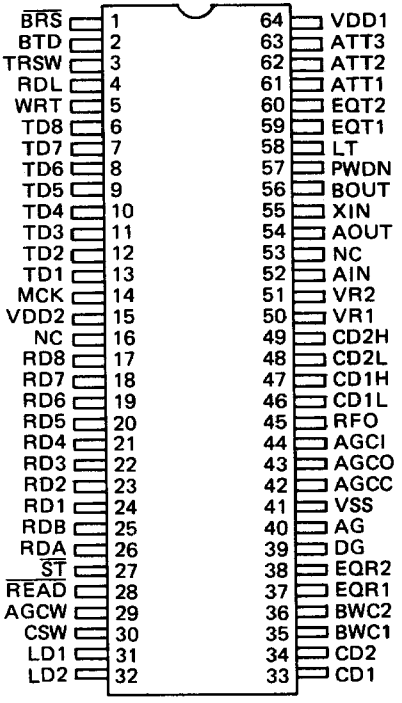
www.DataSheet4U.com

BLOCK DIAGRAM

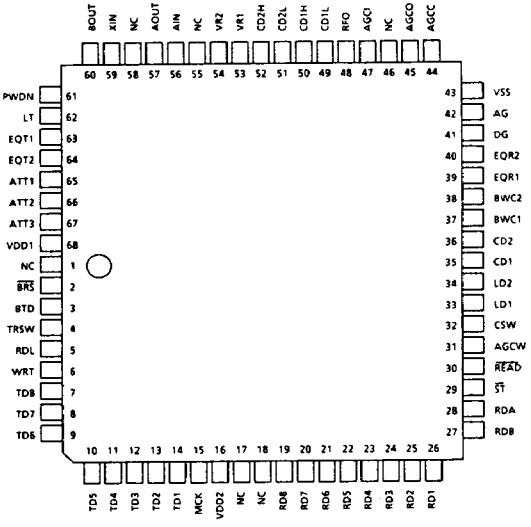


PIN CONFIGURATION (Top View)

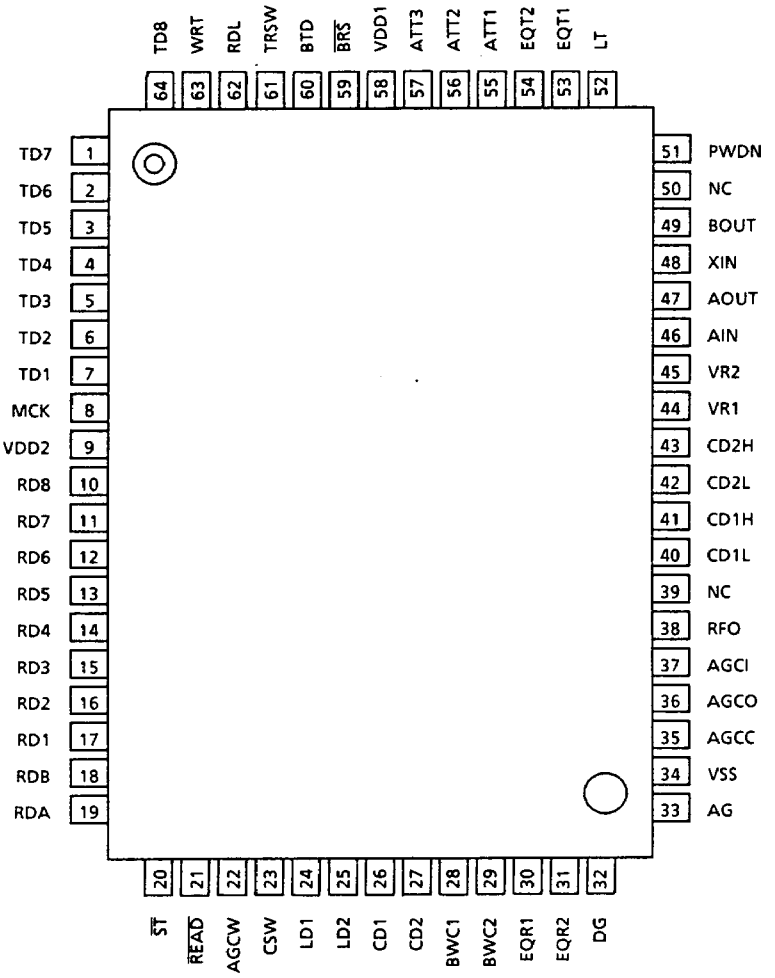
64 pin mini DIP (MSM6949SS)



68 pin PLCC (MSM6949JS)



64 pin FLAT (MSM6949GS-V1K)



PIN ASSIGNMENTS (SS ... 64 pin mini-size DIP, JS ... 68 pin PLCC, GS ... 64 pin FLAT)

Pin Name	Pin No.			Function	
	SS	JS	GS		
$\overline{BRS}$	1	2	59	Request to Send for backward channel (V.23)	
BTD	2	3	60	Transmit Data for backward channel (V.23)	
TRSW	3	4	61	Control signal for connection of DA input bus	
RDL	4	5	62	Latch clock for RD to input to DA within chip	
WRT	5	6	63	Control signal for writing TD to DA	
TD8	6	7	64	Transmit signal digital data bus input to DA	MSB
TD7	7	8	1		–
TD6	8	9	2		–
TD5	9	10	3		–
TD4	10	11	4		–
TD3	11	12	5		–
TD2	12	13	6		–
TD1	13	14	7		LSB
MCK	14	15	8	Master clock input 3.456 MHz	
VDD2	15	16	9	+5V power supply	
RD8	17	19	10	Receive signal digital data bus output from AD (3-state I/O)	MSB
RD7	18	20	11		–
RD6	19	21	12		–
RD5	20	22	13		–
RD4	21	23	14		–
RD3	22	24	15		–
RD2	23	25	16		–
RD1	24	26	17		LSB
RDB	25	27	18	Additional digit for RD bit shifting (3-state output)	
RDA	26	28	19		
$\overline{ST}$	27	29	20	Control signal for starting of AD conversion	
$\overline{READ}$	28	30	21	Control signal for reading RD from AD	
AGCW	29	31	22	Writing clock for setting data to AGC circuit	
CSW	30	32	23	RD bit shifting enable	
LD1	31	33	24	Outputs of level comparators put to AGC circuit's output. These are used to set AGC at typical gain when detecting urgent changes.	
LD2	32	34	25		
CD1	33	35	26	Carrier detect for QAM/PSK signal	
CD2	34	36	27	Carrier detect for FSK signal (T.30)	

Pin Name	Pin No.			Function
	SS	JS	GS	
BWC1	35	37	28	Receive filter bandwidth select
BWC2	36	38	29	
EQR1	37	39	30	Fixed compromise cable amplitude equalization select for receiving
EQR2	38	40	31	
DG	39	41	32	Digital ground (0V)
AG	40	42	33	Analog ground (0V)
VSS	41	43	34	−5V power supply
AGCC	42	44	35	External capacitor terminal for AGC circuit
AGCO	43	45	36	AGC circuit output
AGCI	44	47	37	AGC circuit input connected for RFO through external capacitor
RFO	45	48	38	Receive filter output connected to AGCI through external capacitor
CD1L	46	49	40	Carrier detect level select for CD1
CD1H	47	50	41	
CD2L	48	51	42	Carrier detect level select for CD2
CD2H	49	52	43	
VR1	50	53	44	On-chip reference voltage adjust using external resistors
VR2	51	54	45	
AIN	52	56	46	Receive analog signal input
AOUT	54	57	47	Transmit analog signal output
XIN	55	59	48	External analog signal input
BOUT	56	60	49	75 bps FSK transmit signal output
PWDN	57	61	51	Power down mode select
LT	58	62	52	Analog loop test
EQT1	59	63	53	Fixed compromise cable amplitude equalization select for transmitting
EQT2	60	64	54	
ATT1	61	65	55	8 steps attenuator select for transmit signal level
ATT2	62	66	56	
ATT3	63	67	57	
VDD1	64	68	58	+5V power supply

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit
Power supply voltage	V_{DD}	T_a = 25°C With respect to AG or DG	-0.3 ~ +7	V
	V_{SS}		-7 ~ +0.3	
Analog input voltage	V_{IA}		V_{SS}-0.3 ~ V_{DD}+0.3	
Digital input voltage	V_{ID}		-0.3 ~ V_{DD}+0.3	
Operating temperature	T_{OP}	–	-40 ~ 85	°C
Storage temperature	T_{STG}	–	-55 ~ 150	

2. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	With respect to AG or DG	4.75	5.00	5.25	V
	V_{SS}		-5.25	-5.00	-4.75	
	AG, DG	–	–	0	–	
Operating Temperature	T_{OP}	–	0	–	70	°C
R1	–	Transformer impedance (Hybrid) $\frac{600\Omega}{600\Omega}$: 600Ω	–	600	–	Ω
R2	–		–	600	–	
R3	–		–	300	–	
R4	–	–	–	51	–	kΩ
R5	–		–	51	–	
R6	–		–	51	–	
R7	–		–	51	–	
R8	–		10	33	–	
R9	–		–	36	–	
C1	–	–	–	2.2	–	μF
C2	–		–	1	–	
C3	–		–	0.1	–	
C4	–		–	0.1	–	
C5, C7, C9	–		–	10	–	
C6, C8	–		–	1	–	
R10 ~ R17	–	–	–	10	–	kΩ
Reference Voltage	V_{REF}	Ajusted by External Resistors	–	+2.50	–	V
Master Clock Frequency	f_{MCK}		3.4557	3.456	3.4563	MHz
MCK Duty Cycle	D_{MCK}	50% to 50%	30	50	70	%
Digital Input Rise Time	t_r	RDL, WRT, MCK, $\overline{ST}$, READ, AGCW See Figure 1	0	–	50	ns
Digital Input Fall Time	t_f		0	–	50	ns
$\overline{ST}$ Period	t_{PS}	See Figure 2, 3	51	–	143	μs
$\overline{ST}$ Width	t_{WS}		0.4	–	t_{PS}-0.4	μs
READ Width	t_{WRE}		0.3	–	–	μs

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{ST} \rightarrow \overline{READ}$ Timing	t_{SR}	See Figure 2, 3	51	–	$t_{PS}+50$	μs
$\overline{ST} \rightarrow$ AGCW Timing	t_{SA}		5	–	$t_{PS}-10$	μs
AGCW Width	t_{WA}		0.3	–	$t_{PS}-0.3$	μs
WRT Period	t_{PW}		20	–	143	μs
WRT Width	t_{WW}		0.4	–	$t_{PW}-0.4$	μs
RDL Period	t_{PRD}	See Figure 3	20	–	143	μs
RDL Width	t_{WRD}		0.3	–	$t_{PRD}-0.3$	μs
RDL → WRT Timing	t_{RDW}		0	–	$t_{PRD}-0.6$	μs
Allowable XIN Input DC Offset Voltage	V_{OSXIN}	–	-100	–	+100	mV
Allowable AIN Input DC Offset Voltage	V_{OSAIN}	–	-100	–	+100	mV

Refer to Figure 16.

3. Power Dissipation

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power-Down Current	I_{DDS}	PDWN = 1	–	0.2	0.5	mA
	I_{SSS}		–	0.2	0.5	mA
Active Current	I_{DD}	PDWN = 0	–	14	25	mA
	I_{SS}		–	13	25	mA

NOTE) I_{DD} means both of I_{DD1} and I_{DD2}.

4. Digital Interface

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	–	0	–	0.6	V
Input High Voltage	V_{IH}	–	2.2	–	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 0.4 mA	0	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 20 μA	2.4	–	V_{DD}	V
Input Low Current	I_{IL}	DG ≤ V_{IN} ≤ V_{IL}	-10	–	10	μA
Input High Current	I_{IH}	V_{IH} ≤ V_{IN} ≤ V_{DD}	-10	–	10	μA
TD Data Set-up Time	t_{STD}	See Figure 2, 3	200	–	–	ns
TD Data Hold Time	t_{HTD}		100	–	–	ns
AGC Data Set-up Time	t_{SAG}		100	–	–	ns
AGC Data Hold Time	t_{HAG}		100	–	–	ns
RD Data Set-up Time	t_{SRD}	See Figure 3	200	–	–	ns
RD Data Hold Time	t_{HRD}		100	–	–	ns
AD Data Output Delay Time	t_{D1}	See Figure 2, 3	–	–	300	ns
	t_{D2}		–	–	300	ns

5. Analog Interface

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reference Voltage						
Reference Voltage	VR	Without adjustment $R_s = \infty$	+1.02	+1.20	+1.38	V
Backward Channel Transmit Signal Output (BOUT), External Signal Input (XIN)						
Output Resistance	R_{OB}	BOUT —	—	10	20	Ω
Load Resistance	R_{BOUT}	BOUT —	10	—	—	kΩ
Load Capacitance	C_{BOUT}	BOUT —	—	—	100	PF
DC Offset Voltage	V_{OSB}	BOUT —	-200	—	+200	mV
Output Carrier Level	V_{BOUT}	BOUT $R_{BOUT} \geq 10$ kΩ, V_{REF} = +2.50 V	1.74 -2	2.19 0	2.76 2	Vpp dBm
BWC Transmit Signal Level Ratio	L_{RBWC}	$\frac{V_{AOUT}\ (450\ Hz)}{V_{AOUT}\ (390\ Hz)}$	-1	0	1	dB
BWC Transmit Carrier Frequency — Mark "1"	f_{OBM}	BTD = 1	389	390	391	Hz
BWC Transmit Carrier Frequency — Space "0"	f_{OBS}	BTD = 0	449	450	451	Hz
Input Resistance	R_{XIN}	XIN —	25	50	—	kΩ
Input Signal Level	V_{XIN}	XIN —	—	—	4.38 +6	Vpp dBm

NOTE) 0 dBm = 0.775 Vrms = 2.19 Vpp

Transmit Analog Signal Ouput (AOUT)

Parameter		Symbol	Condition			Min	Typ	Max	Unit
Output Resistance		R_{OT}	—			—	10	20	Ω
Load Resistance		R_{AOUT}	—			10	—	—	kΩ
Load Capacitance		C_{AOUT}	—			—	—	100	PF
DC Offset Voltage		V_{OST}	XIN = AG			-200	—	+200	mV
Transmit Level (Single Tone)	Forward* Channel	V_{AOUT}	EQT1 = 1 EQT2 = 1 ATT1 = 1 ATT2 = 1 ATT3 = 1 V_{REF} = +2.50 V	f_{IN}	1.8 kHz Full scale	4.03 +5.3	5.08 +7.3	6.39 +9.3	Vpp dBm
Idle Channel Noise		N_{IDLT}	Using a 0.3 ~ 3.4 kHz flat weighted filter			—	-80	—	dBm
Total Harmonic Distortion		T_{HDT}	—			—	-65	-50	dB

* Transmit data (TD1~TD8) determine this level essentially. If the DA converter sends a single sine wave signal of which amplitude is ±2.5 Vop (Full scale of DA converter, equivalent +7 dBm) to the transmit filter, the transmit signal level at AOUT becomes +7.3 dBm (5.08 Vpp). But, generally in PSK or QAM modulation, maximum peak factor of about 3 dB or 7 dB should be considered in the design. Therefore, for instance, the transmit signal in the QAM forward channel is designed to be 0 dBm. This value shows one example of designs.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Receive Analog Signal Input (AIN)						
Input Resistance	R_{AIN}	–	100	–	–	kΩ
Receive Signal Level Range (Single Tone)	V_{AIN}	Single Tone	4.36		1095	mVo-p
		Allows the peak factor by PSK or QAM modulation.	-48	–	0	dBm
Receive Filter Output (RFO)						
Output Resistance	R_{OR}	–	–	10	20	Ω
Load Resistance	R_{RFO}	–	50	–	–	kΩ
Load Capacitance	C_{RFO}	–	–	–	100	PF
DC Offset Voltage	V_{OSR}	AIN = AG	-200	–	+200	mV
Output Signal Level	V_{RFO}	EQR1 = 1, EQR2 = 1 f_{IN} = 1800 Hz	V_{AIN} -2	V_{AIN}	V_{AIN} +2	dBm
Idle Channel Noise	N_{IDLR}	Using a 0.3 ~ 3.4 kHz flat weighted filter	–	-80	–	dBm
Total Harmonic Distortion	T_{HDR}	–	–	-65	-50	dB

Parameter	Symbol		Condition	Min	Typ	Max	Unit
AGC Circuit Input (AGCI), Output (AGCO)							
Input Resistance	R_{AGCI}	AGCI	–	50	100	–	kΩ
Allowable Input DC Offset Voltage	V_{OSAGCI}		–	-0.5	–	+0.5	mV
Input Signal Level Range*	V_{AGCI}		–	-45.4	–	+5.6	dBm
Output Resitance	R_{OA}	AGCO	–	–	10	20	Ω
Load Resistance	R_{AGCO}		V_{AGCO} = -6 dBm	10	–	–	kΩ
Load Capacitance	C_{AGCO}		–	–	–	100	PF
DC Offset Voltage	V_{OSA}		–	-50	–	+50	mV
Output Signal Level*	V_{AGCO}		Controlled by Demodulator	–	-6	–	dBm

* When V_{AGCI} is within this range, the signal level output from AGC circuit should be about -6 dBm with digitally controlling by the demodulating DSP.

6. Attenuator, Amplitude Equalizers and Filters Characteristics

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Attenuator						
Attenuation Accuracy (0 ~ 14 dB, 2 dB step)	A_{TT}	To the Designed Values	-1	0	+1	dB
Amplitude Equalizer (Transmit and Receive Paths)						
Frequency Characteristics (Relative gain to the gain at 1800 Hz) See Figure 4	EQ0 (Through)	EQT(R)1 = 1 EQT(R)2 = 1	f_{IN}	600 Hz	-1	0	+1	dB
				1200 Hz	-0.5	0	+0.5	
				2400 Hz	-0.5	0	+0.5	
				3000 Hz	-1	0	+1	
	EQ1 (I)	EQT(R)1 = 1 EQT(R)2 = 0		600 Hz	-2.4	-1.4	-0.4	
				1200 Hz	-1.2	-0.7	-0.2	
				2400 Hz	+0.2	+0.7	+1.2	
				3000 Hz	+0.1	+1.1	+2.1	
	EQ2 (II)	EQT(R)1 = 0 EQT(R)2 = 1		600 Hz	-4.8	-3.3	-1.8	
				1200 Hz	-2.8	-1.8	-0.8	
				2400 Hz	+0.4	+1.4	+2.4	
				3000 Hz	+1.2	+2.7	+4.2	
	EQ3 (III)	EQT(R)1 = 0 EQT(R)2 = 0		600 Hz	-6.8	-5.3	-3.8	
				1200 Hz	-3.7	-2.7	-1.7	
				2400 Hz	+1.0	+2.0	+3.0	
				3000 Hz	+2.3	+3.8	+5.3	
Gain Tolerance (Relative gain to the gain of EQ0 at 1800 Hz)	G_{EQ1}	EQT(R)1 = 1 EQT(R)2 = 0	f_{IN}	1800 Hz	-0.5	0	+0.5	dB
	G_{EQ2}	EQT(R)1 = 0 EQT(R)2 = 1			-0.5	0	+0.5	
	G_{EQ3}	EQT(R)1 = 0 EQT(R)2 = 0			-0.5	0	+0.5	

NOTE) This spec is applicable for only amplitude equalizers and does not include other filters' frequency characteristics.

Parameter	Symbol	Condition			Min	Typ	Max	Unit
BWC Transmit LPF								
2nd/3rd Harmonics Components Amplitude (Relative values to the fundamental component amplitude)	H_{BWC}	BTD = 1	$2 \cdot f_{OBM}$	780 Hz	–	-60	-55	dB
			$3 \cdot f_{OBM}$	1170 Hz	–	-60	-55	dB
		BTD = 0	$2 \cdot f_{OBS}$	900 Hz	–	-60	-55	dB
			3·fOBS	1350 Hz	–	-60	-55	dB
Transmit LPF								
Transmit LPF Voltage Gain	G_{TL}	EQT1, 2 = 1 ATT1, 2, 3 = 1 V_{XIN} = −10 dBm		390 Hz 450 Hz	-2	0	+2	dB
				1700 Hz 1800 Hz	-0.8	+1.2	+3.2	dB
Frequency – Amplitude Characteristics (Relative gain to G_{TL} at 390 Hz)	A_{TL}	EQT1, 2 = 1 ATT1, 2, 3 = 1 V_{XIN} = −10dBm	f_{IN}	2400 Hz	+0.5	+1.5	+2.5	dB
				6000 Hz	–	-26	-23	dB
Group Delay Distortion	D_{TL}	EQT1, 2 = 1 1100 Hz ≤ f_{IN} ≤ 2300 Hz			–	–	120	μs
Receive BPF								
Receive BPF Voltage Gain	G_{RB}	EQR1, 2 = 1 V_{AIN} = 0 dBm f_{IN} = 1700 Hz			-2	0	+2	dB
Frequency – Amplitude Characteristic (Relative gain to G_{RB})	A_{RB}	EQR1, 2 = 1 V_{AIN} = 0 dBm	f_{IN}	150 Hz	–	-14	-11	dB
				300 Hz	-4.2	-2.2	-0.2	dB
				3000 Hz	+3	+4	+6	dB
				6000 Hz	–	-19	-16	dB
Group Delay Distortion	D_{RB}	EQR1, 2 = 1 1100 Hz ≤ f_{IN} ≤ 2300 Hz			–	–	100	μs

Parameter	Symbol	Condition			Min	Typ	Max	Unit
Receive HPF								
Receive HPF Voltage Gain *1	G_{RH}	EQR1, 2 = 1 V_{AIN} = 0 dBm f_{IN} = 620 Hz			−2	0	+2	dB
Frequency – Amplitude Characteristics (Relative gain to G_{RH}) *1	A_{RH}	EQR1, 2 = 1 V_{AIN} = 0 dBm	f_{IN}	390 Hz	—	−77	−65	dB
				450 Hz	—	−71	−65	dB
				500 Hz	—	−40	−36	dB
Group Delay Distortion *1	D_{RH}	EQR1, 2 = 1 1100 Hz ≤ f_{IN} ≤ 2300 Hz			—	—	750	μs
Receive LPF (for Call Progress Tone Detection)								
Receive LPF Voltage Gain *1	G_{RL}	EQR1, 2 = 1 V_{AIN} = 0 dBm f_{IN} = 400 Hz			−4	−2	0	dB
Frequency – Amplitude Characteristics (Relative gain to G_{RL}) *1	A_{RL}	EQR1, 2 = 1 V_{AIN} = 0 dBm	f_{IN}	150 Hz	—	−14	−11	dB
				350 Hz	−2.5	−1.5	−0.5	dB
				910 Hz	—	−56	−53	dB

*1 : Includes Receive BPF's characteristics.

NOTE) Each Spec. is measured according to the following table.

Circuits	Signal Input	Signal Output	BWC1	BWC2	ATT 1,2,3	EQT 1,2	EQR 1,2	Measured Block	Reference Figure
Attenuator	XIN	AOUT	—	—	000 ≀ 111	1	—	ATT + T·LPF	5
Transmit Amplitude Equalizer	XIN	AOUT	—	—	1	00 ≀ 11	—	AEQL + T·LPF	4, 5
BWC Transmit LPF	BOUT →XIN	AOUT	1	1	1	1	—	BWC·LPF + T·LPF	5, 6
Transmit LPF	XIN	AOUT	—	—	1	1	—	T·LPF	5
Receive Amplitude Equalizer	AIN	RFO	1	1	—	—	00 ≀ 11	AEQL	4
Receive BPF	AIN	RFO	0	0	—	—	1	R·BPF	7
Receive HPF	AIN	RFO	0	1	—	—	1	R·HPF + R·BPF	7, 8
Receive LPF	AIN	RFO	1	0	—	—	1	R·LPF + R·BPF	6, 7

Table 1

7. DA, AD Converter and AGC Circuit

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Transmit Digital to Analog Converter								
Bits of Resolution		B_{REST}	–		–	8	–	bit
DA Conversion Reference Voltage		V_{REF}	–		–	+2.50	–	V
Full Scale*	Plus Full Scale	PFV_{DA}	V_{REF} = + 2.50 V	TD8 ~ TD1: 01111111	+2.31	+2.367	+2.42	V
	Minus Full Scale	NFV_{DA}		TD8 ~ TD1: 10000000	–2.44	–2.386	–2.33	V
Linearity*		N_{LDA}	–			0.5	1.0	%
Receive Analog to Digital Converter								
Bits of Resolution		B_{RESR}	–		–	8	–	bit
AD Conversion Reference Voltage		V_{REF}	–		–	+2.50	–	V
Full Scale*	Plus Full Scale	PFV_{AD}	V_{REF} = + 2.50 V Equivalent values to the input voltage of AD converter		+2.42	+2.48	+2.54	V
	Minus Full Scale	NFV_{AD}			-2.56	-2.50	-2.44	V
Linearity*		NL_{AD}	–		–	0.5	1.0	%
Output DC Offset*		V_{OSAD}	Includes the AGC circuit		–3	–	+3	LSB
AGC Circuit								
Gain Control Bits of Resolution		B_{RESA}	–		–	8	–	bit
Dynamic Range		DY_{AGC}	–		–	51	–	dB
Gain Setting Minimum Step		G_{STP}	–		–	0.2	–	dB
Gain Setting Accuracy		G_E	–		–0.4	0	+0.4	dB
Total Harmonic Distortion		THD_{AGC}	–		–	–	-50	dB
Signal to Noise Ratio		SN_{AGC}	Set Gain = Maximum Signal/Noise at AGCO		50	–	–	dB

* This specification is defined as the voltage at the A_{OUT} terminal, but does not include the DC offset voltage at the terminal.

* This specification does not include the DC offset voltage at the input of the AD converter (AGCO).

8. Timing Characteristics

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Carrier Detect and Level Comparator for AGC Circuit

Parameter		Symbol	Condition			Min	Typ	Max	Unit
CD1 See Figure 9-1	OFF→ON	T_{CDON1}	CD1H = V_{SS}	CD1L = 0 BWC1 = 0	V_{AIN} = 0 dBm f_{IN} = 1700 Hz	–	2.1	–	ms
	ON →OFF	T_{CDOFF1}				–	9.6	–	ms
	OFF→ON	T_{CDON2}			V_{AIN} = -36 dBm f_{IN} = 1700 Hz	–	2.7	–	ms
	ON →OFF	T_{CDOFF2}				–	6.7	–	ms
	OFF→ON	T_{CDON3}		CD1L = 1 BWC1 = 0	V_{AIN} = 0 dBm f_{IN} = 1800 Hz	–	1.8	–	ms
	ON →OFF	T_{CDOFF3}				–	9.0	–	ms
	OFF→ON	T_{CDON4}			V_{AIN} = -39 dBm f_{IN} = 1800 Hz	–	2.6	–	ms
	ON →OFF	T_{CDOFF4}				–	5.4	–	ms
	OFF→ON	T_{CDON5}		BWC1 = 1 BWC2 = 0	V_{AIN} = 0 dBm f_{IN} = 400 Hz	–	1.7	–	ms
	ON →OFF	T_{CDOFF5}				–	20.0	–	ms
	OFF→ON	T_{CDON6}			V_{AIN} = -40 dBm f_{IN} = 400 Hz	–	4.5	–	ms
	ON →OFF	T_{CDOFF6}				–	5.0	–	ms
CD2 See Figure 9-1	OFF→ON	T_{CDON7}	CD2H = V_{SS}		V_{AIN} = 0 dBm f_{IN} = 1650 Hz	–	1.2	–	ms
	ON →OFF	T_{CDOFF7}				–	10	–	ms
	OFF→ON	T_{CDON8}			V_{AIN} = -40 dBm f_{IN} = 1650 Hz	–	2.0	–	ms
	ON →OFF	T_{CDOFF8}				–	6.0	–	ms
LD1 See Figure 9-2	OFF→ON	T_{LD1ON}				–	*	–	ms
	ON →OFF	T_{LD1OFF}				–	*	–	ms
LD2 See Figure 9-2	OFF→ON	T_{LD2ON}				–	*	–	ms
	ON →OFF	T_{LD2OFF}				–	*	–	ms

*TBD

Power Down Control Timing

Power ON Time	T_{PWON}	PWDN: 1→0 See Figure 10	–	–	200	ms
Power Down Time	T_{PWOFF}	PWDN: 0→1 See Figure 10	–	–	10	ms

9. Transmission Performance

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Transmitter							
Out-of-Band Energy Referred to Carrier Level	E_{OT}	EQT1, 2 = 1 V_{AOUT} = −10 dBm See Figure 11	4 ~ 8 kHz	–	–	-20	dB
			8 ~ 12 kHz	–	–	-40	dB
			12 kHz ~	–	–	-60	dB

Receiver

Dynamic Range	DY_R	As a single tone				-48	–	0	dBm/600Ω
Carrier Detect Threshold*3	TH_{CDON1}	CD1H = V_{SS}	CD1L = 0 BWC1 = 0 f_{IN} = 1700 Hz	CD1	ON	–	-39.2	–	dBm
	TH_{CDOFF1}				OFF	–	-49.3	–	dBm
	TH_{CDON2}		CD1L = 1 BWC1 = 0 f_{IN} = 1800 Hz	CD1	ON	–	-41.8	–	dBm
	TH_{CDOFF2}				OFF	–	-46.8	–	dBm
	$TH_{CDON/OFF3}$		BWC1 = 1 BWC2 = 0 f_{IN} = 400 Hz	CD1	ON/OFF	–	-45*1	–	dBm
	TH_{CDON4}	CD2H = V_{SS} f_{IN} = 1650 Hz		CD2	ON	–	-45	–	dBm
	TH_{CDOFF4}				OFF	–	-50	–	dBm
*2 Optional Carrier Detect Threshold by External Potentials	TH_{CDON5}	CD1L: 0 ~ V_{DD}		CD1	ON	Adjustable			dBm
	TH_{CDOFF5}	CD1H: 0 ~ V_{DD}			OFF	Adjustable			dBm
	TH_{CDON6}	CD2L: 0 ~ V_{DD}		CD2	ON	Adjustable			dBm
	TH_{CDOFF6}	CD2H: 0 ~ V_{DD}			OFF	Adjustable			dBm

*1 This operating mode is used during the call progress tone monitoring and does not provide the hysteresis of the detect ON and OFF level.

*2 In this mode, CD1's ON/OFF and CD2's ON/OFF levels are determined by external adjustments. It is impossible to use the optional threshold either for CD1 or CD2.

*3 Threshold levels are defined by a single tone input on the AIN terminal. In actual applications, however, input analog signal is not a single tone but a modulated signal by FSK, PSK or QAM. Therefore, the hysteresis values (CD/OFF-CD/ON) become less than the differences of CD/ON and CD/OFF levels shown in the specification table.

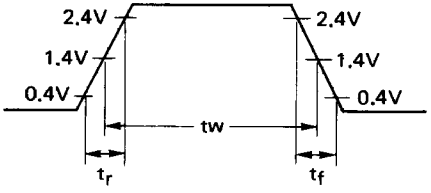


Figure 1 Definition of Rise/Fall Time

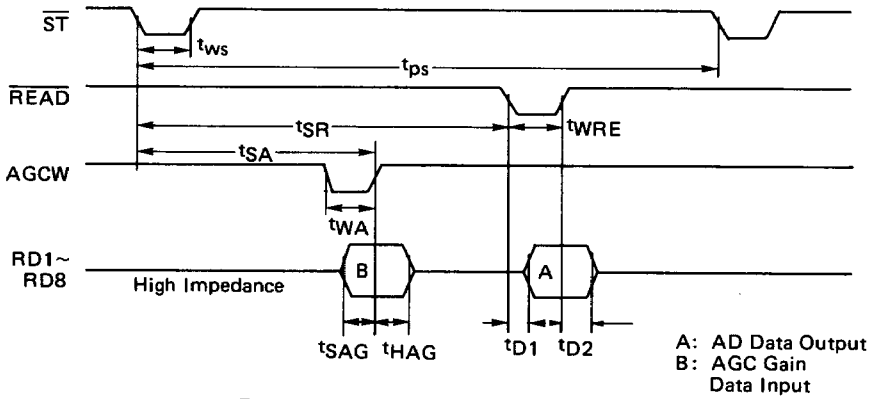


Figure 2-1 Receive Data Timing Chart

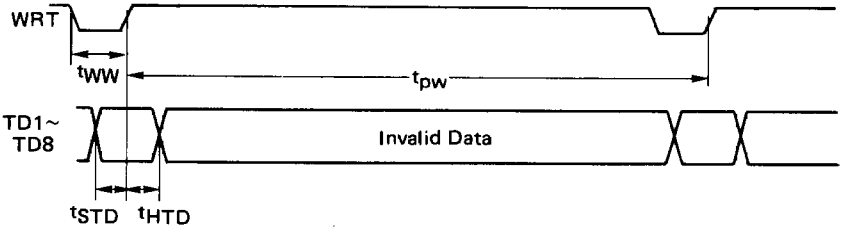


Figure 2-2 Transmit Data Timing Chart

NOTE) Figure 2-1 and Figure 2-2 show the timing when transmit data is input to the chip via TD1 through TD8.

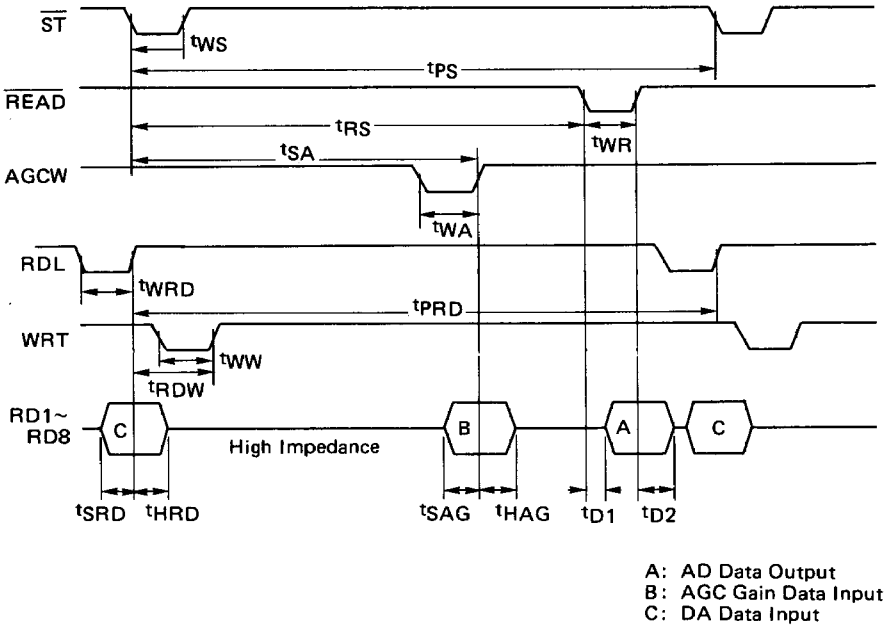


Figure 3 Transmit and Receive Data Timing Chart

NOTE) Figure 3 shows the timing when transmit, receive and AGC data are interfaced via RD1 through RD8 as a common data bus.

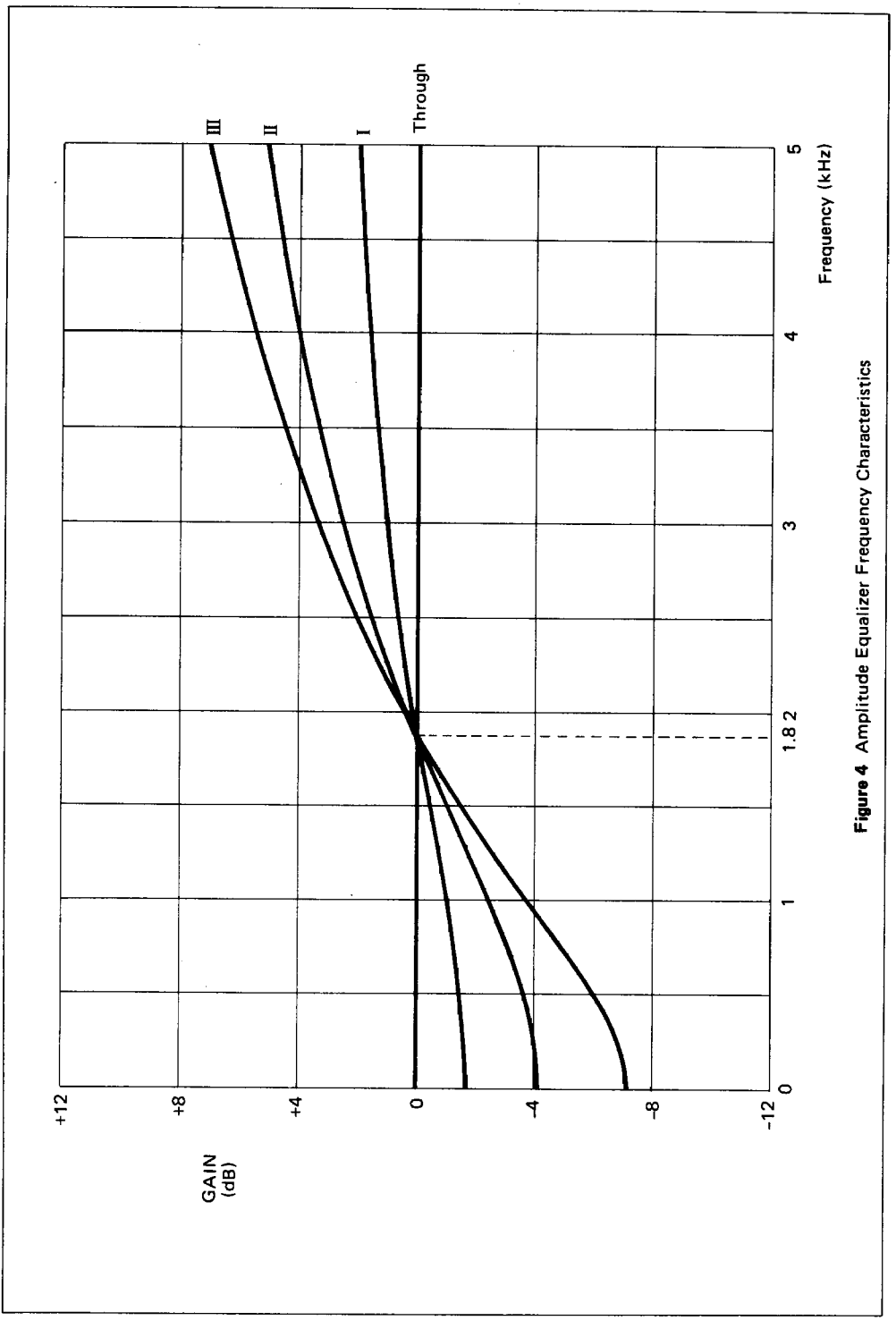


Figure 4 Amplitude Equalizer Frequency Characteristics

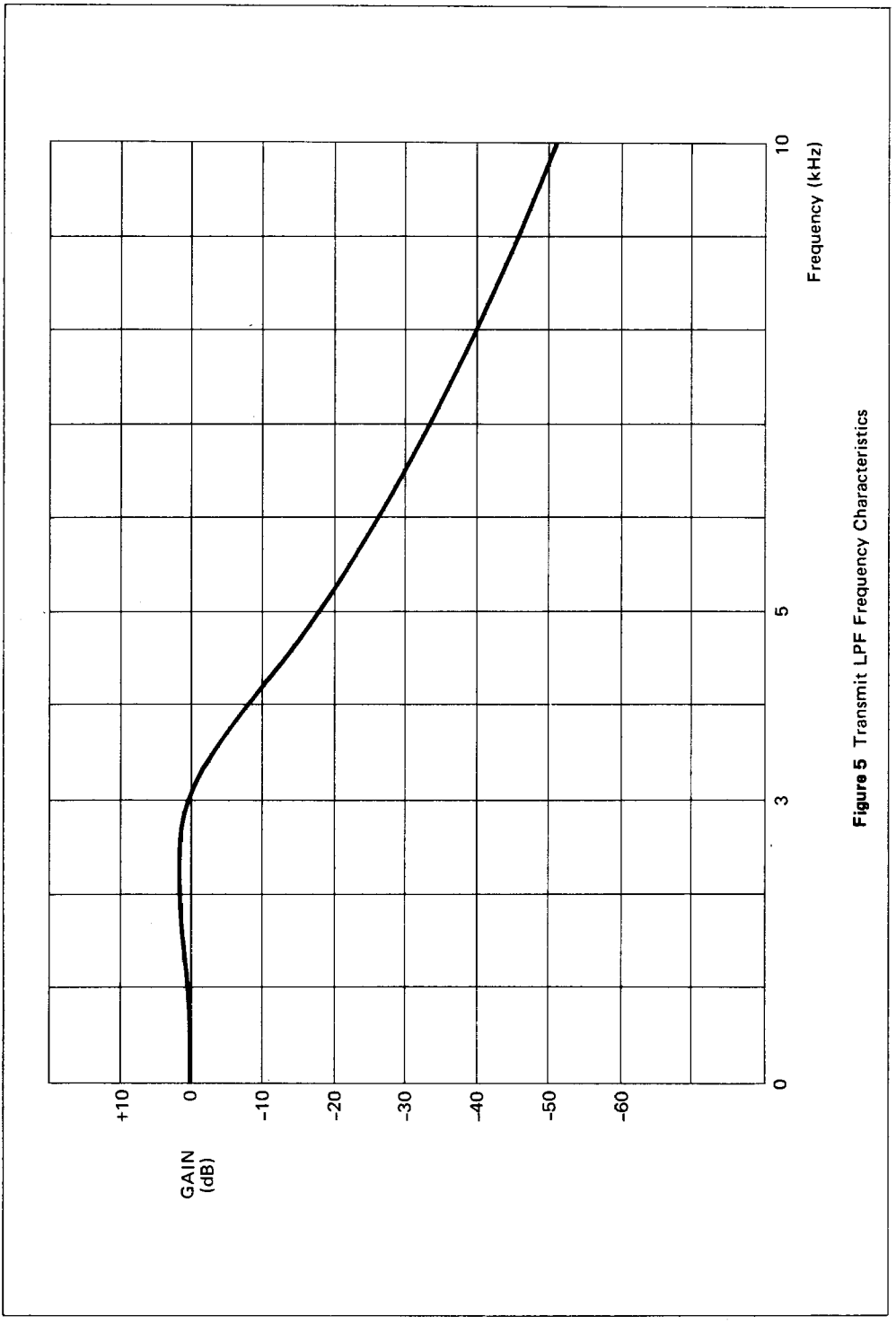


Figure 5 Transmit LPF Frequency Characteristics

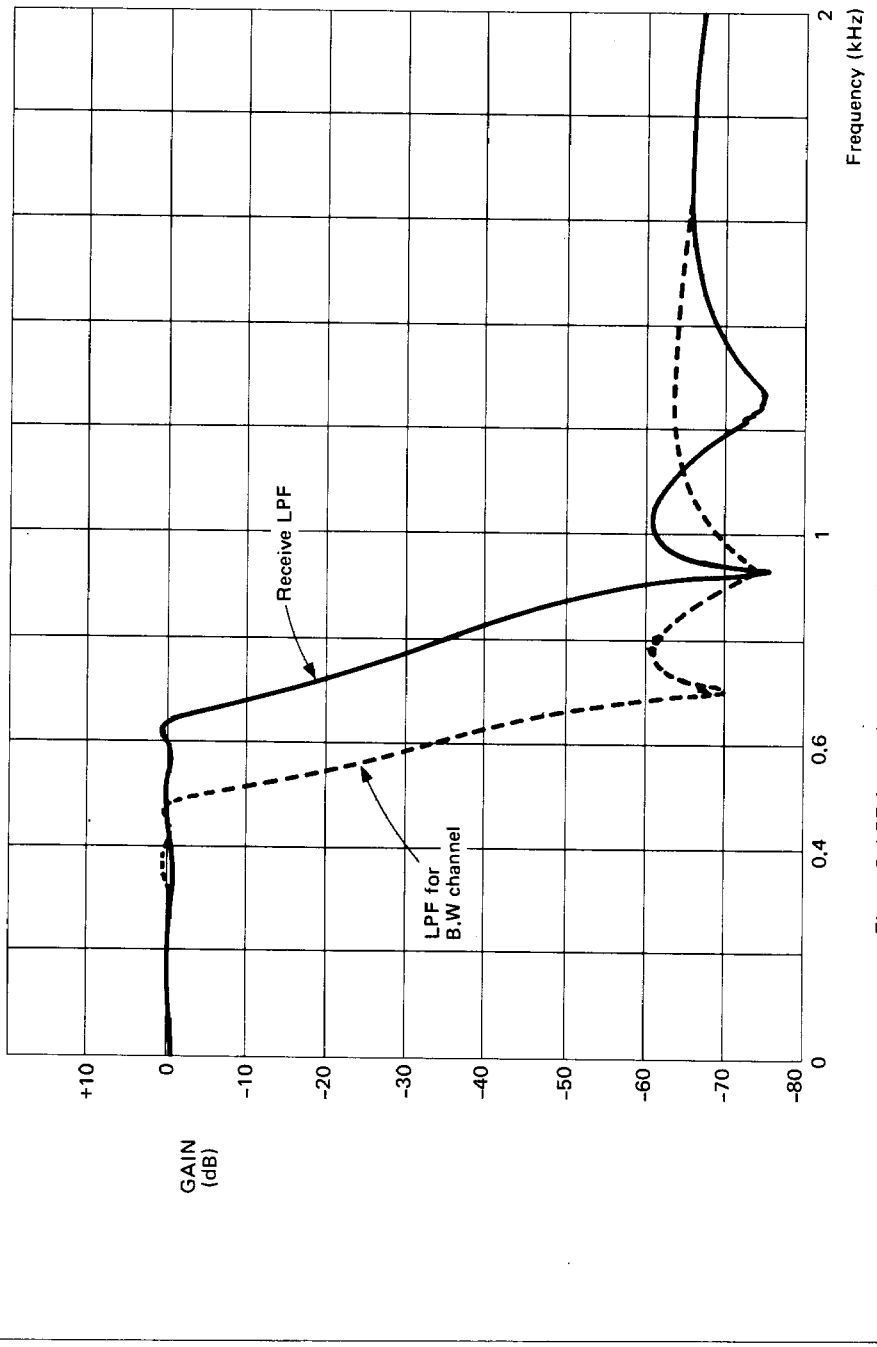


Figure 6 LPF for Backward Channel/Receive LPF Frequency Characteristics

NOTE) The LPF is used for both transmit and receive path changed its bandwidth.

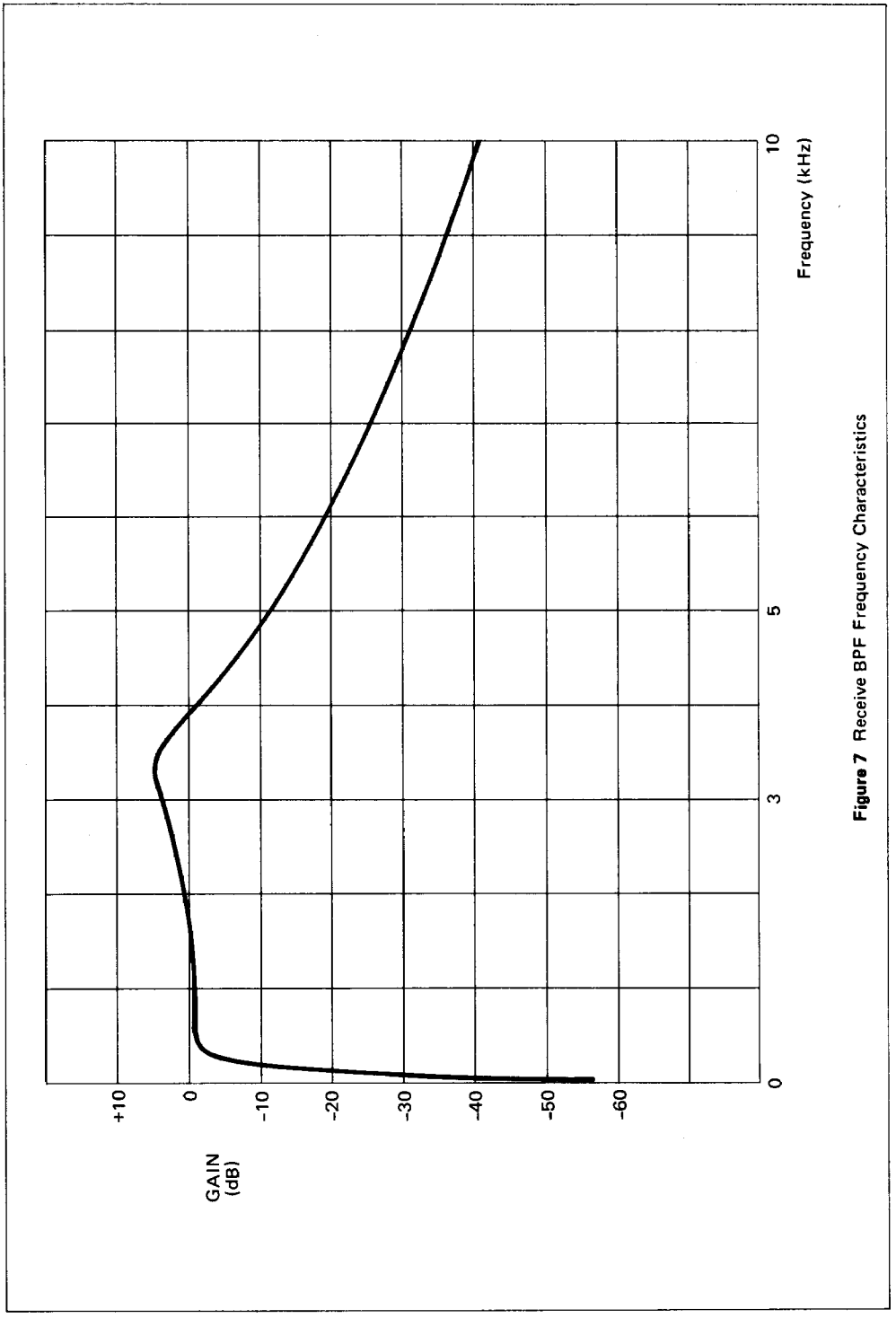


Figure 7 Receive BPF Frequency Characteristics

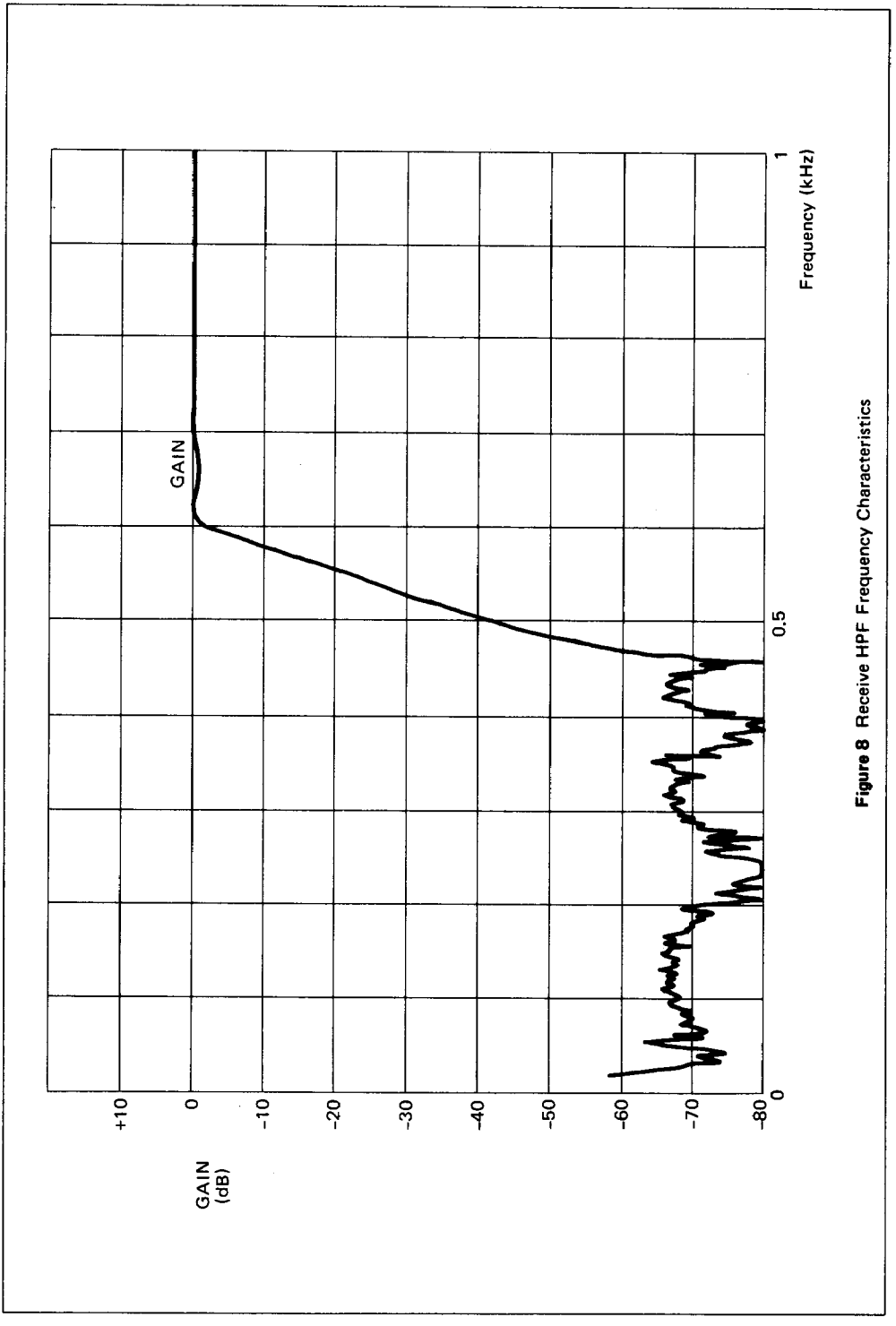


Figure 8 Receive HPF Frequency Characteristics

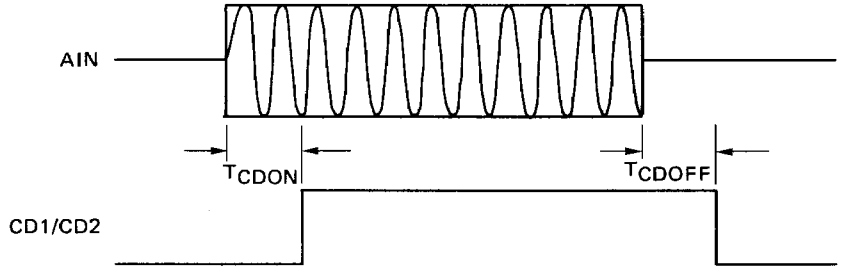


Figure 9-1

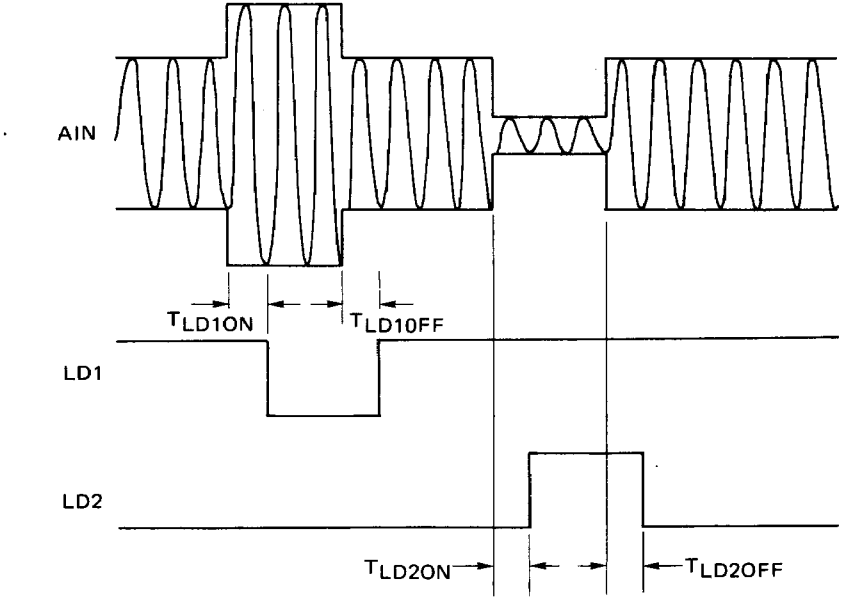


Figure 9-2

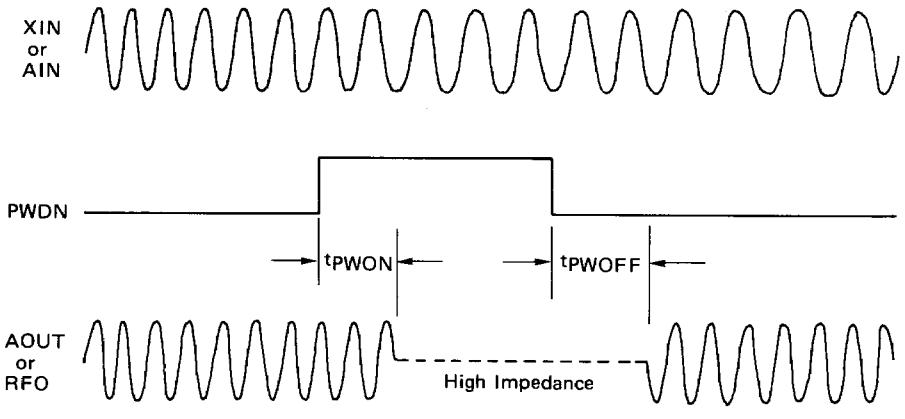


Figure 10 Power Down Mode Response

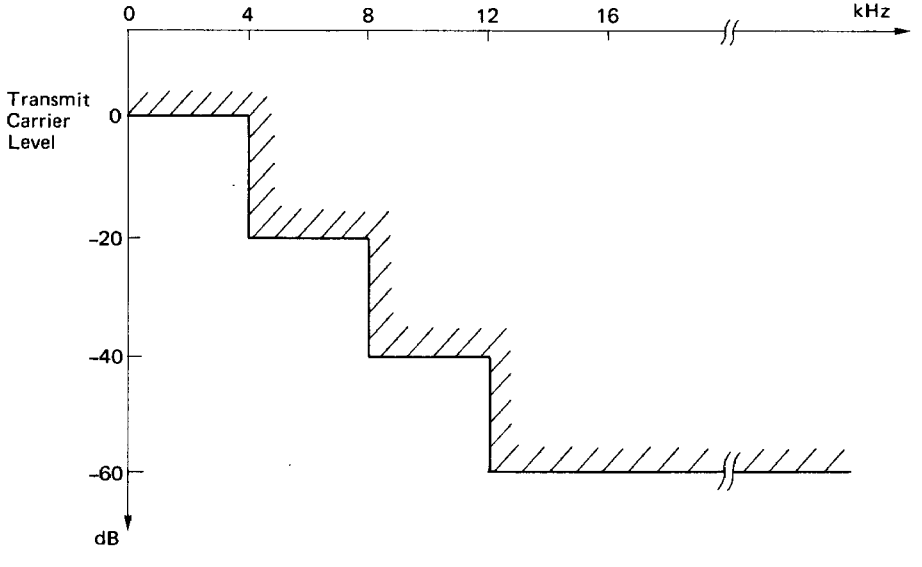


Figure 11 Maximum Level of Out-of-Band Energy Relative to the Transmit Carrier Level

PIN DESCRIPTION

Pin Name	Pin No. SS	JS	GS	Function
$\overline{BRS}$	1	2	59	The chip contains 75 bps FSK modulator (420 ± 30 Hz) that is useful for some kinds of applications, such as videotex systems.
BTD	2	3	60	$\overline{BRS}$ controls the modulator to send FSK signal over telephone line through AOUT.

$\overline{BRS}$	FSK signal transmit
Digital 0	Enable
Digital 1	Disable

Table 2

BTD is the transmit data that should be converted to the modulated FSK signal to be sent over telephone line.

BTD	FSK signal frequency
Digital 0	"Space" 450 Hz
Digital 1	"Mark" 390 Hz

Table 3

TRSW	3	4	61	On-chip DA converter can operate according to not only TD, but also RD for its input data. This function is significant in the special application where both RD and TD are given to and taken from the same data bus line. At this case, it is required to put TRSW on digital 1 state for connecting the input of DA to RD terminals internally in place of TD terminals.
RDL	4	5	62	A clock pulse should be input to RDL to latch RD on it's positive edge. Refer to Figure 12.

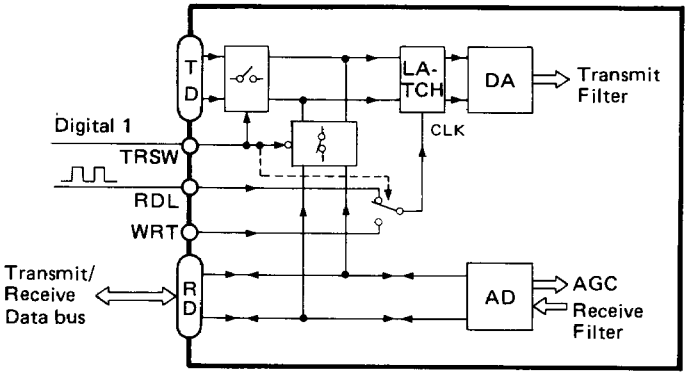


Figure 12

Pin Name	Pin No. SS	JS	GS	Function
WRT	5	6	63	This signal controls to write the data on TD1 ~ TD8 into the DA converter. These data are latched on the positive edge of WRT.
TD1 〉 TD8	13 〉 6	14 〉 7	7 〉 1, 64	Transmit signal digital data input for DA conversion. These pins are 8-bit parallel two's complement data input pins, and the data are loaded into the DA converter on the positive edge of WRT. TD1 is the LSB and TD8 is the MSB. Refer to Table 4.
MCK	14	15	8	A 3.456 MHz clock signal should be applied to this pin. This is the time base for the operation of MSM6949 and is divided down within the chip for variety of internal uses.
V_{DD2}	15	16	9	Positive power supply, +5V. This pin is internally connected only to the digital output logic circuitry for RD1 ~ RD8, RDA and RDB.
RD1 〉 RD8	24 〉 17	26 〉 19	17 〉 10	These are I/O terminals. When $\overline{READ}$ is held on digital 0 state, these pins become output terminals and the result of the AD conversion with 8-bit (or 10-bit) parallel two's complement format appears. Refer to Table 4. When $\overline{READ}$ is held on digital 1 state, these pins become input terminals and the data input to these pins are loaded into the register storing them as the gain setting data for AGC circuit on the positive edge of AGCW.

TD/RD	8	7	6	5	4	3	2	1
Plus Full Scale	0	1	1	1	1	1	1	1
⋮								
Plus 0	0	0	0	0	0	0	0	0
Minus 0	1	1	1	1	1	1	1	1
⋮								
Minus Full Scale	1	0	0	0	0	0	0	0

Table 4 8-digit Data Table for TD and RD

Pin Name	Pin No. SS	JS	GS	Function
				To input digital 1 to each digit of RD1 ~ RD8 means the following amplitude per digit for AGC circuit.

Pin	Gain	Pin	Gain
RD1	+0.2 dB	RD5	+3.2 dB
2	+0.4	6	+6.4
3	+0.8	7	+12.8
4	+1.6	8	+25.6

Table 5

The actual values of AGC circuit's relative and absolute gain are as shown in Table 6.

RD								Gain (dB)	
8	7	6	5	4	3	2	1	Relative	Absolute
1	0	0	0	0	0	0	0	-25.5	-11.6
1	0	0	0	0	0	0	1	-25.3	-11.4
1	1	1	1	1	1	1	1	-0.1	+13.8
0	0	0	0	0	0	0	0	+0.1	+14.0
0	1	1	1	1	1	1	0	+25.3	+39.2
0	1	1	1	1	1	1	1	+25.5	+39.4

Table 6

RDB	25	27	18	These are 3-state output pins to extend the RD bit length when CSW is set at digital 1 state. When CSW is set at digital 1 state, each digit of RD8 ~ RD1 is shifted toward less significant bit by 2 bits and this makes RDA become LSB and MSB appears on RD6, RD7 and RD8 with the same data. This processing is useful to attenuate the received signal level for the demodulator.
RDA	26	28	19	
$\overline{ST}$	27	29	20	This signal allows the MSM6949 to start the AD conversion on the negative edge of $\overline{ST}$. The conversion period should be within 51 ~ 143 μs. The latest AD converted data appear on the RD pins 44 μs after from the falling edge of $\overline{ST}$.

Pin Name	Pin No. SS	JS	GS	Function
$\overline{\text{READ}}$	28	30	21	This is a control signal for 3-state output data bus line RD8 ~ RD1, RDA and RDB. While this pin is in digital 0 state, the output bus is active and the result of the AD conversion appears on RD8 ~ RD1, While this pin is in digital 1 state, the output bus is inactive and RD8 ~ RD1, RDA and RDB become input terminals.
AGCW	29	31	22	This signal controls to load the gain setting data into the register for AGC circuit through RD8 ~ RD1 on the positive edge of AGCW. At this time, $\overline{\text{READ}}$ must be in digital 1 state.
CSW	30	32	23	As mentioned in the description of RDA and RDB, the RD bit length is extended from 8-bits to 10-bits and the position of each digit is shifted by 2-bits toward the less significant digit when CSW is set at digital 1 state.
LD1	31	33	24	These output signals are of comparators which have different threshold levels each other and the inputs are connected to the output of AGC circuitry (AGCO). When AGCO shows an extraordinary signal level by the abrupt change in the received signal level, LD1 and LD2 can be a warning signal for the demodulator and the AGC circuit.
LD2	32	34	25	

	Signal level on AGCO (dBm)				
	+2	+1		-14.5	-15.5
LD1	0		1		
LD2	0				1

Table 7

For example, the demodulator should be reset when LD1 indicates the digital 0 state.

In other case when LD2 indicates the digital 1 state, the AGC circuit should be set at the nominal gain by setting digital 0 to all of RD digits for the quick escape from the abnormal state. Refer to Table 7 and Figure 13.

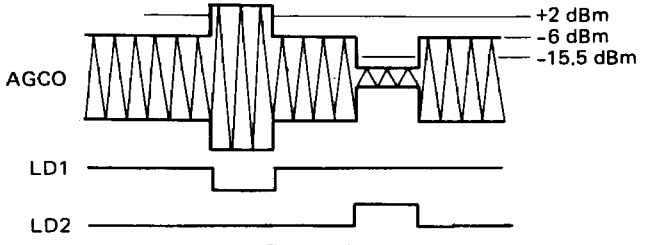


Figure 13

Pin Name	Pin No. SS	JS	GS	Function
CD1	33	35	26	The MSM6949 provides a pair of carrier detect circuitry and each of them has a inherent detect level which is internally fixed.
CD2	34	36	27	On the other hand, their carrier detect levels can be determined by external circuit by using CD1L, CD1H, CD2L and CD2H. Usually, CD1 is used for 2400, 4800, 7200 and 9600 bps data transmission, or for call progress tone monitoring. CD2 is used for FSK transmission, such as CCITT T. 30. The state of digital 1 means that the received signal is within the level range to be demodulated. When indicating the digital 0 state, the received data should be ignored as meaningless information. Refer to the descriptions for CD1L, CD1H, CD2L and CD2H.
BWC1	35	37	28	These control signals determine the receive filter bandwidth according to the application's requirement. Refer to Figure 6, 7 and 8.
BWC2	36	38	29	

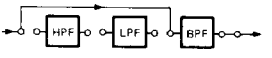
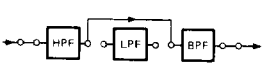
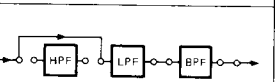
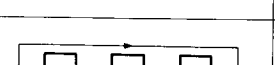
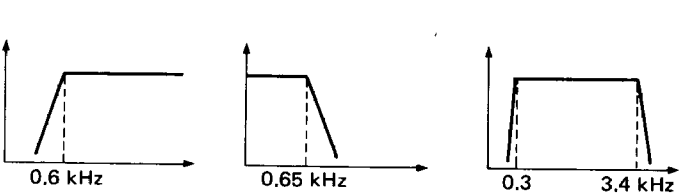
BWC1	BWC2	Receive Filter Composition	Band-width	Application
0	0		0.3 ~ 3.4 kHz	No backward channel transmitting
0	1		0.6 ~ 3.4 kHz	Backward channel transmitting
1	0		0.3 ~ 0.65 kHz	Call progress tone monitor-ing
1	1		Through	Special case (External Filter)

Table 8



<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>SS</th><th>JS</th><th>GS</th></tr>
<tr><td></td><td></td><td></td><td></td><td>When a modem operates without backward channel (BWC) transmiting, receive signal bandwidth should be extended to 0.3 kHz for better transmission data quality. When a modem operates with BWC transmitting, the receive filter must reject the BWC signal which leaks from own BWC transmitter through the hybrid circuit in the 2-wire facilities.
As backward channel transmitting signal's components exsist below 0.6 kHz, the received data quality would be deteriorated if HPF to eliminate them is not used.
Usually, the frequencies of call progress tones are included in the range from 0.3 kHz to 0.65 kHz. The MSM6949 have the filter for detecting those tones.</td></tr>
<tr><td>EQR1</td><td>37</td><td>39</td><td>30</td><td rowspan="2">For better transmission data quality, amplitude equalizers are provided about MSM6949 in both transmitter and receiver.
<table><tr><th>EQR1 / EQT1</th><th>EQR2 / EQT2</th><th>Equalizing Characteristics</th></tr><tr><td>0</td><td>0</td><td>III</td></tr><tr><td>0</td><td>1</td><td>II</td></tr><tr><td>1</td><td>0</td><td>I</td></tr><tr><td>1</td><td>1</td><td>Through</td></tr></table>Table 9
Refer to Figure 4.</td></tr>
<tr><td>EQR2</td><td>38</td><td>40</td><td>31</td></tr>
<tr><td>DG</td><td>39</td><td>41</td><td>32</td><td>Digital ground, 0V.</td></tr>
<tr><td>AG</td><td>40</td><td>42</td><td>33</td><td>Analog ground, 0V.
When digital and analog circuitry are implemented in the same chip, analog functional performances are easy to be deteriorated by the digital noise. Especially, when the digital noise is asynchronous to the operating timing for analog circuitry, such as switched capacitor filter, AD and DA converter, the chip's performances become serious. The delicate chip is designed carefully so that the influence becomes less, but it is important not to mix the noise to AG as possible and design of PCB should be taken care of.</td></tr>
<tr><td>V_{SS}</td><td>41</td><td>43</td><td>34</td><td>Negative power supply, -5V.</td></tr>
</table>

Pin Name	Pin No. SS	JS	GS	Function
AGCC	42	44	35	An external capacitor of 0.1 μF should be connected between AGCC and AG. This capacitor is necessary to compensate the DC offset voltage generated in the AGC circuit.
AGCO	43	45	36	The output of the AGC circuit. This pin is used for the chip test, etc. The gain setting data should be loaded into the chip through RD8 ~ RD1 so that the signal level at AGCO becomes -6 dBm.
AGCI	44	47	37	AGCI is the input of the AGC circuit and RFO is the receive filter's output. These pins should be mutually connected via an external capacitor of 0.1 μF. This capacitor is required as an AC-coupling not to transfer the DC offset voltage to the AGC circuit. The input impedance of AGCI is typically 100 kΩ.
RFO	45	48	38	
CD1L	46	49	40	As described in the description of CD1 and CD2, a pair of carrier detect circuits can be used with the internally fixed inherent detect levels.
CD1H	47	50	41	On the other hand, detect levels can be externally adjusted for various kinds of applications. Internal fixed values and external adjustments are as follows.
CD2L	48	51	42	
CD2H	49	52	43	

CD1L	CD1H	CD2L	CD2H	BWC1	BWC2	CD1 ON	CD1 OFF	CD2 ON	CD2 OFF	Operating MODE
0	VSS	*	*	0	*	-39.2	-49.3	–	–	7200/9600 bps
1	VSS	*	*	0	*	-41.8	-46.8	–	–	2400/4800 bps
*	VSS	*	*	1	0	-45	–	–	–	Call Progress Tone
*	*	*	VSS	*	*	–	–	-45	-50	300 bps (T. 30)
>0V	>0V	*	*	0	*	Depend on V_{CD1L}, V_{CD1H}		–	–	External Adjustment
>0V	>0V	*	*	1	0	Depend on V_{CD1L}, V_{CD1H}		–	–	
*	*	>0V	>0V	*	*	–	–	Depend on V_{CD2L}, V_{CD2H}		

NOTE 1) Unit of CD1/2 detect level: dBm (0 dBm = 0.775 Vrms)
2) These levels are defined with a single tone.

Table 10

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>SS</th><th>JS</th><th>GS</th></tr>
<tr><td></td><td></td><td></td><td></td><td>If an external adjustment is required, each of these terminals should be connected to the appropriate potential, which is over 0V, and this determines the carrier detect ON/OFF level. Four different kind of potentials determine the level as follows.

<table>
<tr><th>Terminal</th><th>Carrier Detect</th></tr>
<tr><td>CD1L</td><td>CD1 OFF</td></tr>
<tr><td>CD1H</td><td>CD1 ON</td></tr>
<tr><td>CD2L</td><td>CD2 OFF</td></tr>
<tr><td>CD2H</td><td>CD2 ON</td></tr>
</table>
Table 11

As an aim for external adjustment, it can be forecast that the carrier detect threshold level becomes about -40 dBm when the input potential is plus 2.5 V. The relation between the potential and the level is linear.</td></tr>
<tr><td>VR1</td><td>50</td><td>53</td><td>44</td><td>The MSM6949 provides the voltage reference which is used for AD and DA conversions, carrier detect, backward channel transmitter, etc.</td></tr>
<tr><td>VR2</td><td>51</td><td>54</td><td>45</td><td>The potential is stabilized to variations of temperature or supply voltages, but tends to be different from chip to chip. Therefore, an external adjustment is necessary.

The resistors used to adjust the reference voltage are connected to these pins as follows.

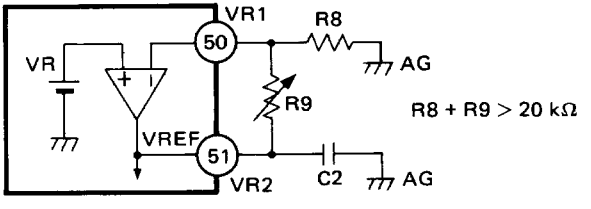
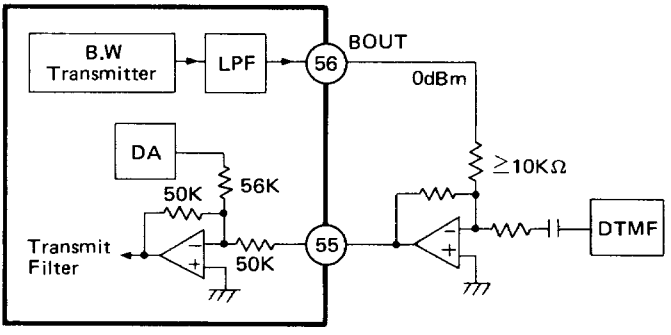
 

Figure 14

A bypass capacitor is required to keep this reference potential in the silent condition and the value of 1 μF is recommended. The reference voltage on VR2 (VREF) is approximately determined by the following equation and the typical value is +2.5V.

$$V_{REF} \simeq 1.2 \times \frac{R8 + R9}{R8} [V]$$</td></tr>
<tr><td>AIN</td><td>52</td><td>56</td><td>46</td><td>This pin is the receive analog signal input.</td></tr>
</table>

Pin Name	Pin No.			Function
	SS	JS	GS	
AOUT	54	57	47	This is the transmit analog signal output pin. The output resistance is about 10Ω and the load resistance should be more than 10 kΩ.
XIN	55	59	48	This is an external analog signal input. Usually, XIN is used as the input for the backward channel transmitter, and frequently for an external DTMF tone. This signal is routed to the transmit filter's input via an adder same as the signal from the DA converter.  **Figure 15** An external operational amplifier can be omitted when the DTMF tone is not input to XIN, and BOUT is connected to XIN directly.
BOUT	56	60	49	This is an output terminal of the backward channel transmitter. Refer to the description for XIN. The signal level is about 0 dBm. While call progress tone monitoring is proceeding, BOUT is internally connected to AG, because LPF is used in the receiver side.
PWDN	57	61	51	When digital 1 is input to PWDN, whole functions in the MSM6949 are disabled and the MSM6949 goes into the power standby mode. At this time, AOUT and RFO become high impedance state.
LT	58	62	52	LT is used to provide the signal path for the local analog loop (AC) test function. When digital 1 is input to LT, the transmit analog signal is routed to the input of the receive filter and AOUT is connected to AG internally.

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>SS</th><th>JS</th><th>GS</th></tr>
<tr><td>EQT1</td><td>59</td><td>63</td><td>53</td><td>Refer to the description of EQR1 and EQR2.</td></tr>
<tr><td>EQT2</td><td>60</td><td>64</td><td>54</td><td></td></tr>
<tr><td>ATT1
∫
ATT3</td><td>61
∫
63</td><td>65
∫
67</td><td>55
∫
57</td><td>The MSM6949 provides attenuator for transmit signal.
<table>
<tr><th>ATT1</th><th>ATT2</th><th>ATT3</th><th>Signal Level Loss (dB)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>14</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>12</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>10</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table>
Table 12</td></tr>
<tr><td>V_{DD1}</td><td>64</td><td>68</td><td>58</td><td>Positive power supply, +5V.</td></tr>
</table>

CIRCUIT WIRING ILLUSTRATION

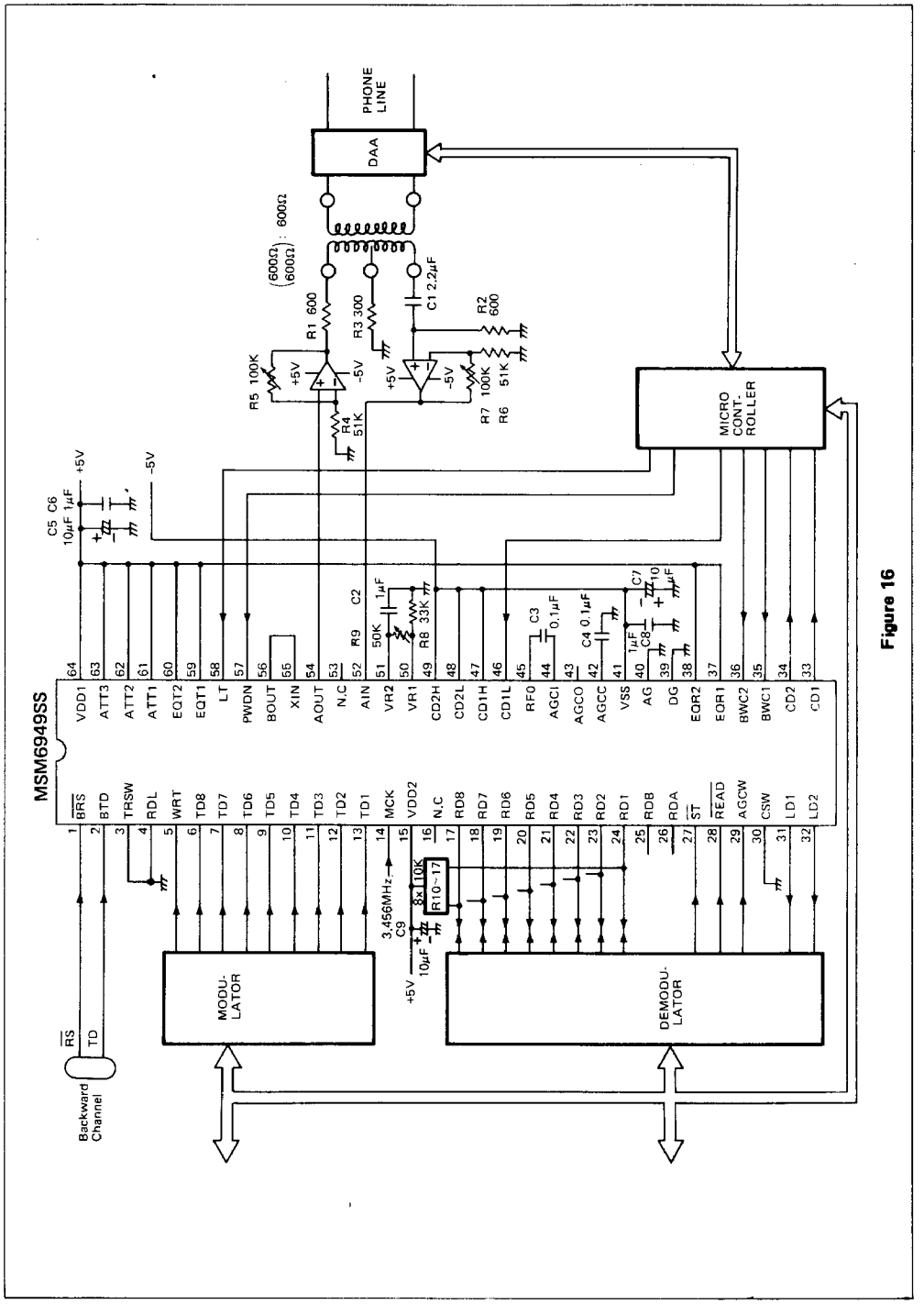


Figure 16