DATA SHEET

SKY77324: iPAC™ PAM for Quad-Band GSM / GPRS

Applications

- Quad-band cellular handsets encompassing
  - Class 4 GSM850/900
  - Class 1 DCS1800 PCS1900
  - Class 12 GPRS multi-slot operation

Features

- Low input power range 0 to 6 dBm
- High efficiency
  - GSM850 49%
  - GSM900 53%
  - DCS 53%
  - PCS 53%
- Internal I_{CC} sense resistor for PAC
- Closed loop iPAC or open loop operation with external PAC circuit
- Input/Output matching 50 Ω internal (with DC blocking)
- 22-pin package
  - Small outline 6 mm x 8 mm
  - Low profile 1.2 mm maximum
- Low APC current 20 µA
- Gold plated, lead-free contacts

The SKY77324 Power Amplifier Module (PAM) is designed in a low profile (1.2 mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation. The PAM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of separate GSM850/900 PA and DCS1800/PCS1900 PA blocks, impedance-matching circuitry for 50 Ω input and output impedances, and a Power Amplifier Control (PAC) block with an internal current-sense resistor. The custom CMOS integrated circuit provides the internal PAC function and interface circuitry. Fabricated onto a single Gallium Arsenide (GaAs) die, one Heterojunction Bipolar Transistor (HBT) PA block supports the GSM850/900 bands and the other supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current. The GaAs die, the Silicon (Si) die, and the passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

RF input and output ports of the SKY77324 are internally matched to a 50 Ω load to reduce the number of external components for a quad-band design. Extremely low leakage current (2.5 µA, typical) of the dual PA module maximizes handset standby time. The SKY77324 also contains band-select switching circuitry to select GSM (logic 0) or DCS/PCS (logic 1) as determined from the Band Select (BS) signal. In Figure 1, below, the BS pin selects the PA output (DCS/PCS OUT or GSM850/900 OUT) and the Analog Power Control (VAPC) controls the level of output power.

VBATT and VSENSE pins connect to an internal current-sense resistor and interface to an integrated power amplifier control (iPAC™) function, which is insensitive to variations in temperature, power supply, and process. The PAC ENABLE input allows initial turn-on of PAC circuitry to minimize battery drain.

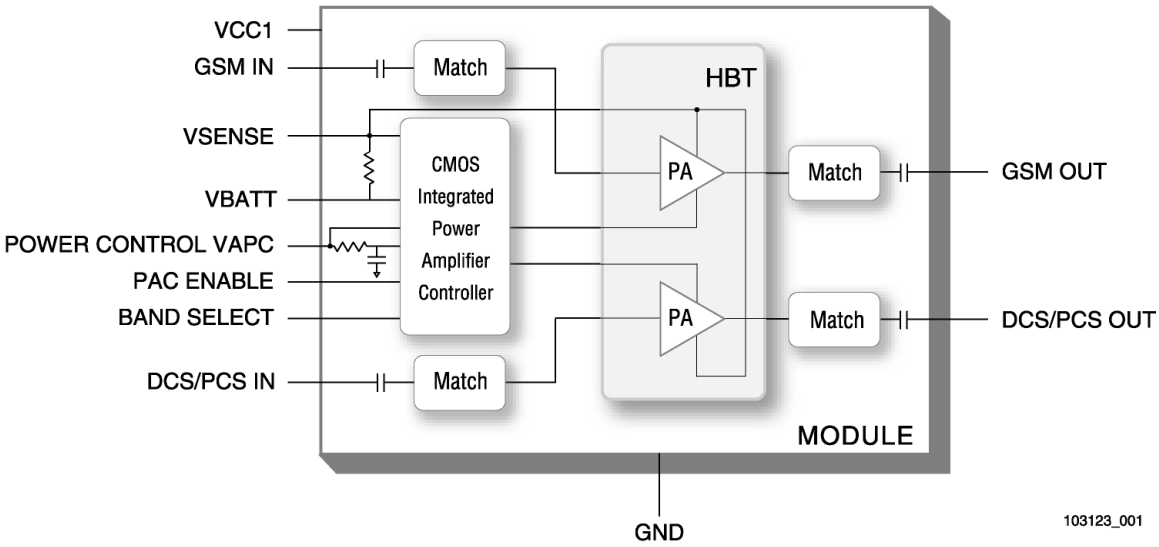


Figure 1. Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the SKY77324 Power Amplifier Module. Table 1 lists the absolute maximum ratings and Table 2 shows the recommended operating conditions. Table 3 lists the electrical characteristics of the SKY77324 for modes GSM850, GSM900, DCS1800, and PCS1900.

Figure 2 is a diagram of a typical SKY77324 application.

The SKY77324 is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields. Detailed information on device dimensions, pin descriptions, packaging and handling can be found in later sections of this data sheet.

Table 1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Power (P_{IN})	—	15	dBm
Supply Voltage (V_{CC}), Standby, $V_{APC} \leq$ 0.3 V, PAC ENABLE $\leq$ 0.2 V	—	7	V
Control Voltage (V_{APC})	–0.5	V_{CC_MAX} – 0.2 (See Table 3)	V
Storage Temperature	–55	+100	°C

Table 2. Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage (V_{CC})	2.9	3.5	4.8V [1]	V
Supply Current (I_{CC})	0	—	2.5 [1]	A
Operating Case Temperature (T_{CASE}) – Package Bottom Surface				
1-Slot (12.5% duty cycle)	–20	—	+100	°C
2-Slot (25.0% duty cycle)	–20	—	+100	
3-Slot (37.5% duty cycle)	–20	—	+85	
4-Slot (50.0% duty cycle)	–20	—	+85	

[1] In open loop operation: For charging conditions with $V_{CC} > 4.8$ V, derate I_{CC} linearly down to 0.5 A, maximum, at $V_{CC} = 5.5$ V.

Table 3. SKY77324 Electrical Specifications [1] *(1 of 9)*

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Units
General							
Supply voltage		V_{CC}	—	2.9	3.5	4.8	V
Power control impedance		Z_{APC}	—	85	100	115	kΩ
PAC ENABLE control voltage	Low	V_{PE}	—	–0.1	—	0.7	V
	High	V_{PE}	—	2.0	—	V_{CC}	
PAC ENABLE current		I_{PE}	$V_{PE} \leq 3.0$ V	—	—	30	µA
Band Select control voltage	Low	V_{BS}	—	–0.1	—	0.5	V
	High	V_{BS}	—	2.0	—	V_{CC}	
Band Select current		I_{BS}	$V_{BS} \leq 3.0$ V	—	—	30	µA
Standby Mode Leakage current		I_Q	$V_{CC} \leq 4.5$ V $V_{APC} \leq 0.3$ V PAC ENABLE ≤ 0.2 V $T_{CASE} = +25$ °C $P_{IN} \leq -60$ dBm	—	2.5	10	µA
Closed Loop V_{APC} Input Filter Bandwidth		$V_{APC\ FBW}$	—	95	135	170	kHz
Closed Loop V_{APC} Threshold		$V_{APC\ THCL}$	—	400	420	460	mV
Open Loop [4] V_{APC} Enable Threshold		$V_{APC\ THOL}$	—	200	—	800	mV

Table 3. SKY77324 Electrical Specifications [1] *(2 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
GSM850 Mode (f = 824 to 849 MHz and P_{IN} = 0 to 6dBm)						
Frequency range	f		824	—	849	MHz
Input power	P_{IN}		0	—	6	dBm
Analog power control voltage	V_{APC}		0.4	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 34.5 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	45	49	—	%
2nd to 13th harmonics	2fo to 13fo	BW = 3 MHz 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	–25	–10	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	34.5	35.0	—	dBm
	P_{OUT} MAX LOW VOLTAGE	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	32.0	34.0	—	
	P_{OUT} MAX HIGH VOLTAGE	V_{CC} = 4.5 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	32.0	35.7	—	
Input VSWR	Γ_{IN}	P_{OUT} = 6.5 to 34.5 dBm, controlled by V_{APC}	—	1.5:1	2.0:1	—
Forward isolation	P_{OUT} STANDBY	P_{IN} = 6 dBm V_{APC} = 0.3 V PAC ENABLE ≤ 0.2 V	—	–40	–35	dBm
	P_{OUT} ENABLED	P_{IN} = 6 dBm V_{APC} ≤ 0.35 V PAC ENABLE ≥ 2.0V	—	–30	–16	
Open Loop[4] Switching time	τ_{RISE}	Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +6.5 dBm	—	1.2	2.0	µs
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +20.0 dBm	—	1.0	1.3	
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +34.5 dBm	—	1.4	1.7	

Table 3. SKY77324 Electrical Specifications [1] *(3 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_O + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	–84	–82	dBm
		At f_O + 10 MHz RBW = 100 kHz V_{CC} = 3.5 V 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	–81	–76	dBm
		At 1805 to 1880 MHz RBW = 100 kHz V_{CC} = 3.5 V 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	–106	–84	dBm
Coupling of Fundamental, 2nd, and 3rd harmonics from the GSM band into the DCS/PCS band	f_O	Measured at the DCS/PCS output –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	–8	0	dBm
	$2f_O$		—	–30	–20	
	$3f_O$		—	–30	–20	
Power control dynamic range	P_{CDR}	—	30	50		dB
Power control variation [5] (Control level 5–15) 3.2 ≤ V_{CC} ≤ 4.5	P_{CV}	P_{OUT} +14.5 to +34.5 dBm, +25 °C	–0.8	—	+0.8	dB
		P_{OUT} +14.5 to +34.5 dBm	–1.5	—	+1.4	
Power control variation [5] (Control level 16–19)	P_{CV}	P_{OUT} +6.5 to +12.5 dBm, +25 °C	–1.2	—	+1.2	dB
		P_{OUT} +6.5 to +12.5 dBm	–2.0	—	+2.0	
Power control slope	P_{CS}	6.5 to 34.5 dBm	2	—	300	dB/V
Closed loop bandwidth	B_{CL}	V_{APC} = 1.0 V	—	700	—	kHz
Loop phase margin	P_M	V_{APC} = 1.0 V	50	65	—	deg.

Table 3. SKY77324 Electrical Specifications [1] *(4 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
GSM900 Mode (f = 880 to 915 MHz and P_{IN} = 0 to 6 dBm)						
Frequency range	f	—	880	—	915	MHz
Input power	P_{IN}	—	0	—	6	dBm
Analog power control voltage	V_{APC}	—	0.4	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 34.5 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	49	53	—	%
2nd to 13th harmonics	2f0 to 13f0	BW = 3 MHz 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	–30	–10	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	34.5	35.0	—	dBm
	P_{OUT} MAX LOW VOLTAGE	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	32.0	33.0	—	
	P_{OUT} MAX HIGH VOLTAGE	V_{CC} = 4.5 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	32.0	36.3	—	
Input VSWR	Γ_{IN}	P_{OUT} = 6.5 to 34.5 dBm controlled by V_{APC}	—	1.5:1	2.0:1	—
Forward isolation	P_{OUT} STANDBY	P_{IN} = 6 dBm V_{APC} = 0.3 V PAC ENABLE ≤ 0.2 V	—	–40	–35	dBm
	P_{OUT} ENABLED	P_{IN} = 6 dBm V_{APC} ≤ 0.35 V PAC ENABLE ≥ 2.0 V	—	–30	–16	
Open Loop[4] Switching time	τ_{RISE}	Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +6.5 dBm	—	1.2	2.0	µs
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +20.0 dBm	—	1.0	1.3	
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +34.5 dBm	—	1.4	1.7	

Table 3. SKY77324 Electrical Specifications [1] *(5 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_O + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	–84	–82	dBm
		At f_O + 10 MHz RBW = 100 kHz V_{CC} = 3.5 V 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	–81	–76	
		At 1805 to 1880 MHz RBW = 100 kHz V_{CC} = 3.5 V 6.5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	–106	–84	
Coupling of Fundamental, 2nd, and 3rd harmonics from the GSM band into the DCS/PCS band	f_O	Measured at the DCS/PCS output, –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	–12	0	dBm
	$2f_O$		—	–30	–20	
	$3f_O$		—	–30	–20	
Power control dynamic range	P_{CDR}	—	30	50	—	dB
Power control variation [5] (Control level 5–15) 3.2 ≤ V_{CC} ≤ 4.5	P_{CV}	P_{OUT} +14.5 to +34.5 dBm, +25 °C	–0.8	—	+0.8	dB
		P_{OUT} +14.5 to +34.5 dBm	–1.5	—	+1.4	
Power control variation [5] (Control level 16–19)	P_{CV}	P_{OUT} +6.5 to +12.5 dBm, +25 °C	–1.2	—	+1.2	dB
		P_{OUT} +6.5 to +12.5 dBm	–2.0	—	+2.0	
Power control slope	P_{CS}	6.5 to 34.5 dBm	2	—	300	dB/V
Closed loop bandwidth	B_{CL}	V_{APC} = 1.0 V	—	700	—	kHz
Loop phase margin	P_M	V_{APC} = 1.0 V	50	65	—	deg.

Table 3. SKY77324 Electrical Specifications [1] *(6 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
DCS1800 Mode (f = 1710 to 1785 MHz and P_{IN} = 0 to 6 dBm)						
Frequency range	f	—	1710	—	1785	MHz
Input power	P_{IN}	—	0	—	6	dBm
Analog power control voltage	V_{APC}	—	0.4	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 32.0 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	45	53	—	%
	$PAE_{LOW\ INPUT}$	V_{CC} = 3.5 V P_{OUT} = 32.0 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C P_{IN} = –2 dBm	—	51	—	
2nd to 7th harmonics	2fo to 7fo	BW = 3 MHz 1.5 dBm ≤ P_{OUT} ≤ 32.0 dBm	—	–22	–10	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	32.0	33.0	—	dBm
	$P_{OUT\ MAX\ LOW\ INPUT}$	V_{CC} = 3.5 V T_{CASE} = +25 °C P_{IN} = –2 dBm	—	32.1	—	
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	29.0	31.0	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.5 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	29.0	34.3	—	
Input VSWR	Γ_{IN}	P_{OUT} = 1.5 to 32.0 dBm controlled by V_{APC}	—	1.5:1	2.0:1	—
Forward isolation	$P_{OUT\ STANDBY}$	P_{IN} = 6 dBm V_{APC} = 0.3 V PAC ENABLE ≤ 0.2 V	—	–40	–35	dBm
	$P_{OUT\ ENABLED}$	P_{IN} = 6 dBm V_{APC} ≤ 0.35 V PAC ENABLE ≥ 2.0 V	—	–40	–20	

Table 3. SKY77324 Electrical Specifications [1] *(7 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Open Loop [4] Switching time	τ_{RISE}	Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +1.5 dBm	—	0.5	3.0	µs
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +20.0 dBm	—	0.8	1.1	
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +32.0 dBm	—	1.2	1.5	
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_O + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 1.5 dBm ≤ P_{OUT} ≤ 32.0 dBm T_{CASE} = +25 °C	—	–82	–80	dBm
		At 925 to 960 MHz RBW = 100 kHz V_{CC} = 3.5 V 1.5 dBm ≤ P_{OUT} ≤ 32.0 dBm T_{CASE} = +25 °C	—	–97	–87	
Power control dynamic range	P_{CDR}	—	35	50	—	dB
Power control variation [5] (Control level 0–8) 3.2 V ≤ V_{CC} ≤ 4.5 V	P_{CV}	P_{OUT} +15.5 to +32.0 dBm, +25 °C	–1.0	—	+1.0	dB
		P_{OUT} +15.5 to +32.0 dBm	–1.6	—	+1.6	
Power control variation [5] (Control level 9–13)	P_{CV}	P_{OUT} +5.5 to +13.5 dBm, +25 °C	–1.8	—	+1.8	dB
		P_{OUT} +5.5 to +13.5 dBm	–3.3	—	+3.3	
Power control variation [5] (Control level 14–15)	P_{CV}	P_{OUT} +1.5 to +3.5 dBm, +25 °C	–3.0	—	+3.0	dB
		P_{OUT} +1.5 to +3.5 dBm	–4.5	—	+4.5	
Power control slope	P_{CS}	1.5 to 32.0 dBm	—	—	400	dB/V
Closed loop bandwidth	B_{CL}	V_{APC} = 1.0 V	—	500	—	kHz
Loop phase margin	P_M	V_{APC} = 1.0 V	75	—	—	deg.

Table 3. SKY77324 Electrical Specifications [1] *(8 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
PCS1900 Mode (f = 1850 to 1910 MHz and P_{IN} = 0 to 6 dBm)						
Frequency range	F	—	1850		1910	MHz
Input power	P_{IN}	—	0		6	dBm
Analog power control voltage	V_{APC}	—	0.4		2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 32.0 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	45	53	—	%
	$PAE_{LOW\ INPUT}$	V_{CC} = 3.5 V P_{OUT} = 32.0 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C P_{IN} = –2 dBm	—	51	—	
2nd to 7th harmonics	2fo to 7fo	BW = 3 MHz 1.5 dBm ≤ P_{OUT} ≤ 32.0 dBm	—	–18	–10	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	32.0	33.0	—	dBm
	$P_{OUT\ MAX\ LOW\ INPUT}$	V_{CC} = 3.5 V T_{CASE} = +25 °C P_{IN} = –2 dBm	—	32.5	—	
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	29.0	31.0	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.5 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	29.0	34.1	—	
Input VSWR	Γ_{IN}	P_{OUT} = 1.5 to 32.0 dBm controlled by V_{APC}	—	1.5:1	2.0:1	—
Forward isolation	$P_{OUT\ STANDBY}$	P_{IN} = 6 dBm V_{APC} = 0.3 V PAC ENABLE ≤ 0.2 V	—	–40	–35	dBm
	$P_{OUT\ ENABLED}$	P_{IN} = 6 dBm V_{APC} ≤ 0.35 V PAC ENABLE ≥ 2.0 V	—	–40	–20	

Table 3. SKY77324 Electrical Specifications [1] *(9 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Open Loop[4] Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +1.5 dBm	—	0.5	3.0	µs
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +20.0 dBm	—	0.8	1.1	
		Time from P_{OUT} = –10 dBm to within 0.5 dBm of P_{OUT} = +32.0 dBm	—	1.2	1.5	
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_O + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 1.5 dBm ≤ P_{OUT} ≤ 32.0 dBm T_{CASE} = +25 °C	—	–82	–80	dBm
		At 869 to 894 MHz RBW = 100 kHz V_{CC} = 3.5 V 1.5 dBm ≤ P_{OUT} ≤ 32.0 dBm T_{CASE} = +25 °C	—	–97	–87	
Power control dynamic range	P_{CDR}	—	35	50	—	dB
Power control variation [5] (Control level 0–8) 3.2 V ≤ V_{CC} ≤ 4.5 V	P_{CV}	P_{OUT} +15.5 to +32.0 dBm, +25 °C	–1.0	—	+1.0	dB
		P_{OUT} +15.5 to +32.0 dBm	–1.6	—	+1.6	
Power control variation [5] (Control level 9–13)	P_{CV}	P_{OUT} +5.5 to +13.5 dBm, +25 °C	–1.8	—	+1.8	dB
		P_{OUT} +5.5 to +13.5 dBm	–3.3	—	+3.3	
Power control variation [5] (Control level 14–15)	P_{CV}	P_{OUT} +1.5 to +3.5 dBm, +25 °C	–3.0	—	+3.0	dB
		P_{OUT} +1.5 to +3.5 dBm	–4.5	—	+4.5	
Power control slope	P_{CS}	1.5 to 32.0 dBm	—	—	400	dB/V
Closed loop bandwidth	B_{CL}	V_{APC} = 1.0 V	—	500	—	kHz
Loop phase margin	P_M	V_{APC} = 1.0 V	75	—	—	deg.

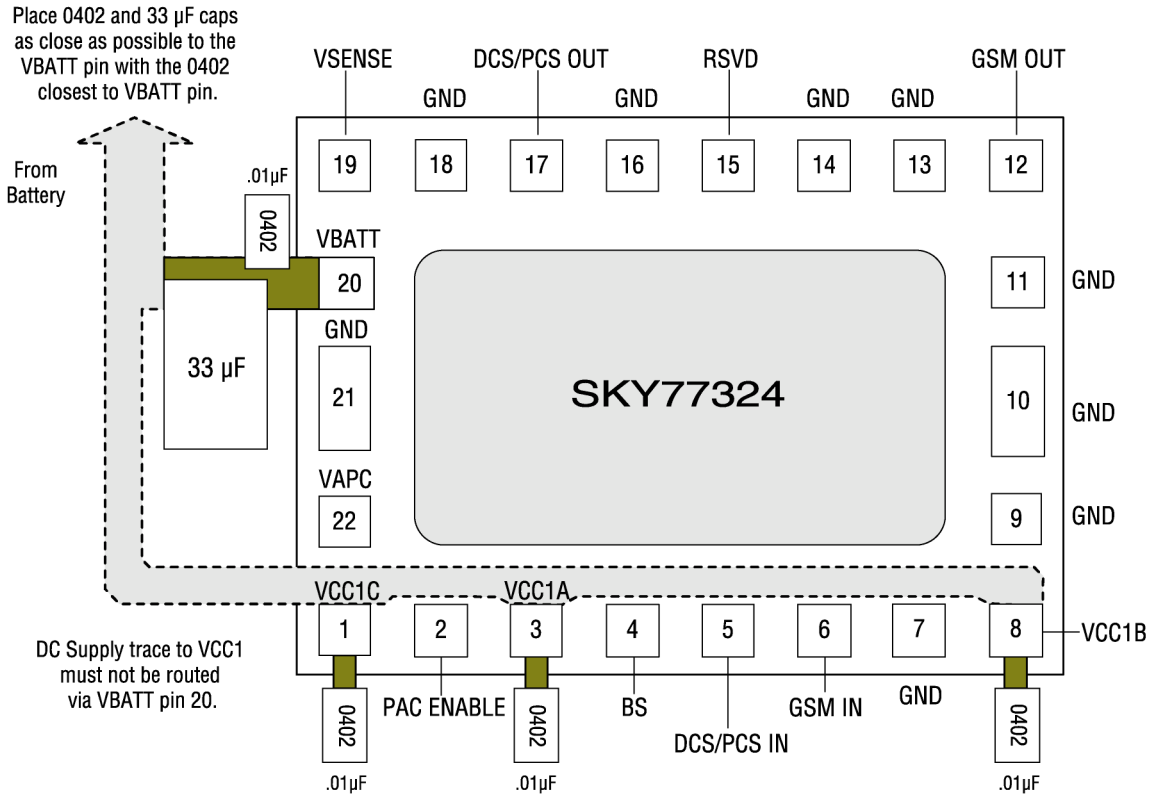
[1] Unless specified otherwise:
T_{CASE} = –20 °C to maximum operating temperature (see Table 2)
RL = 50 Ω
pulsed operation with pulse width ≤ 1154 µs and duty cycle ≤ 2:8
V_{CC} = 2.9 V to 4.8 V.

[2] I_{CC} = 0A to xA, where x = current at P_{OUT} = 34.5 dBm, 50 Ω load, and V_{CC} = 3.5 V.

[3] I_{CC} = 0A to xA, where x = current at P_{OUT} = 32.0 dBm, 50 Ω load, and V_{CC} = 3.5 V.

[4] This device has an Open Loop mode that allows bypassing of the internal PAC circuitry. See the Technical Information section at end of this document for further information.

[5] Power control variation is measured by comparing power obtained at a specified control voltage over all conditions, against the power obtained with the same control voltage at nominal conditions. For this module, nominal conditions are defined as
T = 25 °C
V_{CC} = 3.5 V
P_{IN} = 3 dBm
Frequency = mid-band



NOTES:
1. The value of 33 µF cap depends on the noise level on the phone board.
2. Depending on phone board noise level, not all 0402 and 0.01 µF caps may be needed.
3. Ensure sufficient numbers of vias connect VBATT pin to battery trace.
4. VBATT trace should be ≥ 1.0 mm.
5. Ensure sufficient numbers of vias connect VCC1A, B, and C to battery trace.
6. VCC1A, B, and C trace widths should be ≥ 0.25 mm.
7. Ground terminals of all bypass caps are connected to ground plane with vias.
8. Dotted traces can be routed in the inner layers.

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Figure 2. Typical SKY77324 PAM Application

Package Dimensions and Pin Description

Figure 3 is a mechanical diagram of the pad layout for the SKY77324, a 22-pin leadless quad-band PA module. Figure 4 provides a recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50 Ω terminals.

Figure 5 shows the device pin configuration and Table 4 lists the pin names and signal descriptions. The pin numbering convention starts with pin 1 at the upper left, as indicated in Figure 5, and increments counter-clockwise around the package. Figure 6 interprets typical case markings.

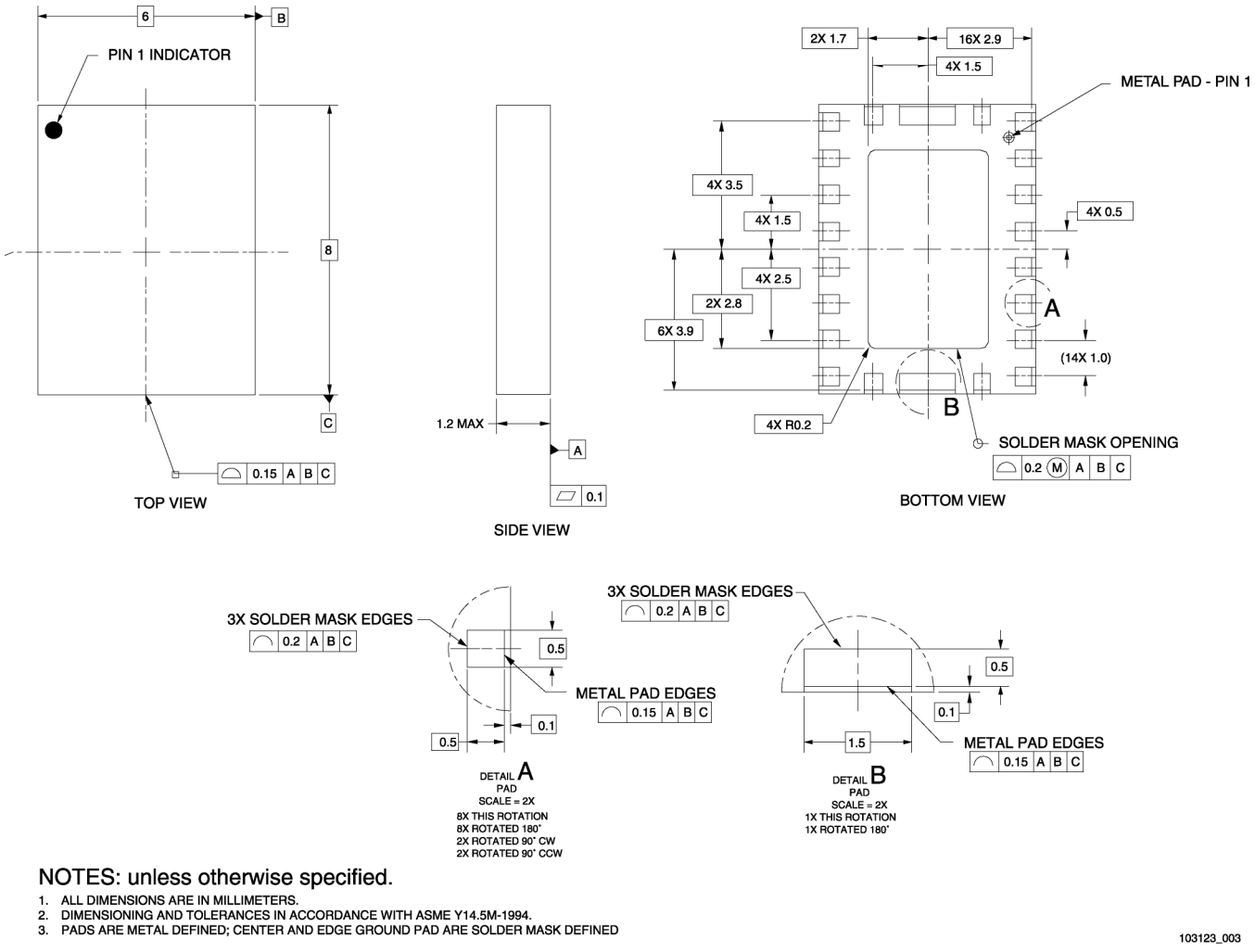


Figure 3. SKY77324 PAM Package Dimensions—22-Pin Leadless (All Views)

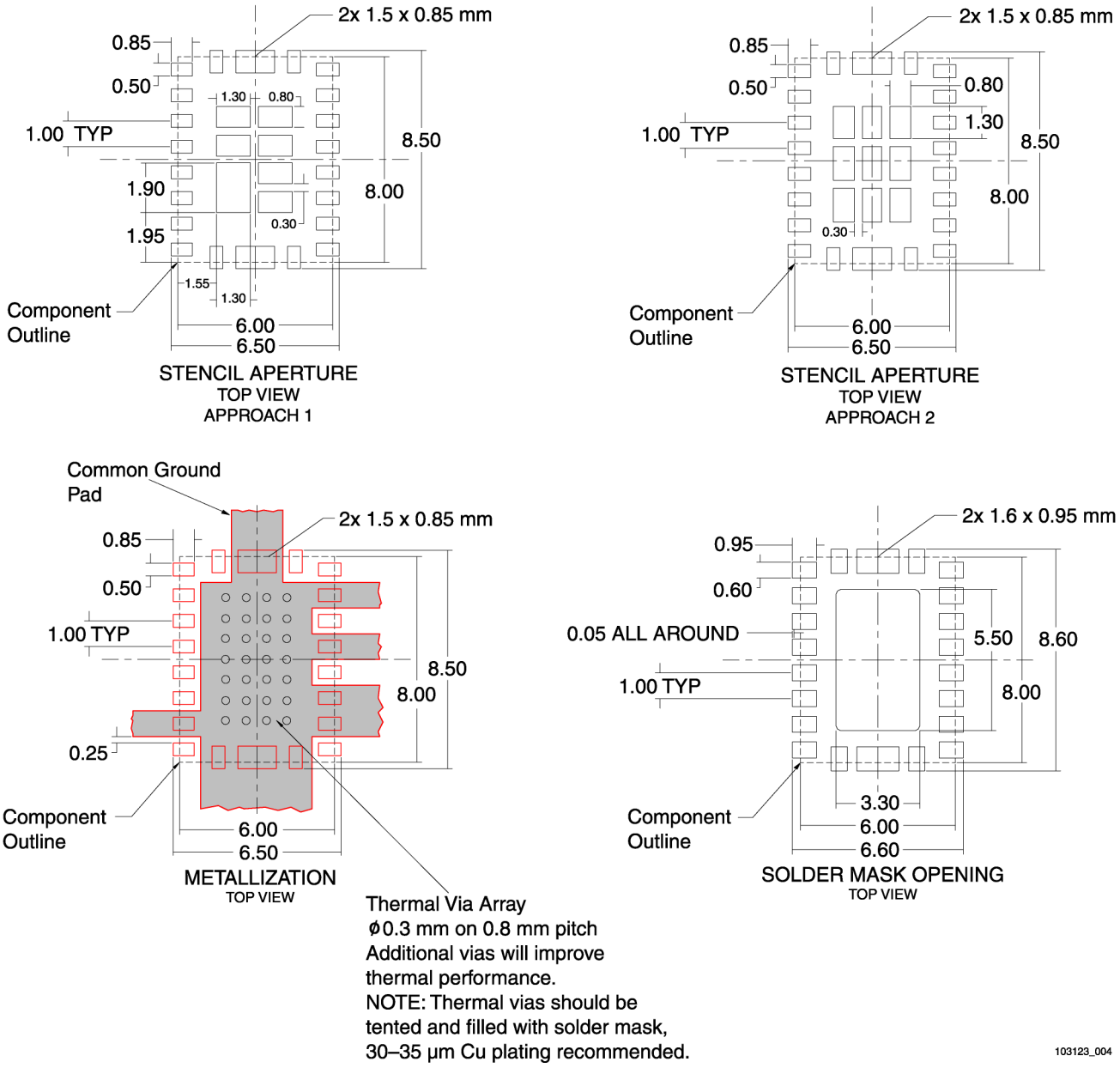


Figure 4. Phone Board Layout Footprint for 6 x 8 mm Package – SKY77324 Specific

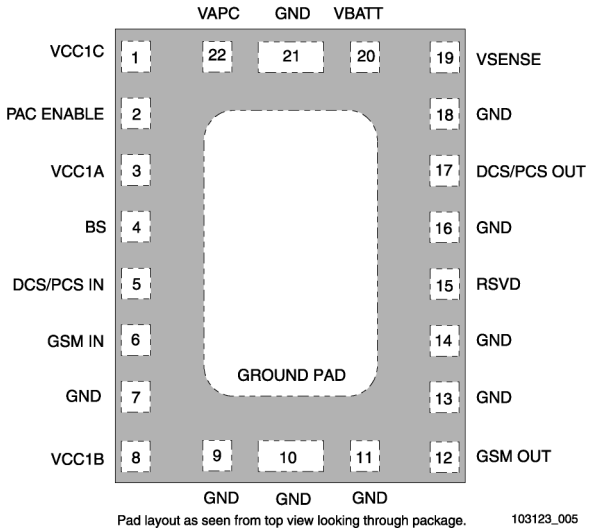


Figure 5. SKY77324 PAM Pin Configuration—22-Pin Leadless (Top View)

Table 4. SKY77324 Pin Names and Signal Descriptions

Pin	Name	Description
1	VCC1C	VCC (to PAC)
2	PAC ENABLE	Closed loop PAC mode CMOS enable
3	VCC1A	VCC (to GSM 1st stage, DCS 1st stages)
4	BS	Band Select
5	DCS/PCS IN	RF input 1710–1910 MHz
6	GSM IN	RF input 824–915 MHz
7	GND	RF and DC Ground
8	VCC1B	VCC (to GSM 2nd stage, DCS 2nd stage)
9	GND	RF and DC Ground
10	GND	RF and DC Ground
11	GND	RF and DC Ground
12	GSM OUT	RF Output 824–915 MHz
13	GND	RF and DC Ground
14	GND	RF and DC Ground
15	RSVD	Reserved
16	GND	RF and DC Ground
17	DCS/PCS OUT	RF Output 1710–1910 MHz
18	GND	RF and DC Ground
19	VSENSE	Voltage output of low side of internal sense resistor (DO NOT CONNECT IN CLOSED LOOP MODE.)
20	VBATT	Battery input to high side of internal sense resistor
21	GND	RF and DC Ground
22	VAPC	Power Control Bias Voltage
GND PAD (23)	GND	Ground Pad, bottom

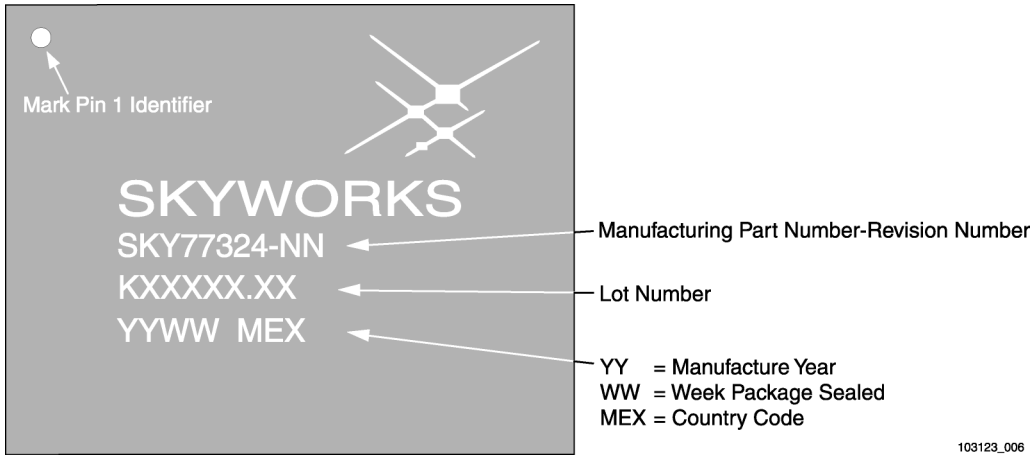


Figure 6. Typical Case Markings

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77324 is currently qualified for MSL3/240 °C. Demonstration of the SKY77324 to withstand an MSL3/250 °C solder reflow is pending completion of qualification tests.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 250 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 250 °C for more than 10 seconds.

For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD-020B*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Application Note: Tape and Reel, Document Number 101568.*

Electrostatic Discharge Sensitivity

The SKY77324 is a Class I device. Figure 7 lists the Electrostatic Discharge (ESD) immunity level for each pin of the SKY77324 module. The numbers specify the ESD threshold levels for each pin where the I-V curve between the pin and ground starts to show degradation.

ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If the magnitude of ESD damage threshold is found to consistently exceed 2000 volts, this so is indicated. If the ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

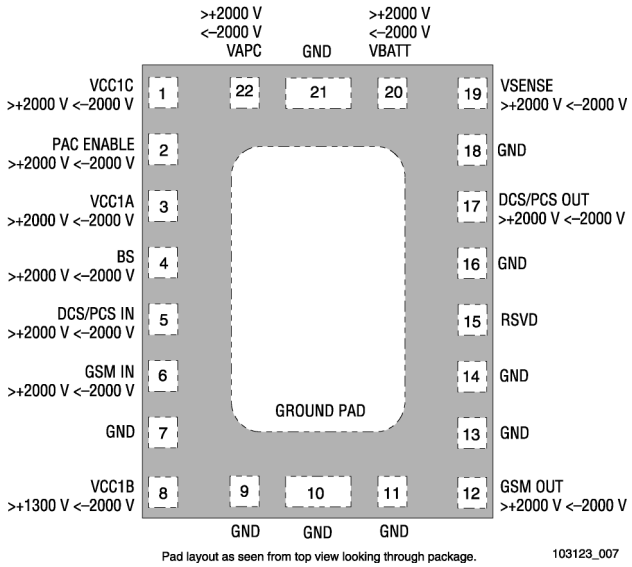


Figure 7. ESD Sensitivity Areas (Top View)

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks’ most stringent criteria fail devices as soon as the pin begins to show any degradation on a curve tracer. To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in

Table 5.

Table 5. Precautions for Handling GaAs IC based Products to Avoid ESD Induced Damage

Personnel Grounding	Facility
Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges	Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation	**Protective Packaging & Transportation**
Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors	Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

Technical Information

Closed loop control of the amplifier is enabled when PAC ENABLE is driven to logic high. The PA collector current will then be directly proportional to the V_{APC} input voltage over the range of 400 mV to 2.1 V.

To meet the GSM power versus time mask and switching transient requirements the PAM must be provided with a DAC ramp profile on the V_{APC} input as well as proper timing on digital controls for the PAC circuitry.

Note: Please refer to 3GPP TS 51.010-1: Mobile Station (MS) conformance specification. All GSM specifications are now the responsibility of 3GPP. The standards are available at http://www.3GPP.org.

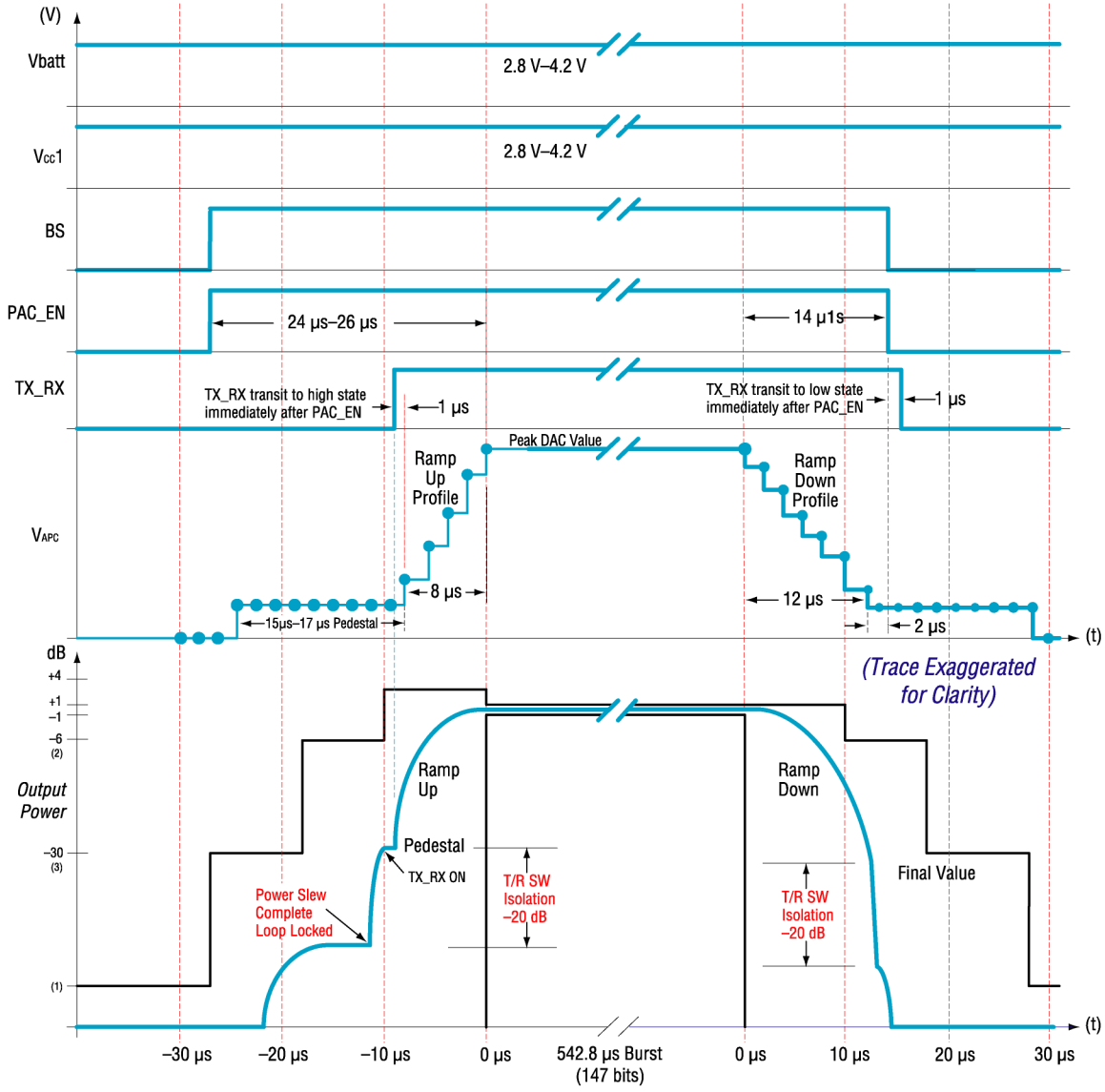
The SKY77324 has been designed to comply with interface requirements and DAC resolution of leading base band devices. The ramp profile typically consists of a pedestal voltage, 10–16 discrete voltage steps on the rising edge of the burst, a constant region, 10–16 steps on the falling edge, and a final voltage. Typically, the user defines the start, stop, and 10–16 percentage values for each rising and falling edge, which are then applied as discrete voltages at the V_{APC} input. For the SKY77324, generally the same profile, scaled in amplitude, is used for all frequencies and power control levels. The ultimate purpose is to keep the RF output power ramp within the time mask and to maintain acceptable spectral limits at specified offset frequencies. The V_{APC} input has an internal reconstruction filter such that external resistors or capacitors are unnecessary on the phone board or the test fixture.

Figure 8 represents the dynamic characteristics of the RF output burst power that results from the ramp profile delivered by the DAC to the V_{APC} input. The transmit power must not exceed the given limits at the time specified relative to the start and end of the data burst. Additional requirements are placed on spectral components generated by switching transients. Ramping at high rates will result in components that violate these spectral limits. A ramp control signal must be applied to the V_{APC} pin, which results in the desired power ramp response. The log relationship of V_{APC} to P_{OUT}, along with the finite bandwidth and potential slew rate limitations of the feedback loop, results in a complex mapping of the ramp profile to the actual output power. Careful attention is required in generating the input waveform which results in the desired output response.

Figure 9 shows an example of the Skyworks PAM test setup for evaluation of RF performance with various ramp profiles. The user's test setup may also include a TX/RX switch and a diplexer in the output signal path. Alternatively, the SKY77324 PAM may be installed in a phone board.

Figure 10 shows an example Skyworks software interface for the setup in Figure 9 that can be used to create a recommended DAC ramp profile. This profile is loaded from the computer into the Skyworks emulator board during test. The software also handles the required PAC Enable and TX_RX control signal timing.

Figure 11 and Figure 12 show the GSM and DCS/PCS calibration screens, respectively, called up from the ramp profile interface in Figure 10. These calibrations, done for each PAM, generate an output power versus V_{APC} curve from sample data. Points from this curve are combined with the ramp coefficients to generate the DAC ramp during handset operation or test.



(1)	For GSM850 / EGSM	–59 dBc or –36 dBm, whichever is higher.
	For DCS1800/PCS1900	–48 dBc or –48 dBm, whichever is higher.
(2)	For GSM850 / EGSM	–4 dBc for power control level 16, –2 dBc for power control level 17, –1 dBc for power control level 18 and 19.
	For DCS1800/PCS1900	–4 dBc for power control level 11, –2 dBc for power control level 12, –1 dBc for power control level 13, 14, 15.
(3)	For GSM850 / EGSM	–30 dBc or –17 dBm, whichever is higher.
	For DCS1800/PCS1900	–30 dBc or –20 dBm, whichever is higher.

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Figure 8. Example of PAM Recommended Timing Diagram

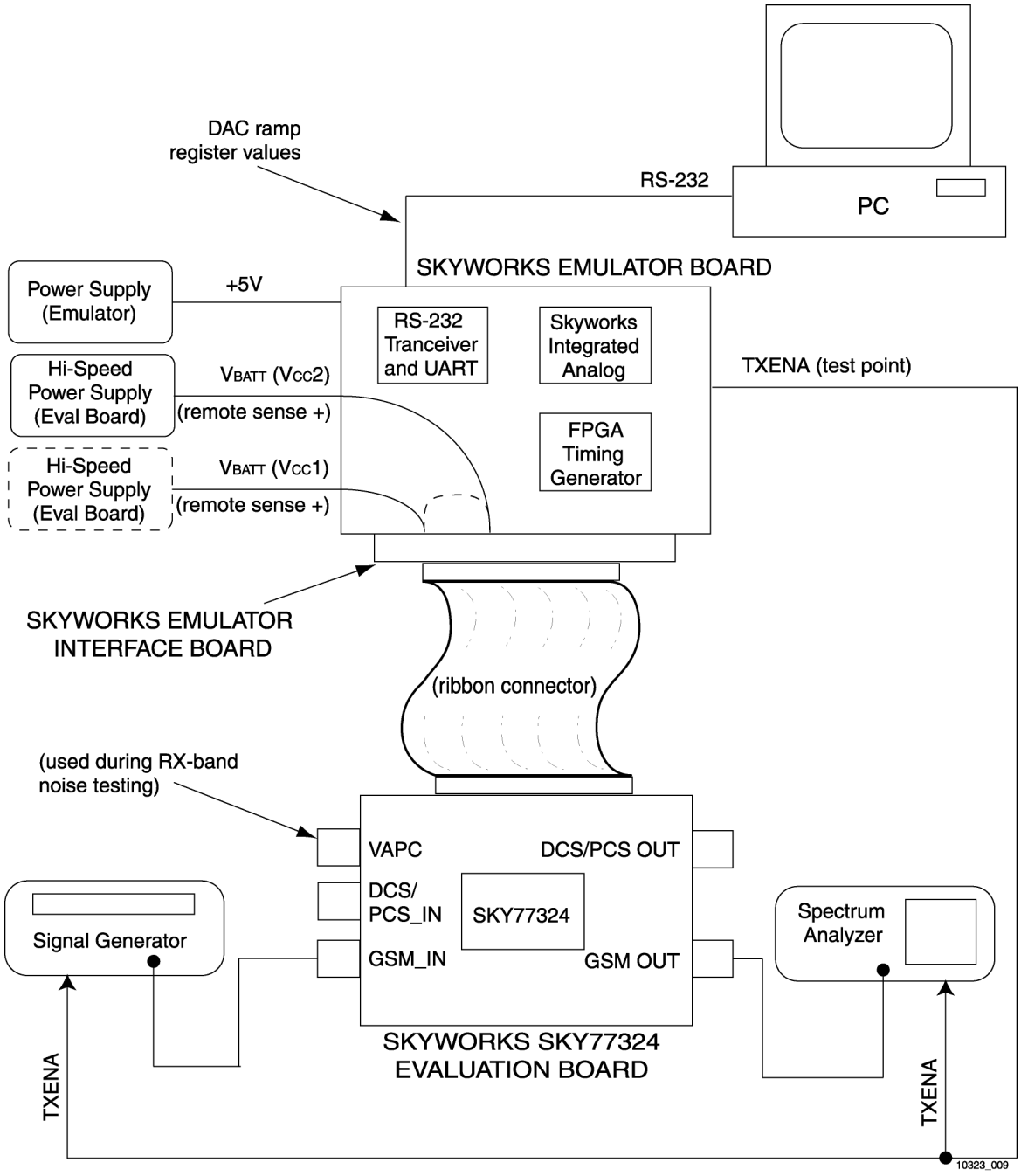

Figure 9. PAM Evaluation Test Setup.

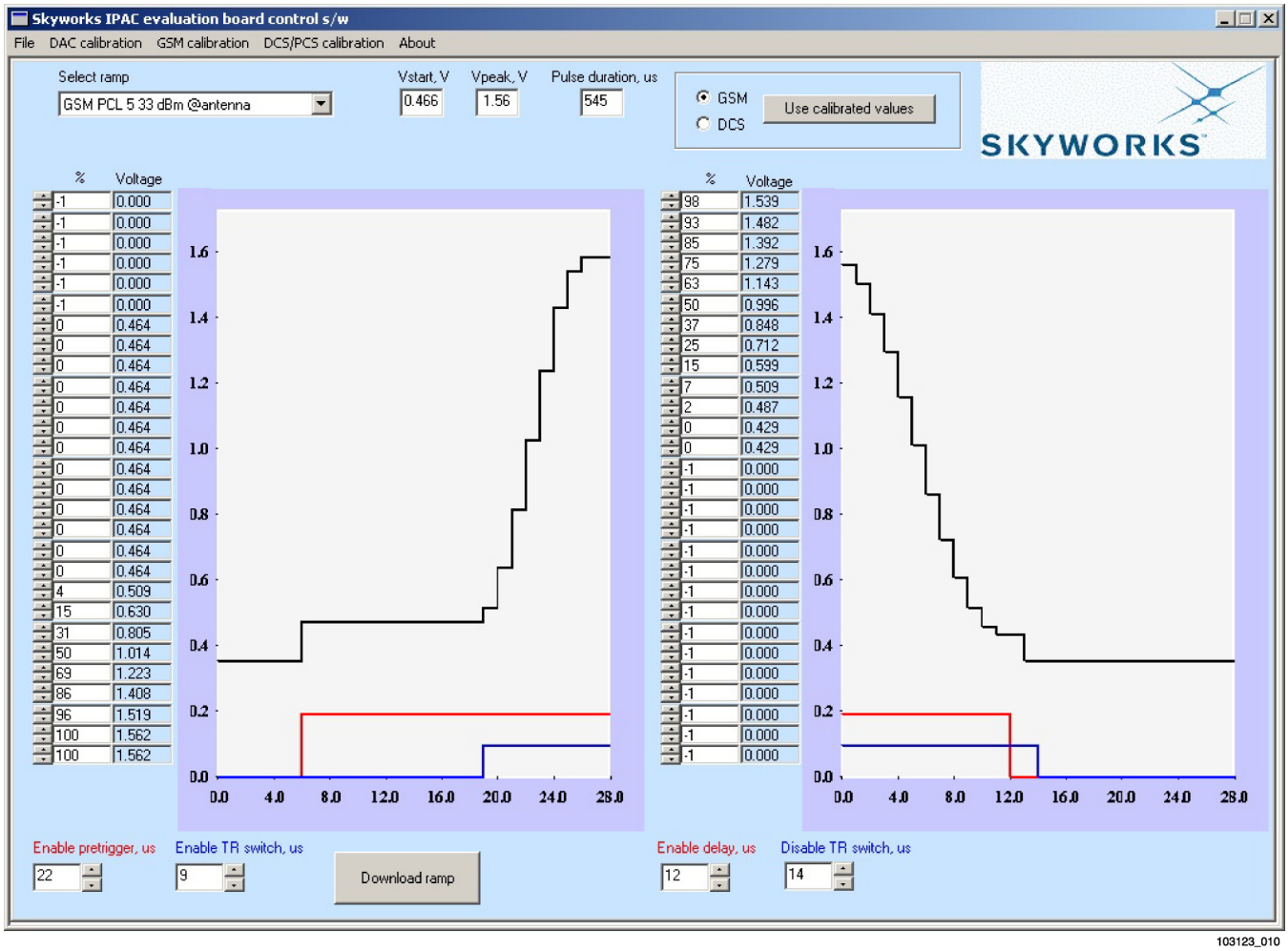

Figure 10. Example of DAC Ramp Profile Generation.

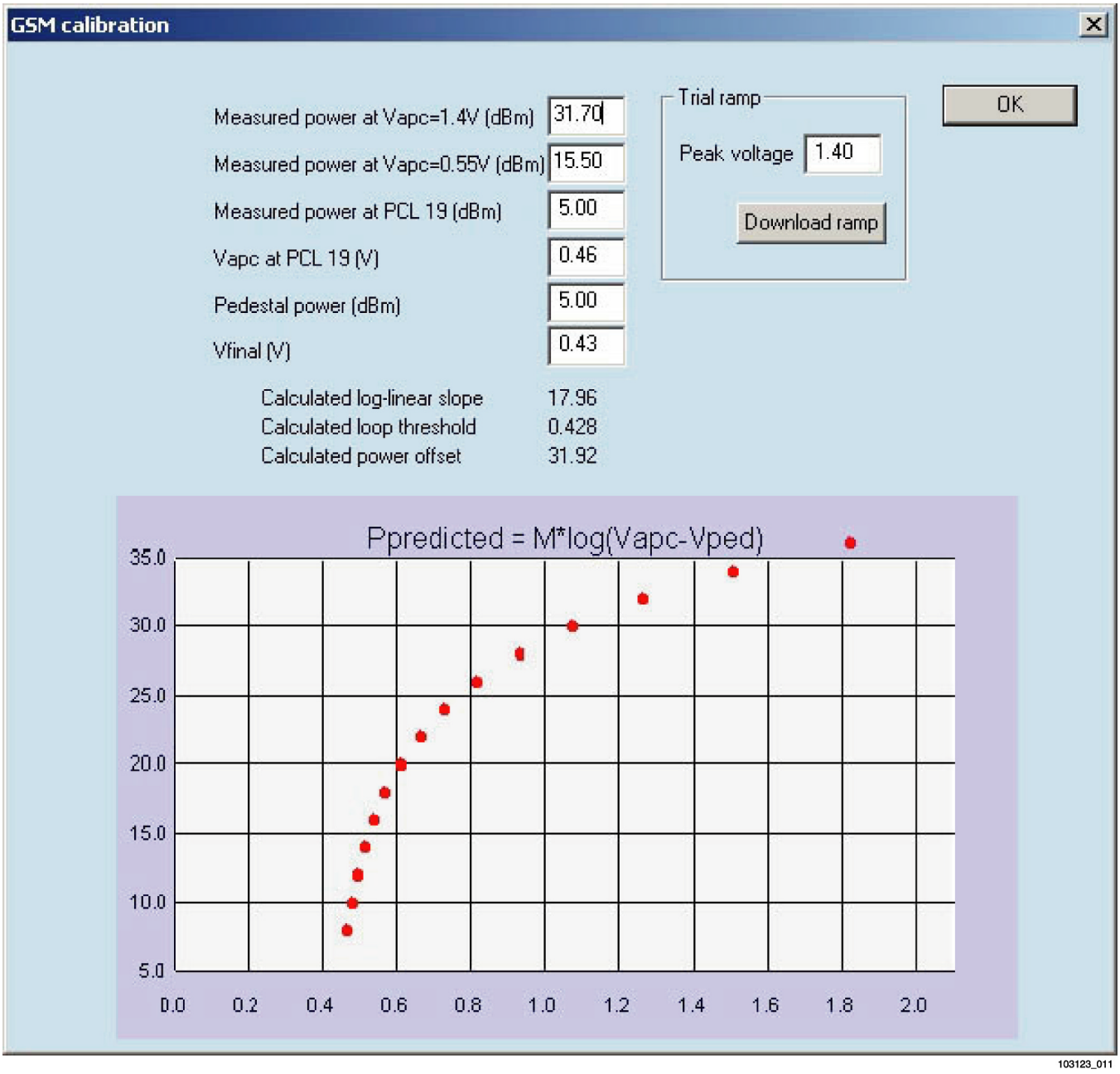

Figure 11. Example of GSM Calibration Screen

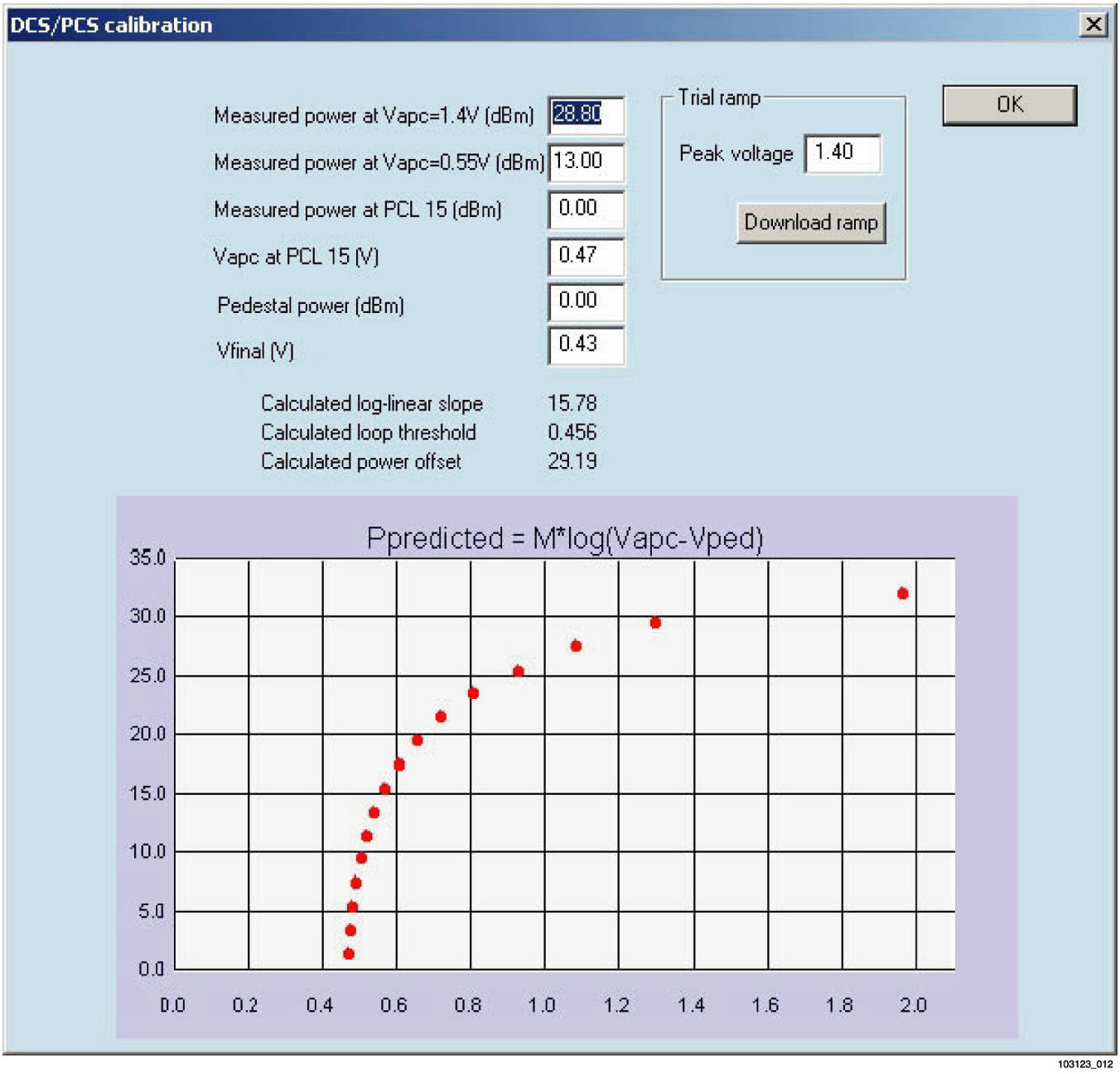

Figure 12. Example of DCS/PCS Calibration Screen

Open Loop Control Mode

With PAC ENABLE at a logic low, the voltage applied to V_{APC} is buffered and applied directly to the bases of the RF devices. This mode of operation provides backward compatibility with the existing amplifier designs and allows for various test scenarios. As with previous designs, an active clamp acts as a protection mechanism limiting the maximum voltage that can be applied to the base of the RF devices. This clamp voltage decreases with increasing supply voltage.

The enable threshold on the V_{APC} input for open loop operation exhibits a wide tolerance, which may vary from 200 mV to 800 mV. When enabled in Open Loop mode, the internal PAC circuitry (V-I converter and integrator) is placed in standby.

Ordering Information

Model Number	Manufacturing Part Number	Package	Operating Temperature
SKY77324	SKY77324	6 x 8 x 1.2 mm	–20 °C to +100 °C

Revision History

Revision	Level	Date	Description
A		September 18, 2003	Initial Release
B		September 29, 2003	Revise: Table 3
C		January 7, 2004	Revise: Table 3

References

Application Note: Tape and Reel, Document Number 101568

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

Application Brief: iPAC™ GSM Transmitter Timing, Calibration and Baseband Control, Document Number 103138

Application Note: SKY77324 Evaluation Board Information, Document Number 103195

JEDEC Standard J–STD–020B

3GPP TS 51.010-1; Mobile Station (MS) Conformance Specification (http://www.3GPP.org)