



# 1 of 2:4 Differential Clock/Data Fanout Buffer

## Features

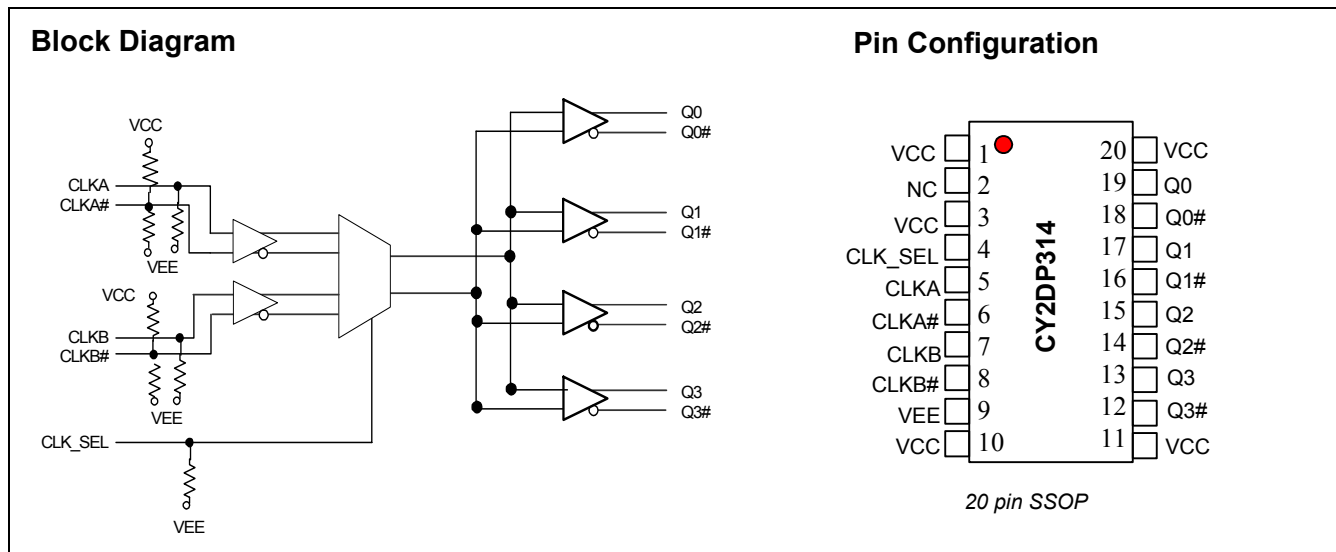
- Four ECL/PECL differential outputs
- One ECL/PECL differential or single-ended inputs (CLKA)
- One HSTL differential or single-ended inputs (CLKB)
- Hot-swappable/-insertable
- 50-ps output-to-output skew
- 150-ps device-to-device skew
- 400-ps propagation delay (typical)
- 0.8-ps RMS period jitter (max.)
- 1.5-GHz operation (2.7-GHz maximum toggle frequency)
- PECL and HSTL mode supply range:  $V_{CC} = 2.5V \pm 5\%$  to  $3.3V \pm 5\%$  with  $V_{EE} = 0V$
- ECL mode supply range:  $V_{EE} = -2.5V \pm 5\%$  to  $-3.3V \pm 5\%$  with  $V_{CC} = 0V$
- Industrial temperature range:  $-40^{\circ}C$  to  $85^{\circ}C$
- 20-pin SSOP package
- Temperature compensation like 100K ECL

## Functional Description

The CY2DP314 is a low-skew, low propagation delay 2-to-4 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz (full swing).

The device features two differential input paths that are multiplexed internally. This mux is controlled by the CLK\_SEL pin. The CY2DP314 may function not only as a differential clock buffer but also as a signal-level translator and fanout on HSTL or LVCMOS /LVTTTL single-ended signal to four ECL/PECL differential loads.

Since the CY2DP314 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2DP314 delivers consistent performance over various platforms.



**Pin Definitions**

Pin	Name	I/O	Type	Description
1,10,11,20,3	VCC	+PWR	Power	Power supply, positive connection
2	NC			No connect
4	CLK_SEL	I,PD	LVC MOS	InPut Clock Select
5	CLKA	I,PD <sup>[1]</sup>	ECL/PECL	Default differential clock input
6	CLKA#	I, PD/PU	ECL/PECL	Default differential clock input
7	CLKB	I,PD	HSTL	Alternate differential clock input
8	CLKB#	I, PD/PU	HSTL	Alternate differential clock input
9	VEE <sup>[2]</sup>	-PWR	Power	Power supply, negative connection
18,16,14,12	Q[0:3]#	O	ECL/PECL	Complement output
19,17,15,13	Q[0:3]	O	ECL/PECL	True output

**Table 1.**

Control	Operation
CLK_SEL	
0	CLKA, CLKA# input pair is active (Default condition with no connection to pin) CLKA can be driven with ECL- or PECL-compatible signals with respective power configurations
1	CLKB, CLKB# input pair is active. CLKB can be driven with HSTL-compatible signals with respective power configurations

**Governing Agencies**

The following agencies provide specifications that apply to the CY2DP314. The agency name and relevant specification is listed below in *Table 2*.

**Table 2.**

Agency Name	Specification
JEDEC	JESD 020B (MSL) JESD 8-6 (HSTL) JESD 51 (Theta JA) JESD 8-2 (ECL) JESD 65-B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

**Notes:**

- In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power
- In ECL mode (negative power supply mode),  $V_{EE}$  is either  $-3.3V$  or  $-2.5V$  and  $V_{CC}$  is connected to GND (0V). In PECL mode (positive power supply mode),  $V_{EE}$  is connected to GND (0V) and  $V_{CC}$  is either  $+3.3V$  or  $+2.5V$ . In both modes, the input and output levels are referenced to the most positive supply ( $V_{CC}$ ) and are between  $V_{CC}$  and  $V_{EE}$ .

**Absolute Maximum Ratings**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>CC</sub>	Positive Supply Voltage	Non-Functional	-0.3	4.6	V
V <sub>EE</sub>	Negative Supply Voltage	Non-Functional	-4.6	0.3	V
T <sub>S</sub>	Temperature, Storage	Non-Functional	-65	+150	°C
T <sub>J</sub>	Temperature, Junction	Non-Functional		150	°C
ESD <sub>h</sub>	ESD Protection	Human Body Model		2000	V
M <sub>SL</sub>	Moisture Sensitivity Level			3	N.A.
Gate Count	Total Number of Used Gates	Assembled Die		50	gates

**Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**Operating Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
I <sub>BB</sub>	Output Reference Current	Relative to V <sub>BB</sub>		200	µA
LU <sub>I</sub>	Latch Up Immunity	Functional, typical		100	mA
T <sub>A</sub>	Temperature, Operating Ambient	Functional	-40	+85	°C
∅ <sub>Jc</sub>	Dissipation, Junction to Case	Functional		37 <sup>[3]</sup>	°C/W
∅ <sub>Ja</sub>	Dissipation, Junction to Ambient	Functional		132 <sup>[3]</sup>	°C/W
I <sub>EE</sub>	Maximum Quiescent Supply Current	V <sub>EE</sub> pin		130 <sup>[4]</sup>	mA
C <sub>IN</sub>	Input pin capacitance			3	pF
L <sub>IN</sub>	Pin Inductance			1	nH
V <sub>IN</sub>	Input Voltage	Relative to V <sub>CC</sub> <sup>[5]</sup>	-0.3	V <sub>CC</sub> + 0.3	V
V <sub>TT</sub>	Output Termination Voltage	Relative to V <sub>CC</sub> <sup>[5]</sup>		V <sub>CC</sub> - 2	V
V <sub>OUT</sub>	Output Voltage	Relative to V <sub>CC</sub> <sup>[5]</sup>	-0.3	V <sub>CC</sub> + 0.3	V
I <sub>IN</sub>	Input Current <sup>[6]</sup>	V <sub>IN</sub> = V <sub>IL</sub> , or V <sub>IN</sub> = V <sub>IH</sub>		150	µA

**PECL/HSTL DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>CC</sub>	Operating Voltage	2.5V ± 5%, V <sub>EE</sub> = 0.0V 3.3V ± 5%, V <sub>EE</sub> = 0.0V	2.375 3.135	2.625 3.465	V V
V <sub>CMR</sub>	PECL Input Differential Crosspoint Voltage <sup>[7]</sup>	Differential operation	1.2	V <sub>CC</sub>	V
V <sub>X</sub>	HSTL Input Differential Crosspoint Voltage <sup>[8]</sup>	Standard Load Differential Operation	0.68	0.9	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -30 mA <sup>[9]</sup>	V <sub>CC</sub> - 1.25	V <sub>CC</sub> - 0.7	V
V <sub>OL</sub>	Output Low Voltage V <sub>CC</sub> = 3.3V ± 5% V <sub>CC</sub> = 2.5V ± 5%	I <sub>OL</sub> = -5 mA <sup>[9]</sup>	V <sub>CC</sub> - 1.995 V <sub>CC</sub> - 1.995	V <sub>CC</sub> - 1.5 V <sub>CC</sub> - 1.3	V V
V <sub>IH</sub>	Input Voltage, High	Single-ended operation	V <sub>CC</sub> - 1.165	V <sub>CC</sub> - 0.880 <sup>[10]</sup>	V
V <sub>IL</sub>	Input Voltage, Low	Single-ended operation	V <sub>CC</sub> - 1.945 <sup>[10]</sup>	V <sub>CC</sub> - 1.625	V

**Notes:**

- Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1.
- Power Calculation: V<sub>CC</sub> \* I<sub>EE</sub> + 0.5 (I<sub>OH</sub> + I<sub>OL</sub>) (V<sub>OH</sub> - V<sub>OL</sub>) (number of differential outputs used); I<sub>EE</sub> does not include current going off chip.
- where V<sub>CC</sub> is 3.3V ± 5% or 2.5V ± 5%.
- Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
- Refer to *Figure 1*.
- V<sub>X</sub>(AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V<sub>X</sub>(AC) range and the input swing lies within the V<sub>DIF</sub>(AC) specification. Violation of V<sub>X</sub>(AC) or V<sub>DIF</sub>(AC) impacts the device propagation delay, device and part-to-part skew. Refer to *Figure 2*.
- Equivalent to a termination of 50Ω to V<sub>TT</sub>. I<sub>OHMIN</sub> = (V<sub>OHMIN</sub> - V<sub>TT</sub>)/50; I<sub>OHMAX</sub> = (V<sub>OHMAX</sub> - V<sub>TT</sub>)/50; I<sub>OLMIN</sub> = (V<sub>OLMIN</sub> - V<sub>TT</sub>)/50; I<sub>OLMAX</sub> = (V<sub>OLMAX</sub> - V<sub>TT</sub>)/50.
- V<sub>IL</sub> will operate down to V<sub>EE</sub>; V<sub>IH</sub> will operate up to V<sub>CC</sub>.

**ECL DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>EE</sub>	Negative Power Supply	-2.5V ± 5%, V <sub>CC</sub> = 0.0V -3.3V ± 5%, V <sub>CC</sub> = 0.0V	-2.625 -3.465	-2.375 -3.135	V
V <sub>CMR</sub>	ECL Input Differential cross point voltage <sup>[7]</sup>	Differential operation	V <sub>EE</sub> + 1.2	0V	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -30 mA <sup>[9]</sup>	-1.25	-0.7	V
V <sub>OL</sub>	Output Low Voltage V <sub>EE</sub> = -3.3V ± 5% V <sub>EE</sub> = -2.5V ± 5%	I <sub>OL</sub> = -5 mA <sup>[9]</sup>	-1.995 -1.995	-1.5 -1.3	V
V <sub>IH</sub>	Input Voltage, High	Single-ended operation	-1.165	-0.880 <sup>[10]</sup>	V
V <sub>IL</sub>	Input Voltage, Low	Single-ended operation	-1.945 <sup>[10]</sup>	-1.625	V

**AC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>PP</sub>	ECL/PECL Input Differential Input Voltage <sup>[7]</sup>	Differential operation	0.1	1.3	V
V <sub>CMRO</sub>	Output Common Voltage Range (typ.)		V <sub>CC</sub> - 1.425		V
F <sub>CLK</sub>	Input Frequency	50% duty cycle Standard load	-	1.5	GHz
T <sub>PD</sub>	Propagation Delay CLKA or CLKB to Output pair <sup>[12]</sup>	PECL, ECL = 660 MHz HSTL < 1GHz	280 280	650 750	ps ps
V <sub>DIF</sub>	HSTL Differential Input Voltage <sup>[11]</sup>	Duty Cycle Standard Load Differential Operation	0.4	1.9	V
V <sub>X</sub>	HSTL Input Differential Crosspoint Voltage <sup>[8]</sup>	Standard Load Differential Operation	0.68	0.9	V
V <sub>o</sub>	Output Voltage (peak-to-peak; see Figure 2)	< 1 GHz	0.375	-	V
tsk <sub>(0)</sub>	Output-to-output Skew	660 MHz <sup>[12]</sup> , See Figure 3	-	50	ps
tsk <sub>(PP)</sub>	Part-to-Part Output Skew	660 MHz <sup>[12]</sup>	-	150	ps
T <sub>PER</sub>	Output Period Jitter (rms) <sup>[13]</sup>	660 MHz <sup>[12]</sup>	-	0.8	ps
tsk <sub>(P)</sub>	Output Pulse Skew <sup>[14]</sup>	660 MHz <sup>[12]</sup> , See Figure 3	-	50	ps
T <sub>R</sub> , T <sub>F</sub>	Output Rise/Fall Time (see Figure 2)	660 MHz 50% duty cycle Differential 20% to 80%	0.08	0.3	ns

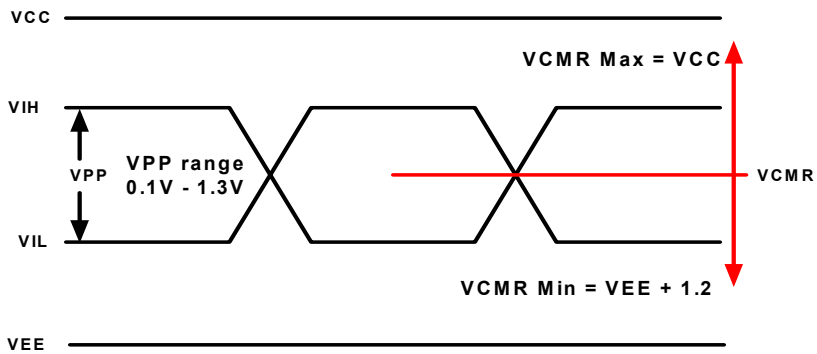
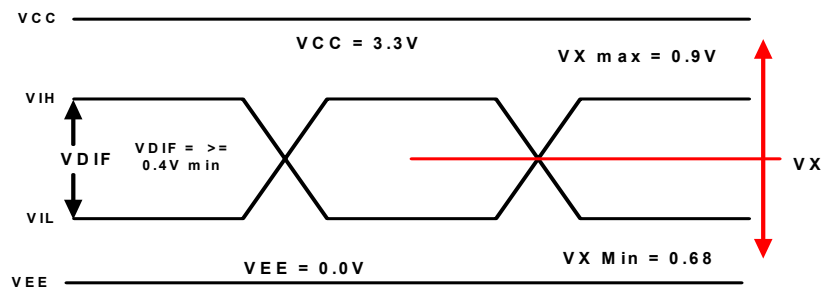
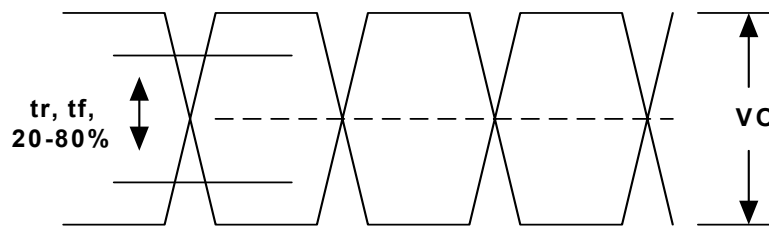
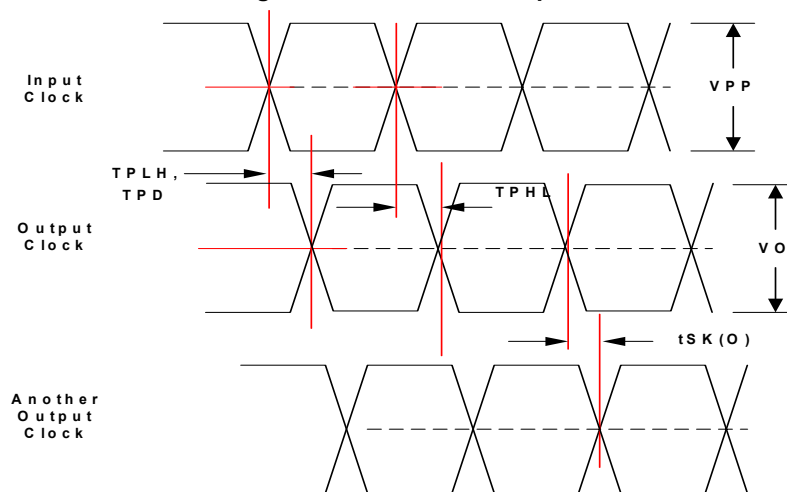
**Notes:**

11. V<sub>DIF</sub> (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tkpd and device-to-device skew.

12. 50% duty cycle; standard load; differential operation.

13. For 3.3V supplies. Jitter measured differentially using an Agilent 8133A Pulse Generator with an 8500A LeCroy Wavemaster Oscilloscope using at least 10,000 data points.

14. Output pulse skew is the absolute difference of the propagation delay times: | t<sub>PLH</sub> - t<sub>PHL</sub> |.

**Timing Definitions**

**Figure 1. PECL/ECL Input Waveform Definitions**

**Figure 2. HSTL Differential Input Waveform Definitions**

**Figure 3. ECL/LVPECL Output**

**Figure 4. Propagation Delay ( $T_{PD}$ ), output pulse skew ( $|t_{PLH} - t_{PHL}|$ ), and output-to-output skew ( $t_{SK(O)}$ ) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL**

### Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

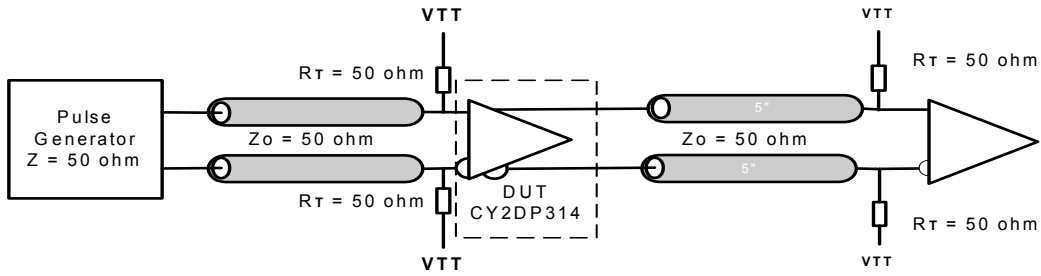


Figure 5. CY2DP314 AC Test Reference

### Applications Information

#### Termination Examples

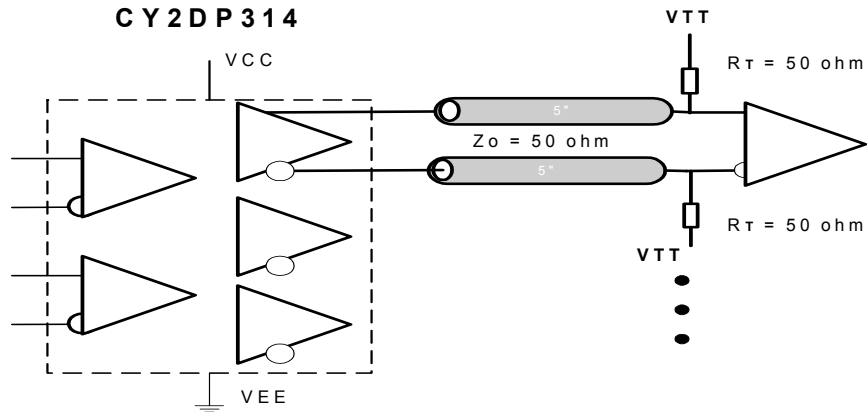


Figure 6. Standard LVPECL - PECL Output Termination

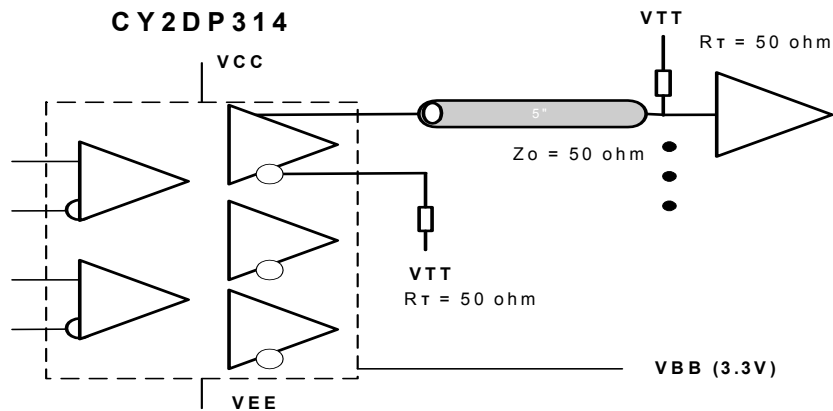
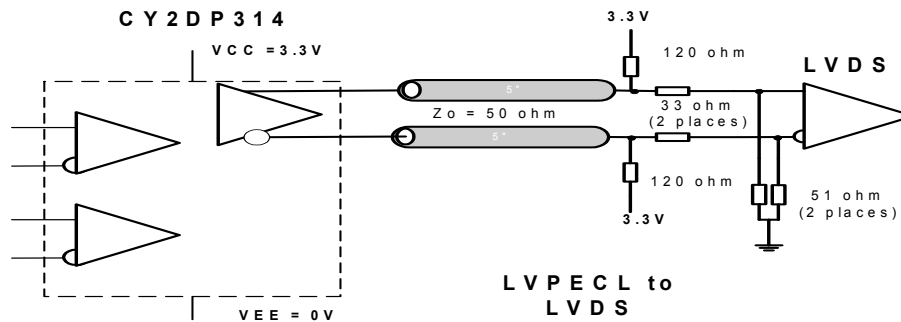
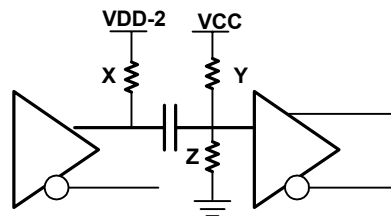


Figure 7. Driving a PECL/ECL Single-ended Input



**Figure 8. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface**

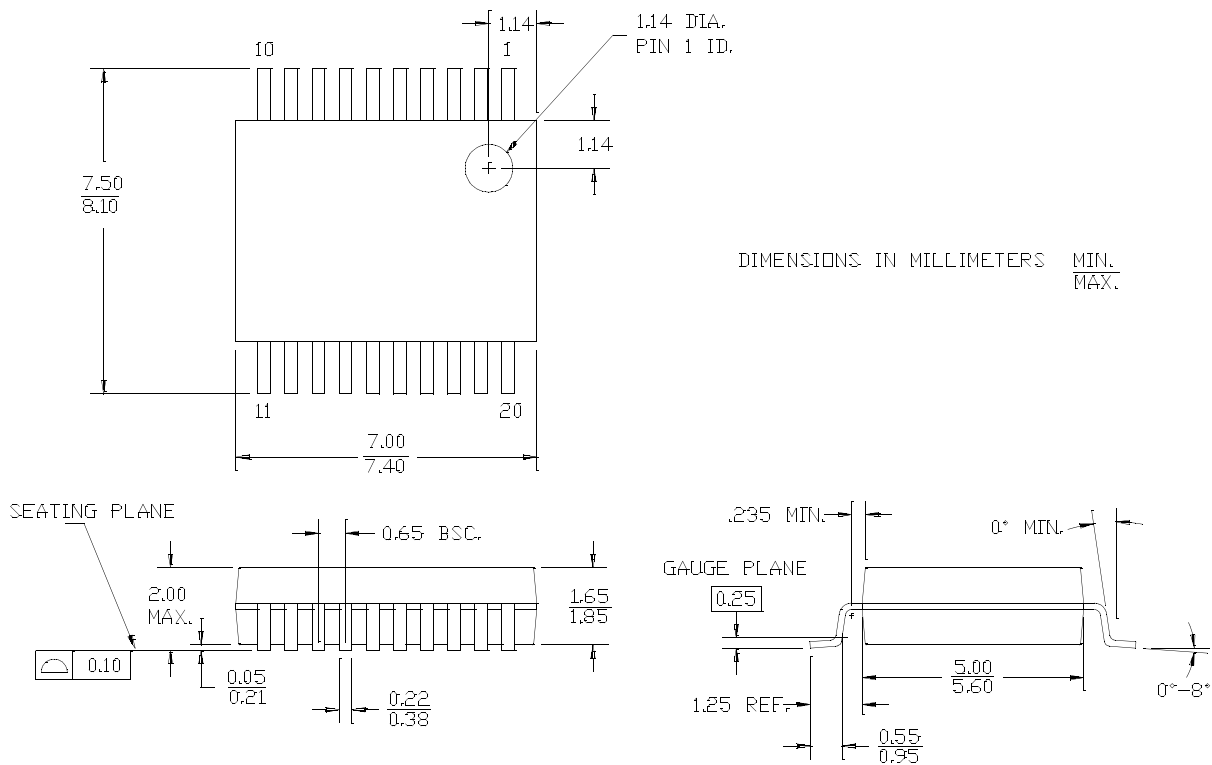


One output is shown for clarity

**Figure 9. Termination for LVPECL to H I S L interface for  $V_{CC}=2.5V$  would use  $X=50$  Ohms,  $Y=2300$  Ohms, and  $Z=1000$  Ohms. See application note entitled *PECL Translation, SAW Oscillators, and Specs for Other Signalling Standards and Supplies***

### Ordering Information

Part Number	Package Type	Product Flow
CY2DP314OI	20-pin SSOP	Industrial, $-40^{\circ}$ to $85^{\circ}C$
CY2DP314OIT	20-pin SSOP – Tape and Reel	Industrial, $-40^{\circ}$ to $85^{\circ}C$
<b>Lead-free</b>		
CY2DP314OXI	20-pin SSOP	Industrial, $-40^{\circ}$ to $85^{\circ}C$
CY2DP314OXIT	20-pin SSOP – Tape and Reel	Industrial, $-40^{\circ}$ to $85^{\circ}C$

**Package Drawing and Dimensions**
**20-Lead (5.3 mm) Shrunk Small Outline Package O20**


51-85077-C

FastEdge is a trademark of Cypress Semiconductor Corporation. All product and company names mentioned in this document are the trademarks of their respective holders.



**Document History Page**

Document Title: CY2DP314 FastEdge™ SERIES 1 of 2:4 Differential Clock/Data Fanout Buffer				
Document Number: 38-07550				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	126779	06/13/03	RGL	New data sheet
*A	128940	08/19/03	RGL	Changed the operation value from 1.5 GHz, reduced swing to 3 GHz to from DC to above 1.5 GHz Changed $V_{CC}$ value in the $I_{IN}$ parameter from 3.6V to 3.645V. Changed the $V_{OL}$ min value from $V_{CC}-1.9$ to $V_{CC}-1.945$ Changed the $I_{EE}$ max value from 48 mA to 130 mA Specified the max input frequency ( $F_{CLK}$ ) to 2200 MHz Specified the TTB max value to 250 ps
*B	207710	See ECN	RGL	Added Junction Temperature ( $T_J$ ) parameter in the Absolute Max. Conditions table Replaced $I_{CC}$ calculation with power calculation in the footnote
*C	237748	See ECN	RGL	Provided data for TBDs to match the device
*D	247603	See ECN	RGL/GGK	Changed $V_{OH}$ and $V_{OL}$ to match the Char Data
*E	270151	See ECN	RGL	Removed all $V_{BB}$ references Added Lead-free devices