# 10-Bit Current-Output D/A Converter

# DAC-100

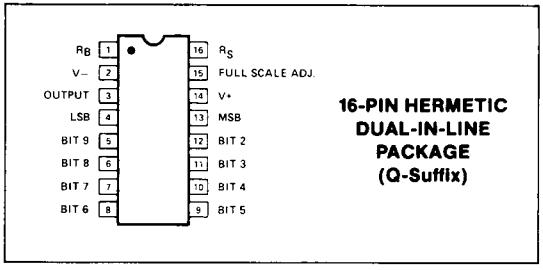
## FEATURES

- **Fast Settling ..... 225nsec (8 Bits), 375nsec (10 Bits)**
- **Stable ..... Tempcos to ±15ppm/°C Max**
- **Commercial, Industrial and Military Models Available**
- **TTL Compatible Logic Inputs**
- **Wide Supply Range ..... ±6V to ±18V**
- **Available in Die Form**

The small size, wide operating temperature range, and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed analog-to-digital converters.

2

## PIN CONNECTIONS




**16-PIN HERMETIC DUAL-IN-LINE PACKAGE (Q-Suffix)**

## GENERAL DESCRIPTION

The DAC-100 is a complete 10-bit resolution digital-to-analog converter constructed on two monolithic chips in a single 16-pin DIP. Featuring excellent linearity vs. temperature performance, the DAC-100 includes a low tempco voltage reference, ten current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output, matched bipolar offset and feedback resistors. Resistors are included for use with an external op amp for voltage output applications.

Although all units have 10-bit resolution, a wide choice of linearity and temperature coefficient options are provided to allow price/performance optimization.

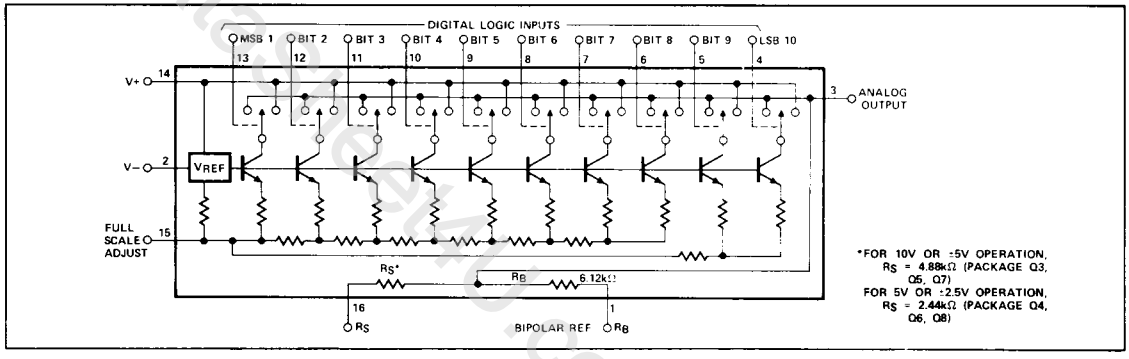
## ORDERING INFORMATION †

| N.L.* %FS MAX | TEMPCO* ppm/°C MAX | MILITARY TEMPERATURE $V_O = \pm5V/10V$ | MILITARY TEMPERATURE $V_O = \pm2.5V/5V$ | INDUSTRIAL TEMPERATURE $V_O = \pm5V/10V$ | INDUSTRIAL TEMPERATURE $V_O = \pm2.5V/5V$ | COMMERCIAL TEMPERATURE $V_O = \pm5V/10V$ | COMMERCIAL TEMPERATURE $V_O = \pm2.5V/5V$ |
|---|---|---|---|---|---|---|---|
| ±0.05 | ±60 | DAC100ACQ5/883 | DAC100ACQ6/883 | DAC100ACQ7 | DAC100ACQ8 | DAC100ACQ3 | DAC100ACQ4 |
| ±0.10 | ±30 | – | – | DAC100BBQ7 | DAC100BBQ8 | – | – |
| ±0.10 | ±60 | DAC100BCQ5/883 | – | – | – | DAC100BCQ3 | DAC100BCQ4 |
| ±0.20 | ±60 | DAC100CCQ5/883 | DAC100CCQ6/883 | DAC100CCQ7 | – | DAC100CCQ3 | DAC100CCQ4 |
| ±0.30 | ±120 | – | – | – | – | DAC100DDQ3 | – |

* Part number construction: The 1st letter following DAC-100 (A-D) refers to the nonlinearity specification; the 2nd letter (A-D) refers to the full-scale tempco; the letter Q refers to the package; and the end numeral indicates the output voltage and temperature.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

## SIMPLIFIED SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ Supply to V– Supply ..... 0 to +36V
V+ Supply to Output ..... 0 to +18V
V– Supply to Output ..... 0 to –18V
Logic Inputs to Output ..... –1V to +6V
Operating Temperature Range Q3, Q4 ..... 0°C to +70°C
Q5, Q6, Q7, Q8 ..... –55°C to +125°C
Junction Temperature ..... –25°C to +150°C

Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

| PACKAGE TYPE | $\Theta_{JA}$ (Note 2) | $\Theta_{JC}$ | UNITS |
|---|---|---|---|
| 16-Pin Hermetic DIP (Q) | 94 | 12 | °C/W |

**NOTES:**
1. Ratings apply to DICE and packaged parts, unless otherise noted.
2. $\Theta_{JA}$ is specified for worst case mounting conditions, i.e., $\Theta_{JA}$ is specified for device in socket for CerDIP package.

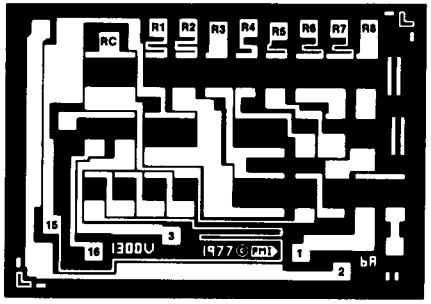
## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$ for Q7 and Q8 devices; $0°C \leq T_A \leq +70°C$ for Q3 and Q4; $-55°C \leq T_A \leq +125°C$ for Q5 and Q6 devices, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | DAC-100 | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Resolution | | | | 10 | — | — | Bits |
| Nonlinearity (For nonlinearity/tempco combinations, see Ordering Information) | NL | (±1/2LSB — 10 bits) | A— | — | — | ±0.05 | %FS |
| | | (±1/2LSB — 9 bits) | B— | — | — | ±0.1 | |
| | | (±1/2LSB — 8 bits) | C— | — | — | ±0.2 | |
| | | (±3/4LSB — 8 bits) | D— | — | — | ±0.3 | |
| Full-Scale Tempco (See Full-Scale Test Circuit) | $T_C$ | | —B | — | — | ±30 | ppm/°C |
| | | | —C | — | — | ±60 | |
| | | | —D | — | — | ±120 | |
| Settling Time $T_A = 25°C$ | $t_S$ | to ±0.05% FS | ALL | — | — | 375 | ns |
| | | to ±0.1% FS | ALL | — | — | 300 | |
| | | to ±0.2% FS | ALL | — | — | 225 | |
| | | to ±0.4% FS | ALL | — | — | 150 | |
| | | to ±0.8% FS | ALL | — | — | 100 | |
| Full-Range Output Voltage (Limits guarantee adjustability to exact 10.0 (5.0)V with a 200Ω Trimpot® between Adjust and V–) | $V_{FR}$ | Connect FS Adjust to V– | | | | | V |
| | | 10V Models (Q3, Q5, Q7) (See Full-Scale Test Circuit) | | 10 | — | 11.1 | |
| | | 5V Models (Q4, Q6, Q8) $V_{IN} = 0.7V$ (See Basic Unipolar Voltage Output Circuit) | | 5 | — | 5.55 | |
| Zero-Scale Output Voltage | $V_{ZS}$ | $V_{IN} = 2.1V$ | ALL | — | — | 0.013 | %FS |
| Logic Inputs: High | $V_{INH}$ | Measured with respect to output pin | ALL | 2.1 | — | — | V |
| Logic Inputs: Low | $V_{INL}$ | Measured with respect to output pin | ALL | — | — | 0.7 | V |
| Logic Input Current, Each Input | $I_{IN}$ | $V_{IN} = 0$ to +6V | ALL | — | — | 5 | µA |
| Logic Input Resistance | $R_{IN}$ | $V_{IN} = 0$ to +6V | ALL | — | 3 | — | mΩ |
| Logic Input Capacitance | $C_{IN}$ | | ALL | — | 2 | — | pF |
| Output Resistance | $R_O$ | | ALL | — | 500 | — | kΩ |
| Output Capacitance | $C_O$ | | ALL | — | 13 | — | pF |
| Applied Power Supplies: V+ | | | ALL | +6 | — | +18 | V |
| Applied Power Supplies: V– | | | ALL | –6 | — | –18 | V |
| Power Supply Sensitivity | $P_{SS}$ | $V_S = \pm 6V$ to ±18V | ALL | — | — | ±0.10 | % per Volt |
| Power Consumption | $P_D$ | $V_S = \pm 15V$ | Q3, Q4 | — | 200 | 300 | mW |
| | | $V_S = \pm 6V$ | Q3, Q4 | — | 80 | — | |
| | | $V_S = \pm 15V$ | Q5, Q6, Q7, Q8 | — | 200 | 250 | |
| Positive Supply Current | I+ | $V_S = +15V$ | Q3, Q4 | — | — | 10 | mA |
| | | $V_S = +15V$ | Q5, Q6, Q7, Q8 | — | — | 8.33 | |
| Negative Supply Current | I– | $V_S = -15V$ | Q3, Q4 | — | — | –10 | mA |
| | | $V_S = -15V$ | Q5, Q6, Q7, Q8 | — | — | –8.33 | |

**NOTE:**
For applications where long-term stability is critical, an external voltage reference is recommended (see PMI REF-01/02).

## DICE CHARACTERISTICS

**DAR-01**



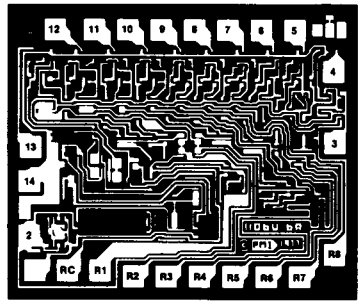

DIE SIZE .090 × .064 inch, 5760 sq. mils
(2.286 × 1.701 mm, 3.888 sq. mm)

1. $R_B$
2. V–
3. OUTPUT
15. FULL-SCALE ADJ
16. $R_S$

R — Pads are connected to similarly marked pads on DAI-01

Note: Pads 4 — 14, See DAI-01

**DAI-01**




DIE SIZE 0.080 x 0.067 inch, 5,360 sq. mils
(2.032 x 1.702 mm, 3.458 sq. mm)

2. V–
3. OUTPUT
4. BIT 10 (LSB)
5. BIT 9
6. BIT 8
7. BIT 7
8. BIT 6
9. BIT 5
10. BIT 4
11. BIT 3
12. BIT 2
13. BIT 1 (MSB)
14. V+

R — Pads are connected to similarly marked pads on DAR-01

Note: Pads 1, 2, 15, 16, See DAR-01

These die versions are available on special order; contact your PMI sales office.

**WAFER TEST LIMITS** at $T_A$ = 25°C for the R-2R Ladder Network comprised of R1—R8, R12, R23, R34, R45 and R56 when connected to an ideal DAI-01, unless otherwise noted.

| | | DAR-01-N | | | DAR-01-G | | | |
|---|---|---|---|---|---|---|---|---|
| PARAMETER | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| Nonlinearity | VR1 = 3.2V | — | — | ±0.035 | — | — | ±0.05 | % |

**WAFER TEST LIMITS** at $T_A$ = 25°C, VR1 = 3.2V, unless otherwise noted.

| | | DAR-01 | | | |
|---|---|---|---|---|---|
| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| Resistance R1 | Absolute Measurement | 2.56 | — | 3.84 | kΩ |
| Ratio RC1 to R1 | Ideal = 1.00503 to 1 | −1 | — | +1 | % |
| Ratio R1 to RS1 | Ideal = 1.29959 to 1 | −1 | — | +1 | % |
| Ratio R1 to RS2 | Ideal = 1.29959 to 1 | −1 | — | +1 | % |
| Ratio RB to R1 | Ideal = 1.92211 to 1 | −1 | — | +1 | % |

**NOTE:**
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** in common to all grades.

| PARAMETER | CONDITIONS | DAR-01 MIN | DAR-01 TYP | DAR-01 MAX | UNITS |
|---|---|---|---|---|---|
| Absolute Temperature Coefficient | All Resistors | — | ±180 | — | ppm/°C |
| Tracking Temperature Coefficient | All Resistors with Respect to R1 | — | 3 | — | ppm/°C |

**WAFER TEST LIMITS** at $T_A$ = 25°C when connected to an ideal DAR-01, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | DAI-01-N MIN | DAI-01-N TYP | DAI-01-N MAX | DAI-01-G MIN | DAI-01-G TYP | DAI-01-G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Nonlinearity | NL | $V_S$ = ±15V | — | — | ±0.05 | — | — | ±0.1 | % |
| Internal Reference Voltage | $V_{MCR}$ | $V_S$ = ±15V | 6.6 | — | 6.900 | 6.6 | — | 6.900 | V |

**WAFER TEST LIMITS** at $V_S$ = ±15V, $T_A$ = 25°C when connected to an ideal DAR-01, unless otherwise noted.

| PARAMETER | CONDITIONS | DAI-01 MIN | DAI-01 TYP | DAI-01 MAX | UNITS |
|---|---|---|---|---|---|
| Resolution | | 10 | — | 10 | Bits |
| Analog Output Current | All Bits Low, V– Connected to FS Adjust | 1840 | — | 2274 | μA |
| Zero-Scale Output Current | All Bits High, V– Connected to FS Adjust | — | — | ±0.011 | $\%I_{FS}$ |
| Logic Input "0" | Measured with Respect to Output | — | — | 0.7 | V |
| Logic Input "1" | Measured with Respect to Output | 2.1 | — | — | V |
| Supply Current | All Bits High, V– Connected to FS Adjust | — | — | 8.33 | mA |
| Power Supply Rejection | $V_S$ = ±6V to ±18V | — | — | 0.1 | $\%I_{FS}/V$ |

**NOTE:**
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

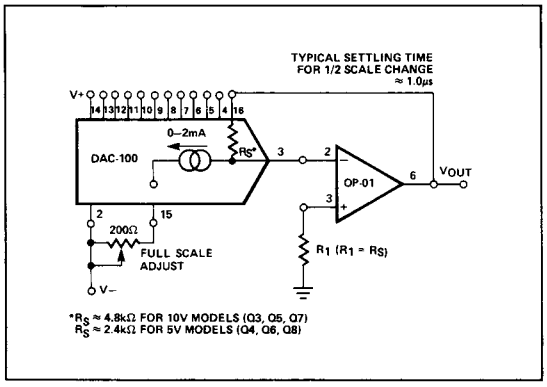
**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S$ = ±15V, and when connected to an ideal DAR-01, unless otherwise noted.

| PARAMETER | CONDITIONS | DAI-01-N MIN | DAI-01-N TYP | DAI-01-N MAX | DAI-01-G MIN | DAI-01-G TYP | DAI-01-G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Full-Scale Temperature Coefficient (Note) | | — | ±60 | — | — | ±60 | — | ppm/°C |

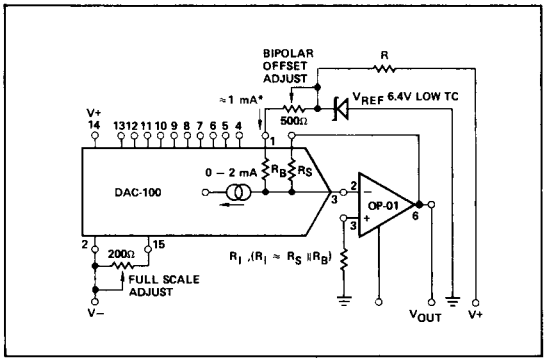
**NOTE:**
Full-Scale Temperature Coefficient is defined as the change in output voltage measured in the basic unipolar voltage output test circuit shown on the DAC-100 data sheet and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

## BASIC CONNECTIONS

### BASIC UNIPOLAR VOLTAGE OUTPUT CIRCUIT




### BASIC BIPOLAR VOLTAGE OUTPUT CIRCUIT

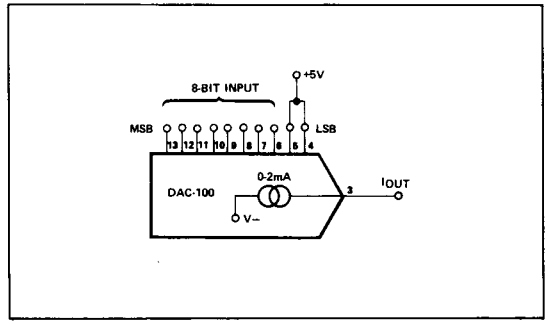



## APPLICATIONS INFORMATION

**FULL RANGE OUTPUT ADJUSTMENT** — The output current of the DAC-100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the full-scale adjust pin and V–. Adjustment should be made with an input of all "zeroes."

**LOWER RESOLUTION APPLICATIONS** — The DAC-100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs **must** be tied to logic high for proper operation. "Floating" logic inputs can cause improper operation.

### REDUCED RESOLUTION APPLICATION




**LOGIC CODING** — The DAC-100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full range output, while an all "ones" input produces a zero-scale output. Each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input turns the bit "OFF," low logic input level turns the bit "ON".

**LOGIC COMPATIBILITY** — The input logic levels are directly compatible with TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

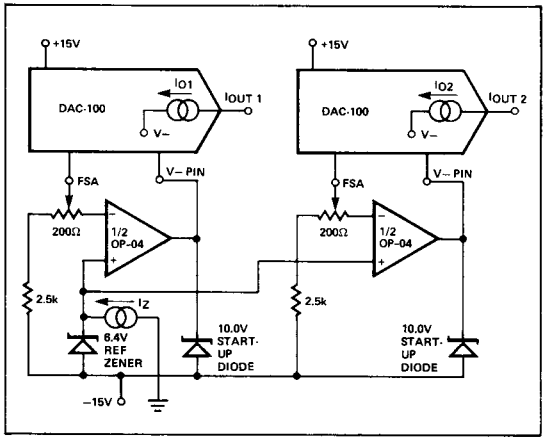
**NONLINEARITY (NL)** — The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of full-scale range (FSR) or given in terms of LSB value. The end points are zero-scale output to full-scale output for unipolar operation and minus full-scale to positive full-scale for bipolar operation.

**BIPOLAR OPERATION** — The DAC-100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volts.

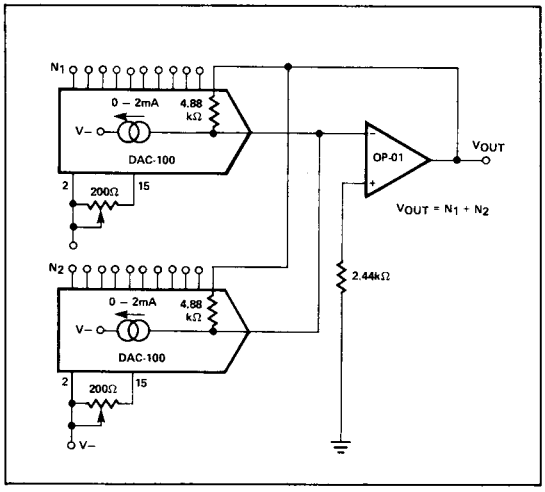
**VOLTAGE AT OUTPUT PIN** — The DAC-100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output to ground is a convenient way of clamping the output to this limit.

## TYPICAL APPLICATIONS

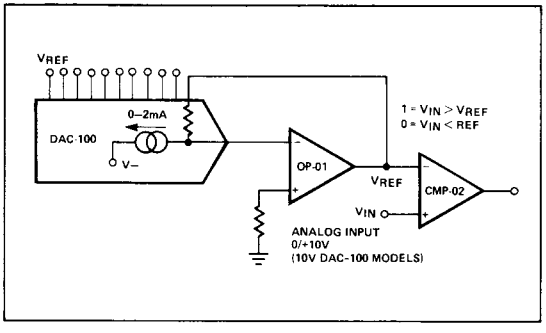
### EXTERNAL REFERENCE CONNECTION



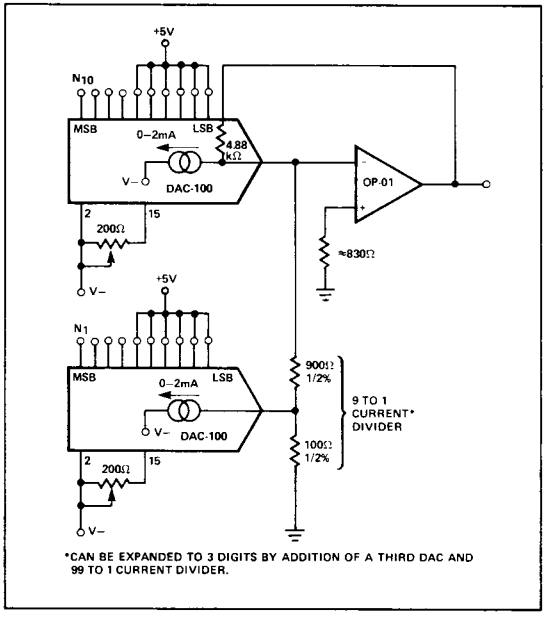

### ANALOG SUM OF TWO DIGITAL NUMBERS




### DIGITALLY PROGRAMMED LEVEL DETECTOR




### BINARY-CODED-DECIMAL D/A CONVERSION




*CAN BE EXPANDED TO 3 DIGITS BY ADDITION OF A THIRD DAC AND 99 TO 1 CURRENT DIVIDER.

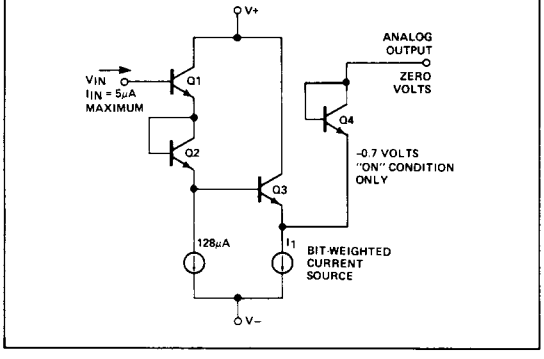
### INTERFACING WITH CMOS LOGIC

The DAC-100 requires only about 1$\mu$A of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed; logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

### LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

### DAC-100 — LOGIC INPUT STAGE



Switching is accomplished by forward biasing Q4, diode-connected transistor, for the bit "ON" condition and back biasing Q4 in the "OFF" condition. For the "ON" condition ($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, $I_1$, flows from the analog output through Q4 and ultimately to V−. In the "OFF" condition ($V_{IN} \geq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If $V_{IN}$ is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

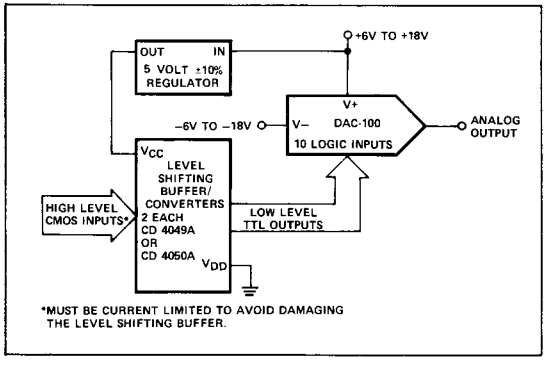
$$1)\ BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100 operation with CMOS inputs is easily achieved.

### ±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 with CMOS logic. At ±6 volts the DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

### BLOCK DIAGRAM — CMOS TO DAC-100 INTERFACE




### HIGH LEVEL CMOS INTERFACING

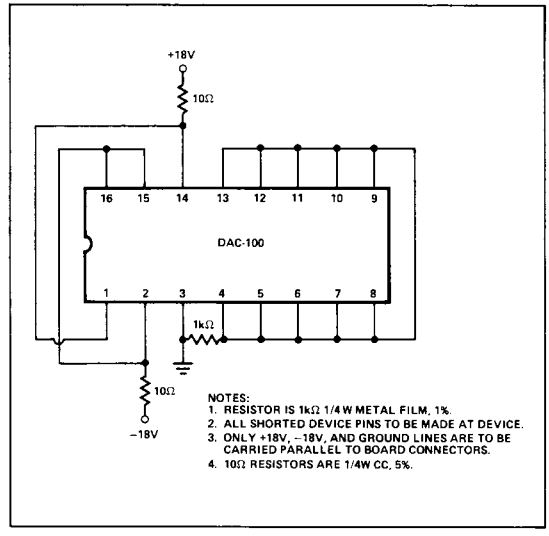
The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with the DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or non-inverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100 to CMOS interfacing method to be used in either type of application.

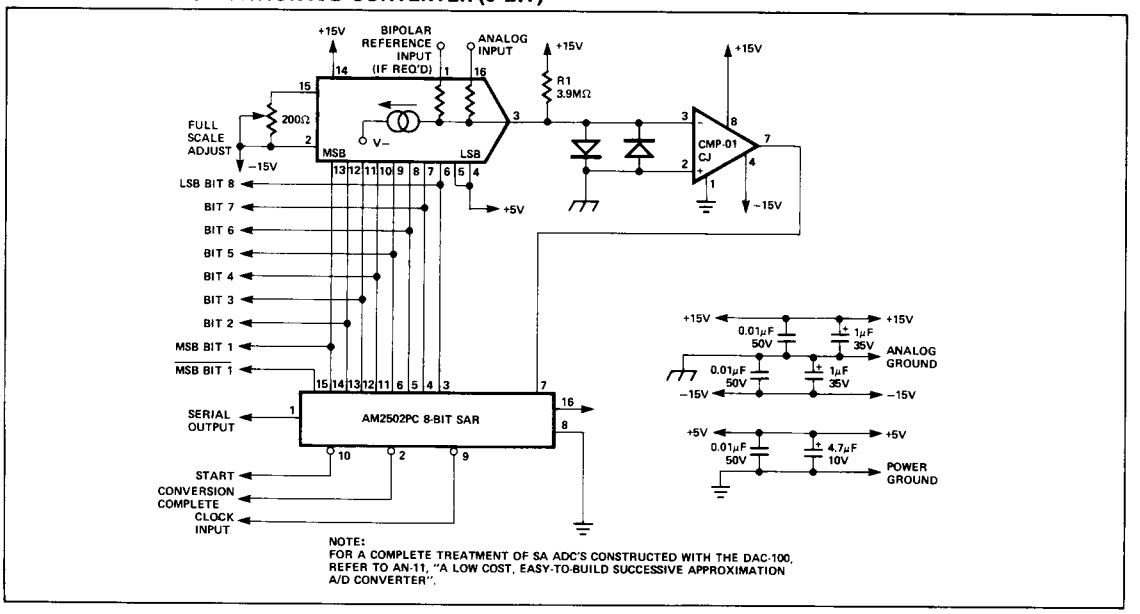
Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive three-terminal IC regulator can supply several level shifting devices.

**NOTE:**
For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/A's with CMOS Logic."

### BURN-IN CIRCUIT

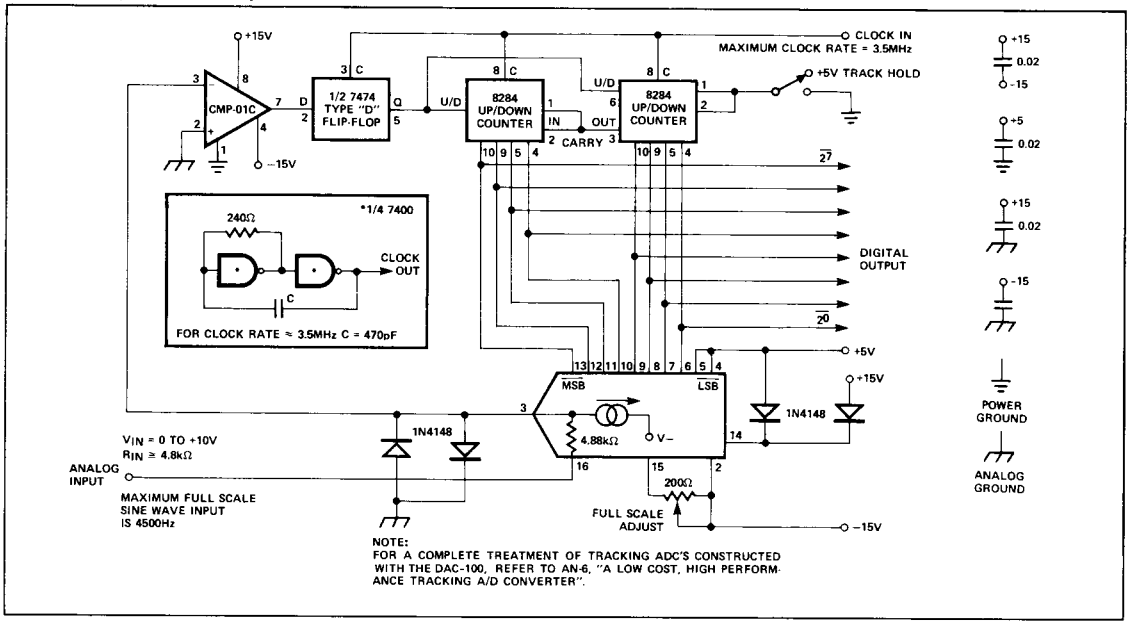


## SUCCESSIVE APPROXIMATION A/D CONVERTER (8-BIT)




NOTE:
FOR A COMPLETE TREATMENT OF SA ADC'S CONSTRUCTED WITH THE DAC-100, REFER TO AN-11, "A LOW COST, EASY-TO-BUILD SUCCESSIVE APPROXIMATION A/D CONVERTER".

## TRACKING (SERVO-TYPE) A/D CONVERTER




NOTE:
FOR A COMPLETE TREATMENT OF TRACKING ADC'S CONSTRUCTED WITH THE DAC-100, REFER TO AN-6, "A LOW COST, HIGH PERFORMANCE TRACKING A/D CONVERTER".