STANDARD MICROSYSTEMS CORPORATION

FDC 1791-02
FDC 1792-02
FDC 1793-02
FDC 1794-02
FDC 1795-02
FDC 1797-02

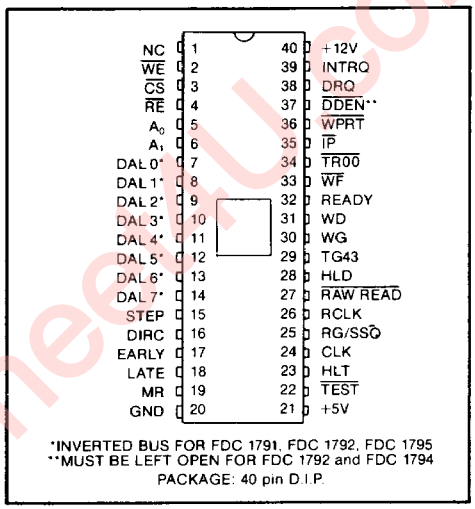
Floppy Disk Controller/Formatter FDC

μPC FAMILY

FEATURES

- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 1795, FDC 1797)
- ☐ WINDOW EXTENSION (IN MFM)

PIN CONFIGURATION



*INVERTED BUS FOR FDC 1791, FDC 1792, FDC 1795
**MUST BE LEFT OPEN FOR FDC 1792 and FDC 1794
PACKAGE: 40 pin D.I.P.

- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FD179X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

GENERAL DESCRIPTION

The FDC 179X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 179X chip design has evolved into six specific parts: FDC 1791, FDC 1792, FDC 1793, FDC 1794, FDC 1795, and the FDC 1797.

This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

The FDC 1791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 1791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

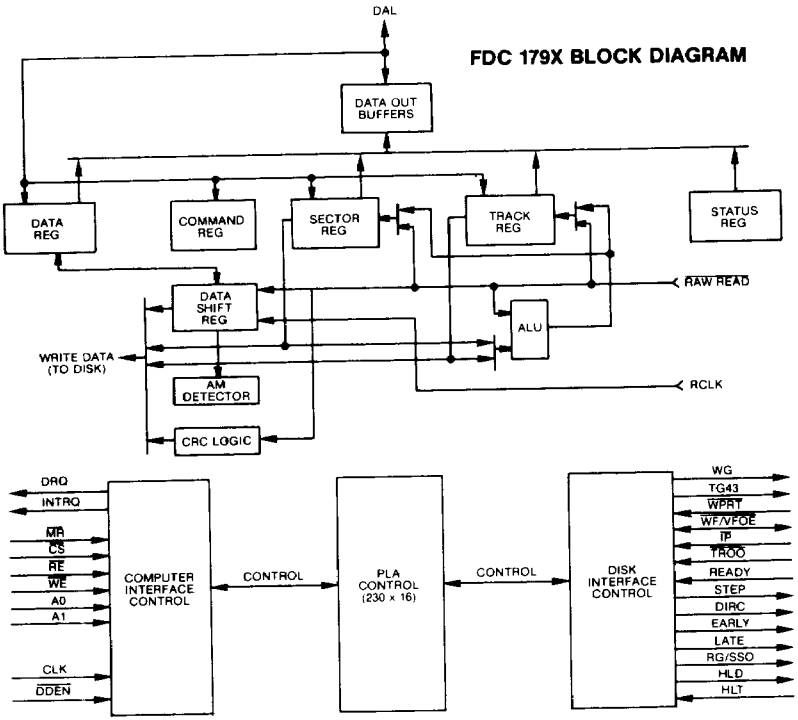
The FDC 1793 is identical to the FDC 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The FDC 1792 operates in the single density mode only. Pin 37 ($\overline{DDEN}$) of the FDC 1792 must be left open for proper operation. The FDC 1794 is identical to the FDC 1792 except the DAL lines are TRUE for systems that utilize true data busses. The FDC 1795 adds side select logic to the FDC 1791. The FDC 1797 adds the side select logic to the FDC 1793.

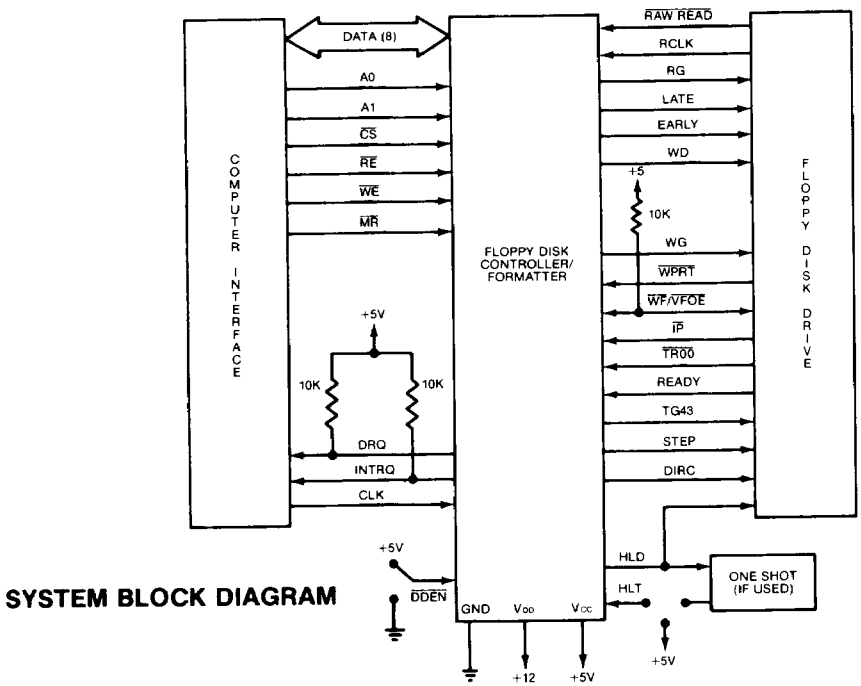
The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on a multiplexed bus with other bus-oriented devices.

SECTION VI

FDC 179X BLOCK DIAGRAM



SYSTEM BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	This pin is internally connected to the substrate bias generator and must be left open.
20	GROUND	V_{SS}	Ground
21	POWER SUPPLY	V_{CC}	+5V
40	POWER SUPPLY	V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into the sector register.
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and the parallel data bus (DAL).
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on DALØ-DAL7 when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 / A0 / $\overline{RE}$ / $\overline{WE}$ 0 / 0 / Status Reg / Command Reg 0 / 1 / Track Reg / Track Reg 1 / 0 / Sector Reg / Sector Reg 1 / 1 / Data Reg / Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$. The Data Bus is inverted on the FDC 1791, FDC 1792 and FDC 1795.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for 5¼" drives.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use a 10K pull-up resistor to +5V.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use a 10K pull-up resistor to +5V.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	Step and direction motor control. The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	TEST	$\overline{TEST}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.

PIN NO.	NAME	SYMBOL	FUNCTION
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S=1, SSO is set to a logic 1. When S=0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$/ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG=1, Pin 33 functions as a $\overline{\text{WF}}$ input. If $\overline{\text{WF}}$=0, any write command will immediately be terminated. When WG=0, Pin 33 functions as a $\overline{\text{VFOE}}$ output. $\overline{\text{VFOE}}$ will go low during a read operation after the head has loaded and settled (HLT=1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. $\overline{\text{VFOE}}$ will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, $\overline{\text{VFOE}}$ will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FDC179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FDC179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$=0, double density is selected. When $\overline{\text{DDEN}}$=1, single density is selected. This line must be left open on the 1792/4.

FUNCTIONAL DESCRIPTION

The FDC 179X-02 major functional blocks are as follows:

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector—The address mark detector detects ID, data and index address marks during ready and write operations.

SECTION VI

OPERATION

FDC 1791, FDC 1793, FDC 1795 and FDC 1797 have two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}} = 1$, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

DDEN must be left open for the FDC 1792 and FDC 1794.

Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track can be from 1 to 255 sectors. The number of tracks is from 0 to 255 tracks.

For read operations, the FDC 179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not, it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FDC179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FDC179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FDC179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF/VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is

transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution against erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FDC179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FDC179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FDC179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}=1$) and 250 ns pulses in MFM ($\overline{\text{DDEN}}=0$). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FDC179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

COMMAND WORDS

The FDC179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

Table 1. Command Summary

		BITS							
COMMAND	TYPE	7	6	5	4	3	2	1	0
Restore	I	0	0	0	0	h	V	r_1	r_0
Seek	I	0	0	0	1	h	V	r_1	r_0
Step	I	0	0	1	u	h	V	r_1	r_0
Step In	I	0	1	0	u	h	V	r_1	r_0
Step Out	I	0	1	1	u	h	V	r_1	r_0
Read Sector	II	1	0	0	m	F_2	E	F_1	0
Write Sector	II	1	0	1	m	F_2	E	F_1	a_0
Read Address	III	1	1	0	0	0	E	0	0
Read Track	III	1	1	1	0	0	E	0	0
Write Track	III	1	1	1	1	0	E	0	0
Force Interrupt	IV	1	1	0	1	I_3	I_2	I_1	I_0

Type I Commands

The Type I Commands are Restore, Seek, Step, Step-In, and Step-Out. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 2.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FDC179X receives a command that specifically disengages the head. If the FDC179X is idle (busy=0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field if read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt

is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FDC179X terminates the operation and sends an interrupt (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (u). When u=1, the track register is updated by one for each step. When u=0, the track register is not updated.

On the FDC 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

Restore (Seek Track 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. if $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FDC179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

Seek

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FDC179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step

Upon receipt of this command, the FDC179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-In

Upon receipt of this command, the FDC179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-Out

Upon receipt of this command, the FDC179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of command. An interrupt is generated at the completion of the command.

Head Positioning

The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$=0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 2) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V=1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FDC179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

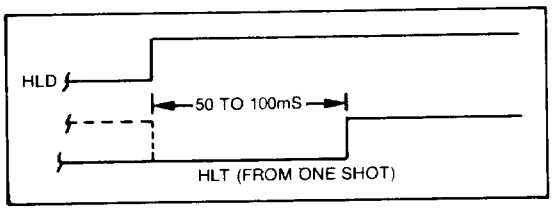
Table 2. Stepping Rates

CLK:		2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$:		0	1	0	1	X	X
r_1	r_0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0	0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0	1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1	0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1	1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h=1), at the end of the Type I command if the verify flag (V=1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h=0 and V=0); or if the FDC179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FDC179X which is used for the head engage time. When HLT=1, the FDC179X assumes the head is completely engaged.

The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FDC179X.



Head Load Timing

When both HLD and HLT are true, the FDC179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

TYPE I COMMANDS FLAG SUMMARY
h=Head Load Flag (Bit 3)
h=1, Load head at beginning h=0, Unload head at beginning
V=Verify flag (Bit 2)
V=1, Verify on destination track V=0, No verify
r_1r_0=Stepping motor rate (Bits 1-0)
Refer to Table 2 for rate summary
u=Update flag (Bit 4)
u=1, Update Track register u=0, No update

Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the system must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag=1 (this is the normal case) HLD is made active and HLT is sampled until true after a 15 msec delay. If the E flag is 0, HLD is made active and HLT is sampled with no delay until true. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FDC179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FDC179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m=0, a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FDC179X will read or write multiple records starting with the sector presently in the sector register. The FDC179X will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C=0, no side comparison is made. When C=1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The FDC1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

Sector Length Table (1791/2/3/4 only)	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Field Format

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record-Not-Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FDC179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FDC179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

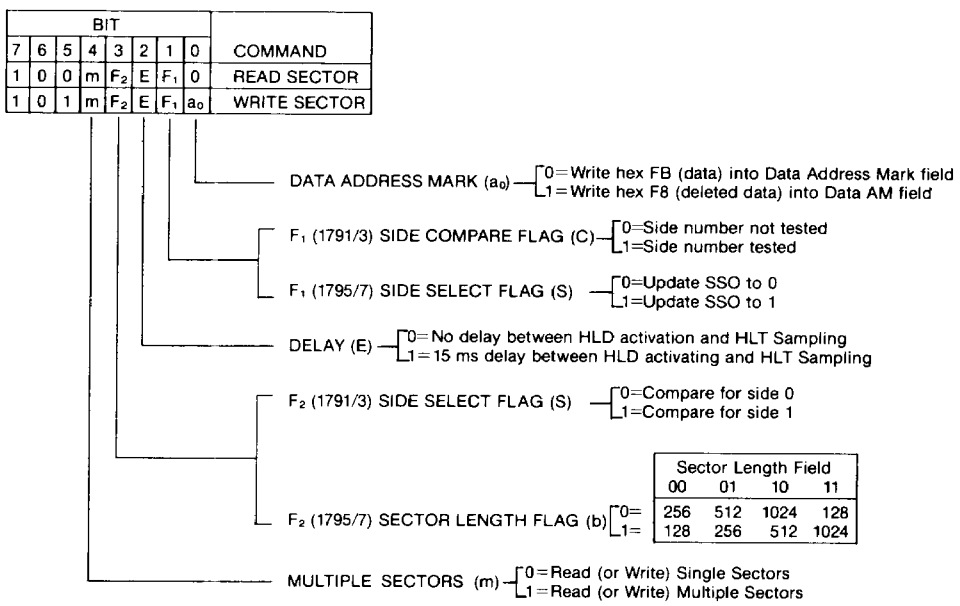


Figure 1. Type II and III Flag Summary

Type III Commands

There are three Type III Commands:

- READ ADDRESS—Read the next ID field (6 bytes) into the FDC.
- READ TRACK—Read all bytes of the entire track, including gaps.
- WRITE TRACK—Write all bytes to the entire track, including gaps.

Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FDC179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

Write Track

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which

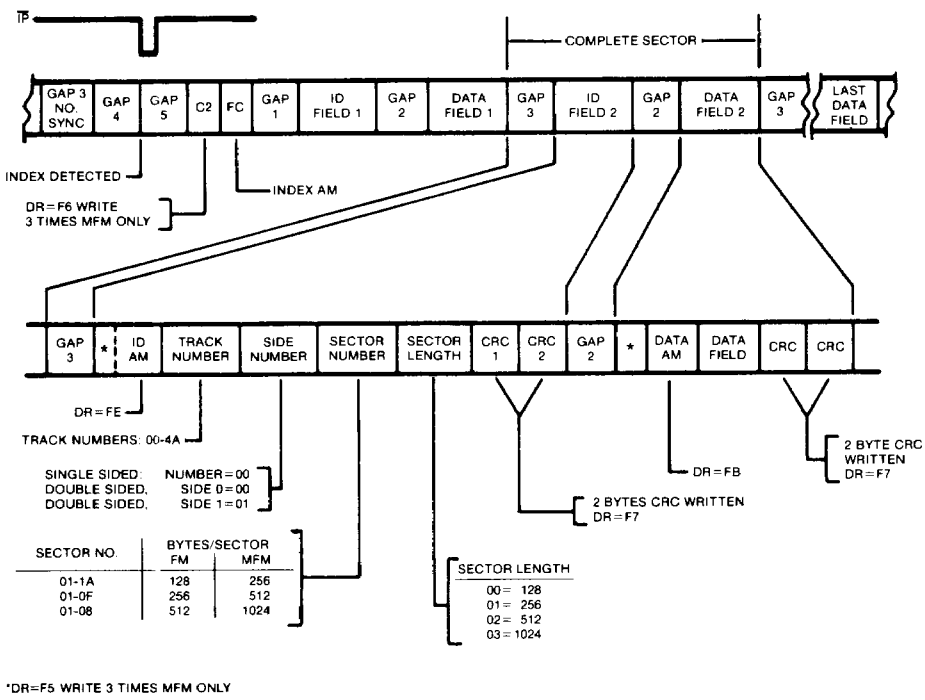


Figure 2. IBM Compatible Sector/Track Format

time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 2 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as an AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting.

Type IV Commands

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 3 tabulates the Type IV command option bits.

The four bits, I_0-I_3, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If I_0-I_3 are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for I_3=1 (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with I_0-I_3 all low.

Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated when there is *not* another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 4 illustrates the meaning of the status bits for each command.

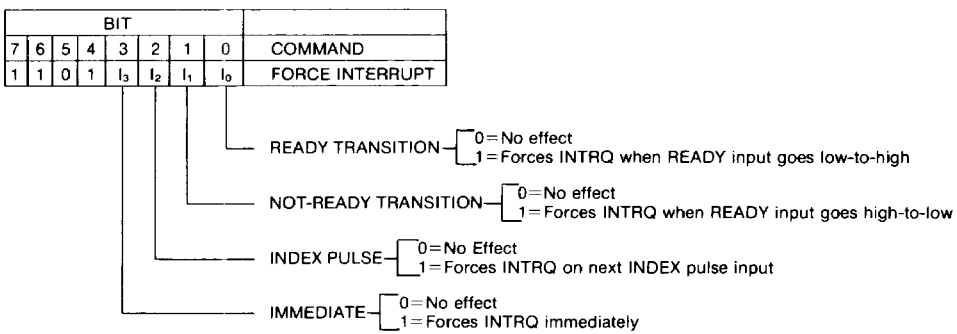


Figure 3. Force Interrupt Command Flags

Figure 4A. Status Register Summary

COMMAND	STATUS BIT							
	7	6	5	4	3	2	1	0
ALL TYPE I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
READ SECTOR	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
WRITE SECTOR	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACK	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

Figure 4B. Status Description for Type I Commands

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0	BUSY	When set command is in progress. When reset no command is in progress.

Figure 4C. Status Description for Type II and III Commands

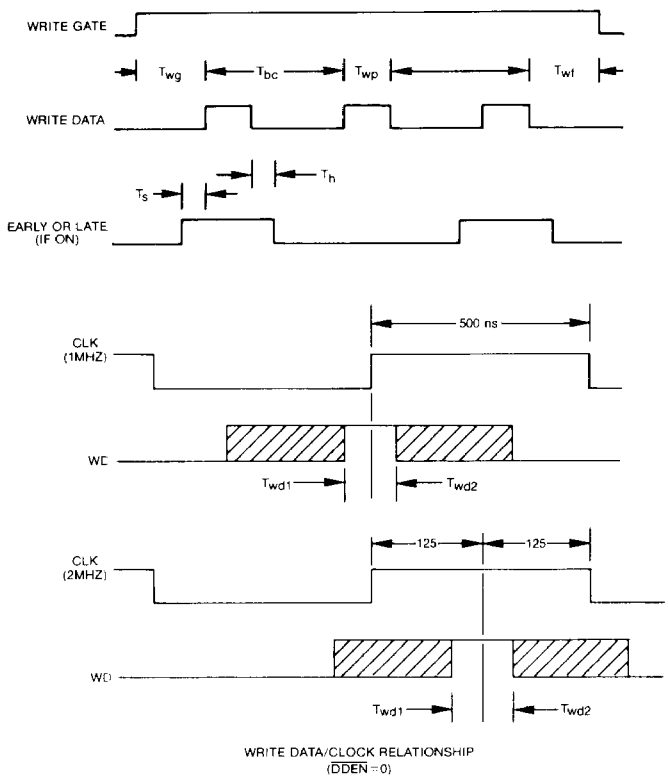
BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1=Deleted Data Mark. 0=Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

Write Data Timing:

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Write Data Pulse Width	T_{wp}	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Write Gate to Write Data	T_{wg}		2		μsec	FM
			1		μsec	MFM
Write data cyle Time	T_{bc}		2, 3, or 4		μsec	$\pm$CLK Error
Early (Late) to Write Data	T_s	125			nsec	MFM
Early (Late) From Write Data	T_h	125			nsec	MFM
Write Gate off from WD	T_{wf}		2		μsec	FM
			1		μsec	MFM
WD Valid to Clk	T_{wd1}	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
WD Valid after Clk	T_{wd2}	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ

These values are doubled when CLK=1 MHz.

Write Data Timing



WRITE DATA/CLOCK RELATIONSHIP
(DDEN=0)

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+15V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5% unless otherwise noted)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS							
Input Voltage Levels							
Low Level, V_{IL}					0.8	V	
High Level, V_{IH}			2.6			V	
Output Voltage Levels							
Low Level V_{OL}					0.45	V	I_{OL}=1.6 mA
High Level V_{OH}			2.8			V	I_{OH}=100 μA
Output Leakage, I_{LO}					10	μA	$V_{OUT}=V_{DD}$
Input Leakage, I_{IL}					10	μA	$V_{IN}=V_{DD}$
Output Capacitance				5		pf	
Input Capacitance				10		pf	
Power Dissipation					500	mW	
AC CHARACTERISTICS							
Processor Read Timing							
Address Setup Time		t_{SETR}	50			ns	Figure 5
Address Hold Time		t_{HLDR}	10			ns	Figure 5
$\overline{RE}$ Pulse Width (C_L=50pF)		t_{RE}	400			ns	Figure 5
DRQ Reset Time		t_{DRR}			500	ns	Figure 5
INTRQ Reset Time		t_{IRR}		500*	3000*	ns	Figure 5
Data Delay Time (C_L=50pF)		t_{DACC}			350	ns	Figure 5
Data Hold Time (C_L=50pF)		t_{DOH}	50		150	ns	Figure 5
Microprocessor Write Timing							
Address Setup Time		t_{SETW}	50			ns	Figure 6
Address Hold Time		t_{HLDW}	10			ns	Figure 6
WE Pulse Width		t_{WE}	350			ns	Figure 6
DRQ Reset Time		t_{DRR}			500	ns	Figure 6
INTRQ Reset Time		t_{IRR}		500*	3000*	ns	Figure 6
Data Setup Time		t_{DS}	250			ns	Figure 6
Data Hold Time		t_{DH}	70			ns	Figure 6
Disk Input Data Timing							
RAWREAD Pulse Width		t_{pw}	100*	200		ns	Figure 7, See Note
Clock Setup Time		t_d	40			ns	Figure 7 See Note
Clock Hold Time for MFM		t_{cd}	40			ns	Figure 7
Clock Hold Time for FM		t_{cs}	40			ns	Figure 7
RAWREAD Cycle Time		t_{bc}	1500			ns	1800 at 70°C, Figure 7
RCLK High Pulse Width	MFM	t_a	0.8	1*		μs	Figure 7
	FM		0.8	2*		μs	Figure 7
RCLK Low Pulse Width	MFM	t_b	0.8	1*		μs	Figure 7
	FM		0.8	2*		μs	Figure 7
RCLK Cycle Time	MFM	t_c		2*		μs	Figure 7
	FM			4*		μs	Figure 7
Miscellaneous Timing							
CLK Low Pulse Width		t_{CD1}	230	250	20000	ns	Figure 8
CLK High Pulse Width		t_{CD2}	200	250	20000	ns	Figure 8
STEP Pulse Width	MFM	t_{STP}	2*			μs	Figure 8
	FM		4*			μs	Figure 8
DIRC Setup Time		t_{DIR}		12		μs	Figure 8
MR Pulse Width		t_{MR}	50*			μs	Figure 8
IP Pulse Width		t_{IP}	10*			μs	Figure 8
WF Pulse Width		t_{WF}	10*			μs	Figure 8
CLK Cycle Time		t_{CYC}		0.5*		μs	Figure 8

*: These Values are doubled when CLK=1 MHz.

Figure 5. Microprocessor Read Timing

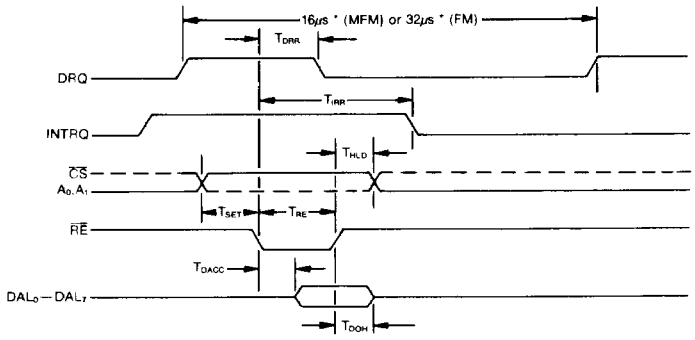


Figure 6. Microprocessor Write Timing

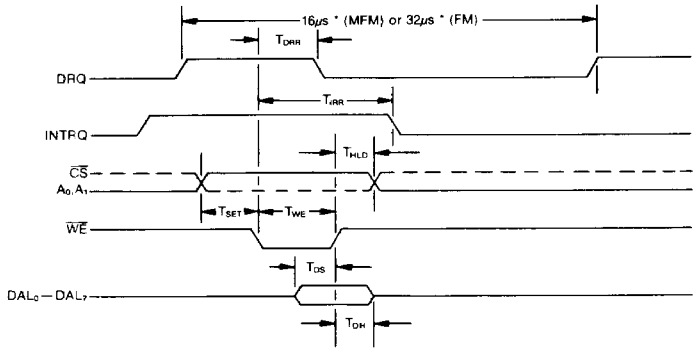
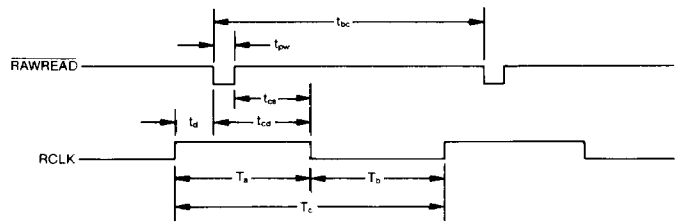
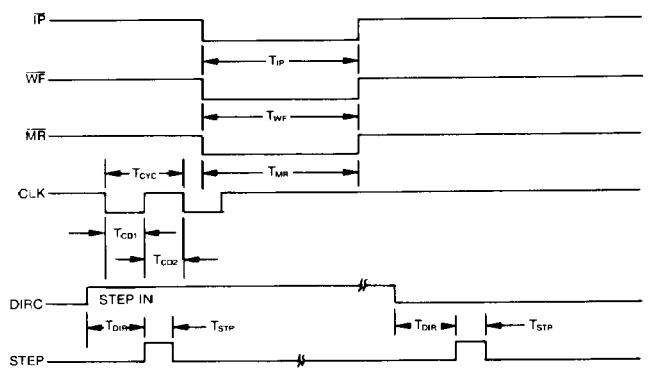


Figure 7. Disk Input Timing



Note: Pulse width on RAW READ (Pin 27) is normally 10-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.

Figure 8. Miscellaneous Timing



Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 9.

IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 10.

Non-IBM Formats

Unique (non-IBM) formats are permissible providing the following restrictions are understood.

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 11.

DATA BYTE (hex)	NO. OF BYTES	COMMENTS
FF	40	Gap 5 (Post Index)
00	6	
FC	1	Index AM
FF	26	Gap 1
00	6	
FE	1	ID AM
XX	1	Track Number (00-4C)
0X	1	Side Number (00 or 01)
XX	1	Sector Number (01-1A)
00	1	Sector Length (128 bytes)
F7	1	Causes 2-Byte CRC to be Written
FF	11	Gap 2 (ID Gap)
00	6	
FB	1	Data AM
E5	128	Data Field
F7	1	Causes 2-Byte CRC to be Written
FF	27	Part of Gap 3 (Data Gap)
FF	247 ②	Gap 4 (Pre Index)

ONE SECTOR ①

Figure 9. Byte Sequence for IBM 3740 Formatting

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX FF UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT

DATA BYTE (hex)	NO. OF BYTES	COMMENTS
4E	80	Gap 5 (Post Index)
00	12	
F6	3	Writes C2
FC	1	Index AM
4E	50	
00	12	Gap 1
F5	3	Writes A1
FE	1	ID AM
XX	1	Track Number (00-4C)
0X	1	Side Number (00 or 01)
XX	1	Sector Number (01-1A)
01	1	Sector Length (256 Bytes)
F7	1	Causes 2-Byte CRC to be Written
4E	22	Gap 2 (ID Gap)
00	12	
F5	3	Writes A1
FB	1	Data AM
40	256	Data Field
F7	1	Causes 2-Byte CRC to be Written
4E	54	Part of Gap 3 (Data Gap)
4E	598 ②	Gap 4 (Pre Index)

ONE SECTOR ①

Figure 10. Byte Sequence for IBM System-34 Formatting

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX 4E UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT.

GAP	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)	NOTE
Gap 1	16 bytes FF	16 bytes 4E	2
Gap 2	11 bytes FF 6 bytes 00	22 bytes 4F 12 bytes 00 3 bytes A1	1
Gap 3	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1	2
Gap 4	16 bytes FF	16 bytes 4E	2

NOTES: 1. THESE BYTES COUNTS ARE EXACT.
2. THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1, WHICH IS EXACT.

Figure 11. Gap Size Limitations