



T-45-19-05

SP8630A & B

600MHz ÷ 10

The SP8630 is an asynchronous emitter coupled logic counter which provides an ECL compatible output when used with an external pulldown resistor. It requires an AC coupled input of 600mV p-p.

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 350mW
- Temperature Range:
 - 55°C to +125°C (A Grade)
 - 30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

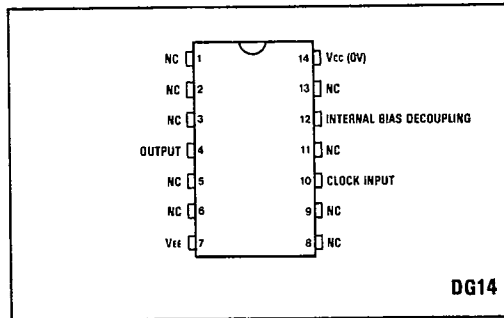


Fig.1 Pin connections - top view

DG14

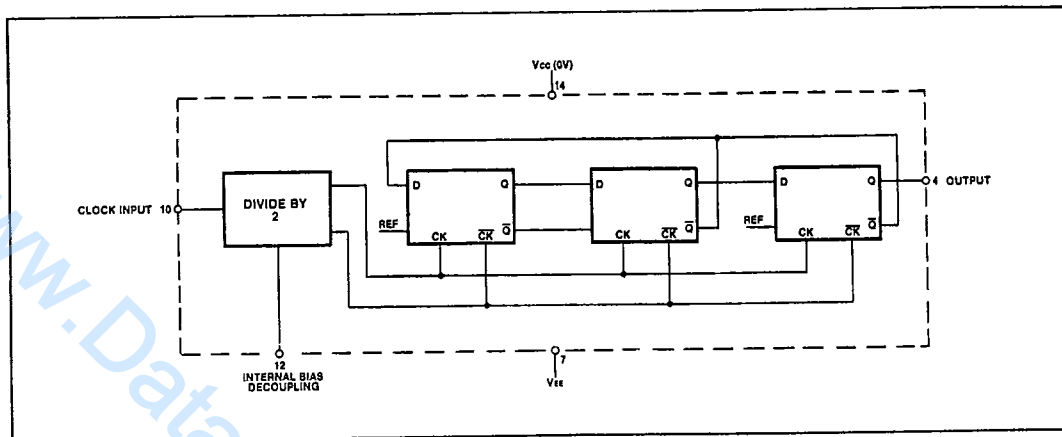


Fig.2 Functional diagram

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ELECTRICAL CHARACTERISTICS

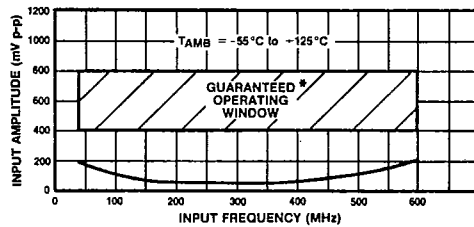
Supply voltage: $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 0.25V$
 Temperature: A Grade $T_{amb} = -55^{\circ}C$ to $+125^{\circ}C$
 B Grade $T_{amb} = -30^{\circ}C$ to $+70^{\circ}C$

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Characteristics	Symbol	Value		Units	Conditions	Note
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		70	mA	$V_{EE} = -5.2V$	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	$V_{EE} = -5.2V$ (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	$V_{EE} = -5.2V$ (25°C)	
Minimum output swing	V_{OUT}	400		mV	$V_{EE} = -5.2V$	

NOTES

1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of $V_{OH} = +1.63mV/^{\circ}C$ and $V_{OL} = +0.94mV/^{\circ}C$ but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



* Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8630A

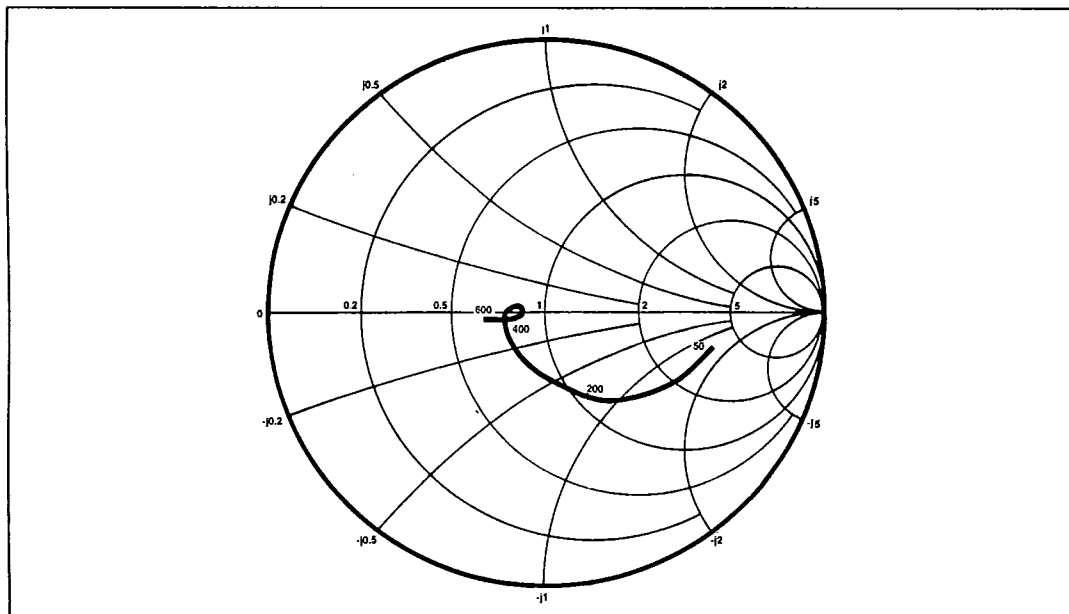


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

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1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than $100V/\mu s$.
3. The outputs are compatible with ECL II. There is an

- internal load of 3k at output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
4. Input impedance is a function of frequency. See Fig.4.
5. All components should be suitable for the frequency in use.

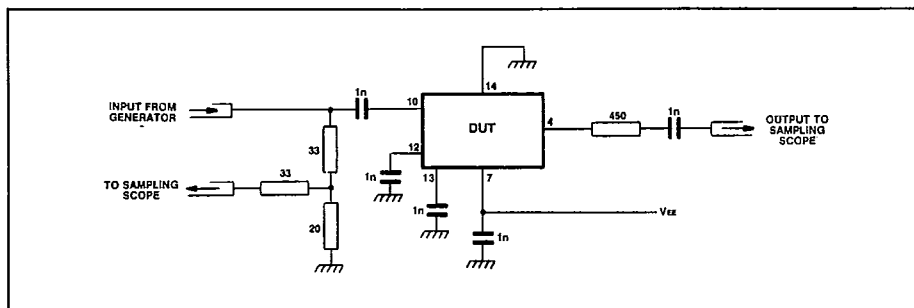


Fig.5 Test circuit

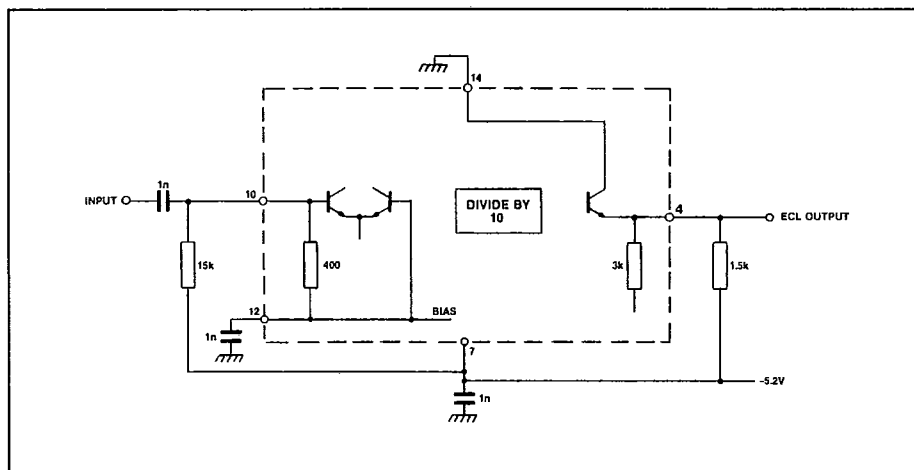


Fig.6 Typical application showing interfacing