- **CMOS Low Power Consumption**
- **2 Voltage Detectors Built-in**
- **Detect Voltage Accuracy: ±2%**
- **Detect Voltage Range: 1.5V ~ 5.0V**
- **SOT-25 Package**

Applications

- Memory battery back-up circuitry
- Microprocessor reset circuits
- Power failure detection
- System power-on reset circuits
- System battery life monitors and re-charge voltage monitors
- Delay circuitry

General Description

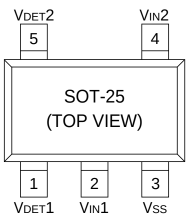
The XC612 series consist of 2 voltage detectors, in 1 mini-molded, SOT-25 package.
The series provides accuracy and low power consumption through CMOS processing and laser trimming and consists of a highly accurate voltage reference source, 2 comparators, hysteresis and output driver circuits.
The input ($V_{IN}1$) for voltage detector 1 (VD1) dually functions as the power supply pin for both detector 1 (VD1) and detector 2 (VD2).

Features

Highly accurate: Set-up voltage accuracy ±2%
Low-power consumption: Typ.2.0μA ($V_{IN}1$=$V_{IN}2$=2.0V, quiescent state)
Detect voltage: 1.5V ~ 5.0V programmable in 0.1V steps.
Detector's voltages can be set-up independently
Operating Voltage Range: 1.5V ~ 10.0V
Temperature characteristics: ±100ppm/℃
Output configuration: N-channel open drain
Small package: SOT-25 (150mW) mini-mold

* CMOS Output is under development

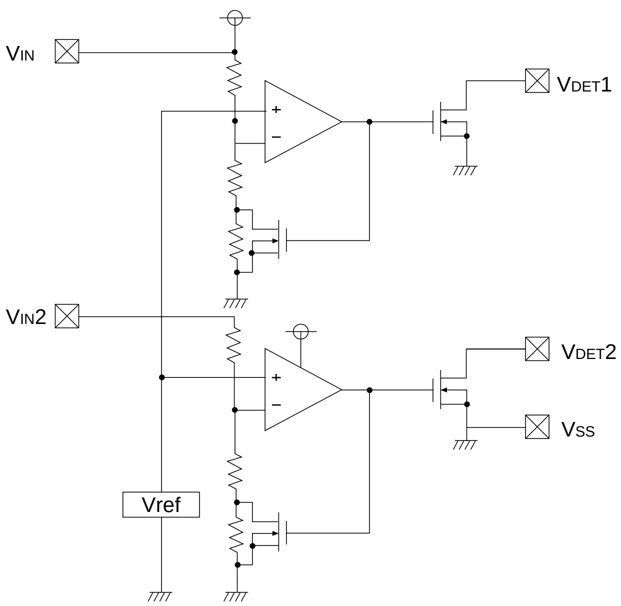
Pin Configuration



Pin Assignment

PIN NUMBER	PIN NAME	FUNCTION
1	$V_{DET}1$	Voltage Detector 1 output
2	$V_{IN}1$	Detector 1 input, Power Supply.
3	V_{SS}	Ground
4	$V_{IN}2$	Voltage Detector 2 Input
5	$V_{DET}2$	Voltage Detector 2 Output

Block Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	UNITS
Input Voltage $V_{IN}1$	$V_{IN}1$	12	V
Input Voltage $V_{IN}2$	$V_{IN}2$	V_{SS}–0.3 ~ $V_{IN}1$+0.3	V
Output Voltage $V_{DET}1$	$V_{VDET}1$	V_{SS}–0.3 ~ 12	V
Output Current $V_{DET}1$	$I_{VDET}1$	50	mA
Output Voltage $V_{DET}2$	$V_{VDET}2$	V_{SS}–0.3 ~ 12	V
Output Current $V_{DET}2$	$I_{VDET}2$	50	mA
Power Dissipation	Pd	150	mW
Operating Ambient Temperature	Topr	–30 ~ +80	℃
Storage Temperature	Tstg	–40 ~ +125	℃

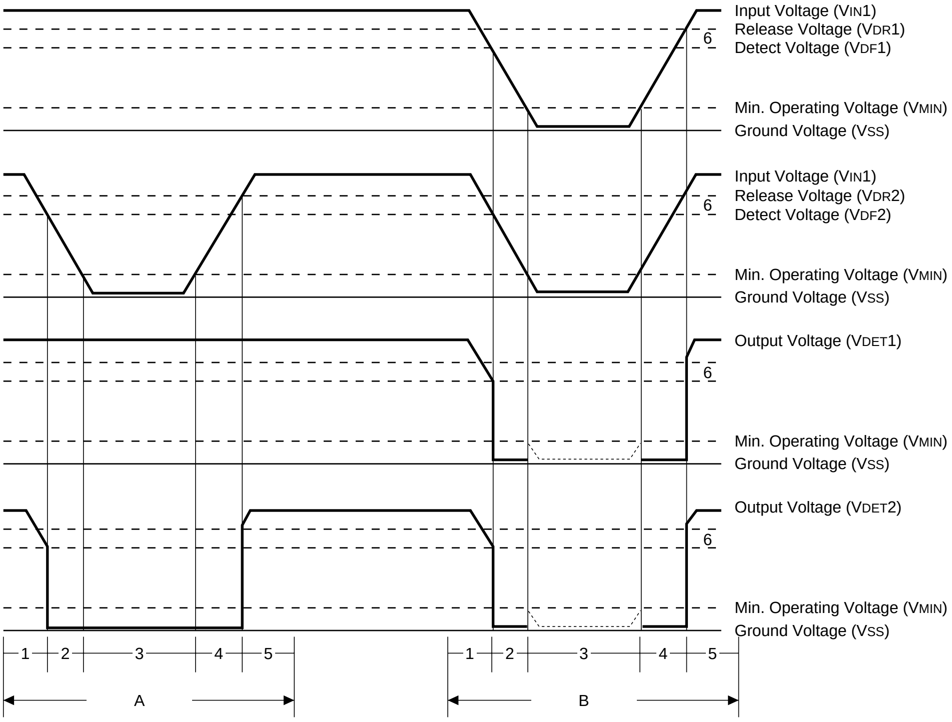
1

Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage VDET1	VDF1	Voltage when VDET1 changes from H to L following a reduction of VIN1	VDF1 x 0.98	VDF1	VDF1 x 1.02	V	1
Detect Voltage VDET2	VDF2	Voltage when VDET2 changes from H to L following a reduction of VIN2	VDF2 x 0.98	VDF2	VDF1 x 1.02	V	1
Hysteresis Range 1	VHYS1	Voltage (VDR1) - VDF1 when VDET1 changes from L to H following an increase of VIN1	VDF1(T) x 0.02	VDF1(T) x 0.05	VDF1(T) x 0.08	V	1
Hysteresis Range 2	VHYS2	Voltage (VDR2) - VDF2 when VDET2 changes from L to H following an increase of VIN2	VDF2(T) x 0.02	VDF2(T) x 0.05	VDF2(T) x 0.08		1
Supply Current	ISS	VIN1=1.5V 2.0V 3.0V 4.0V 5.0V		1.35 1.50 1.95 2.40 3.00	3.90 4.50 5.10 5.70 6.30	μA	2
Input Current VIN2	IIN2	VIN1=1.5V 2.0V 3.0V 4.0V 5.0V		0.45 0.50 0.65 0.80 1.00	1.30 1.50 1.70 1.90 2.10	μA	2
Operating Voltage	VIN	VDF (T) = 1.5V to 5.0V	1.5		10	V	–
Output Current*	IVDET	Nch VDS = 0.5V VIN=1.0V VIN=2.0V VIN=3.0V VIN=4.0V VIN=5.0V	 0.3 3.0 5.0 6.0 7.0	 2.2 7.7 10.1 11.5 13.0		mA	3
Temperature Characteristics*	ΔVDF / ΔTopr・VDF	–30℃ ≦ Topr ≦ 80℃		±100	–	ppm/℃	–
Transient Delay Time* (Release Voltage→Output Conversion)	tDLY	(VDR→VOUT conversion)			0.2	ms	4

1. VDF1(T), VDF2(T) : User specified detect voltage.
2. Release voltage (VDR) = VDF +VHYS
3. Those parameters marked with an asterisk apply to both VDET1 and VDET2.
4. Input Voltage : please ensure that VIN1 ≧ VIN2

■ Timing Chart (Pull up voltage =Input voltage $V_{IN}1$)



■ Operational Notes

Timing Chart A ($V_{IN}1$=voltages above release voltage, $V_{IN}2$=sweep voltage)

Because a voltage higher than the minimum operating voltage is applied to the voltage input pin (V_{IN}), ground voltage will be output at the output pin (V_{DET}) during stage 3. (Stages 1, 2, 4, 5 are the same as in B below).

Timing Chart B ($V_{IN}1$=$V_{IN}2$)

1. When a voltage greater than the release voltage (V_{DR}) is applied to the voltage input pin ($V_{IN}1$, $V_{IN}2$), input voltage ($V_{IN}1$, $V_{IN}2$) will gradually fall.
   When a voltage greater than the detect voltage (V_{DF}) is applied to the voltage input pin ($V_{IN}1$, $V_{IN}2$), a state of high impedance will exist at the output pin ($V_{DET}1$, $V_{DET}2$), so should the pin be pulled up, voltage will be equal to pull up voltage.

2. When input voltage ($V_{IN}1$, $V_{IN}2$) falls below detect voltage (V_{DF}), output voltage ($V_{DET}1$, $V_{DET}2$) will be equal to ground level (V_{SS}).

3. Should input voltage ($V_{IN}1$, $V_{IN}2$) fall below the minimum operational voltage (V_{MIN}), output will become unstable. Should $V_{IN}2$ fall below VMIN, voltage at the output pin ($V_{DET}2$) will be equal to ground level (V_{SS}) if the power supply ($V_{IN}1$) is within the operating voltage range.
   *In general the output pin is pulled up so output will be equal to pull up voltage.

4. Should input voltage ($V_{IN}1$, $V_{IN}2$) rise above ground voltage (V_{SS}), output voltage ($V_{DET}1$, $V_{DET}2$) will equal ground level until the release voltage level (V_{DR}) is reached.

5. When input voltage ($V_{IN}1$, $V_{IN}2$) rises above release voltage, the output pin's ($V_{DET}1$, $V_{DET}2$) voltage will be equal to the voltage dependent on pull up.

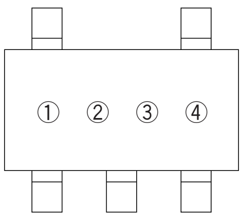
Note : The difference between release voltage (V_{DR}) and detect voltage (V_{DF}) is the Hysteresis Range (6).

Ordering Information

XC612xxxxxMx
a b c d e

DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Output Configuration: N=N-Channel Open Drain	d	Package Type: M=SOT-25
b	Detect Voltage (V_{DET1}) e.g.25=2.5V 38=3.8V		
c	Detect Voltage (V_{DET2}) e.g.33=3.3V 50=5.0V	e	Device Orientation R=Embossed Tape (Orientation of Device: Right) L=Embossed Tape (Orientation of Device: Left)

Marking



SOT-25
(TOP VIEW)

① Represents the output configuration

SYMBOL	CONFIGURATION
N	Nch open drain

②③ Represents the entry order.

④ Denotes the production lot Number

0 to 9, A to Z repeated. (G, I, J, O, W excepted)

Notes on Use

1. Please ensure that input voltage V_{IN2} is less than V_{IN1} + 0.3V. (refer to N.B. 1 below)

2. With a resistor connected between the V_{IN1} pin and the input, oscillation is liable to occur as a result of through current at the time of release. (refer to N.B. 2 below)

3. With a resistor connected between the V_{IN1} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN1} pin.

4. In order to stabilise the IC's operations, please ensure that the V_{IN1} pin's input frequency's rise and fall times are more than 5 µ sec/V.

5. Should the power supply voltage V_{IN1} exceed 6V, voltage detector 2's detect voltage (V_{DF2}) and the release voltage (V_{DR2}) will shift somewhat.

6. Please use this IC within the specified maximum absolute ratings.

N.B.

1. Voltage detector 2's input voltage (V_{IN2})
   An input protect diode is connected from input detector 2's input (V_{IN2}) to input detector 1's input. Therefore, should the voltage applied to V_{IN2} exceed V_{IN1}, current will flow through V_{IN1} via the diode. (refer to diagram1)

2. Oscillation as a result of through current
   Since the XC612 series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations. (refer to diagram 2)
   Since hysteresis exists during detect operations, oscillation is unlikely to occur.

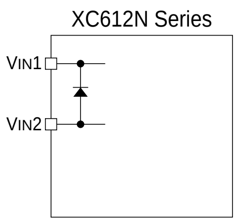


Diagram 1. Voltage detector 2's input voltage V_{IN2}

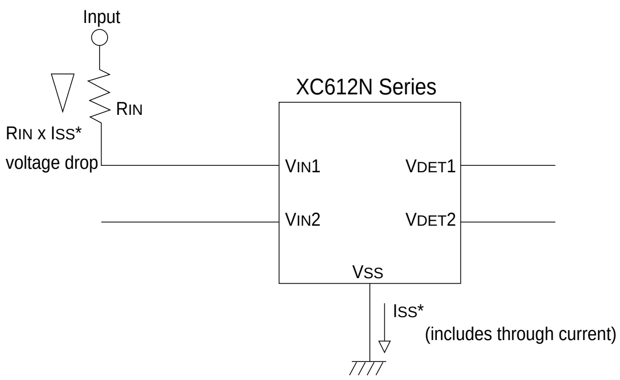
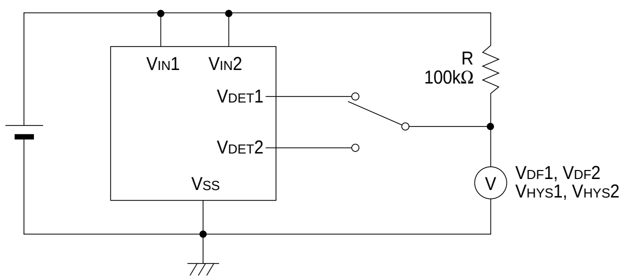


Diagram 2. Through current oscillation

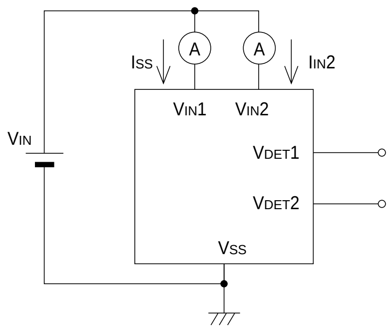
1

■ Standard Circuits

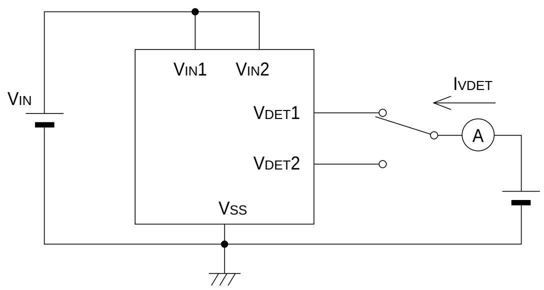
Circuit 1.



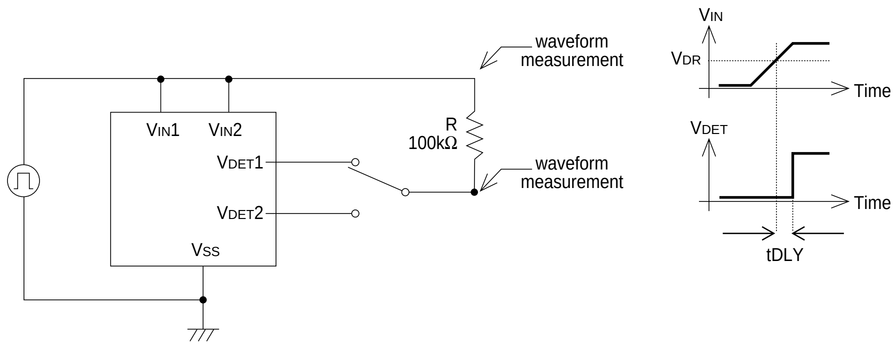
Circuit 2.



Circuit 3.

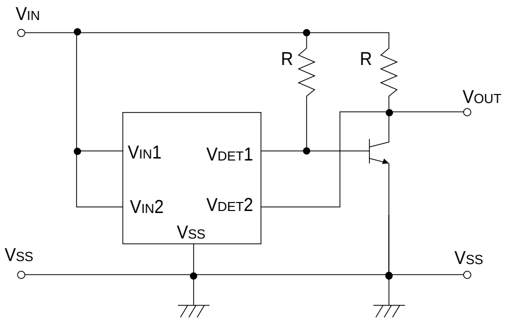


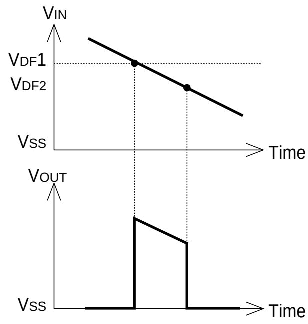
Circuit 4.



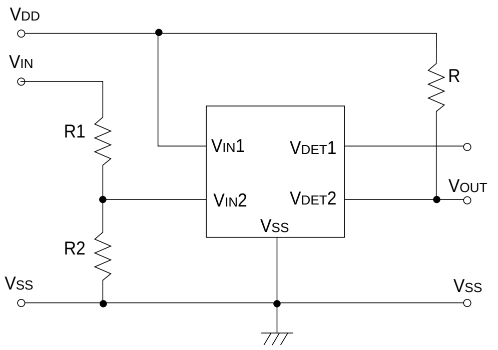
Typical Application Circuits

● Window comparator circuit





● Detect voltages above respective established voltages circuit



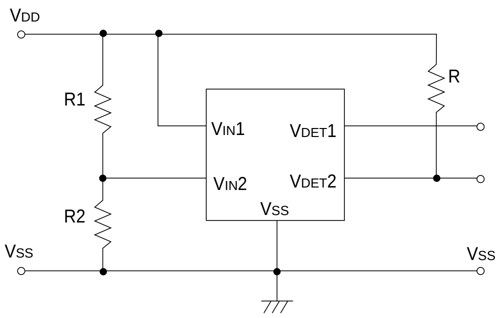
Notes on resistors R1 and R2's (1), (2) functions :

Detect voltage = { (R1 + R2) ÷ R2} x $V_{DF}2$ (1)
N.B. $V_{DF}2$ = detect voltage VD2

Please set-up so that
Hysteresis ($V_{HYS}2$) = { (R1 + R2) ÷ } x $V_{HYS}2$ (2)

Note : Please ensure that input voltage 2 ($V_{IN}2$) is less than $V_{IN}1$ + 0.3V

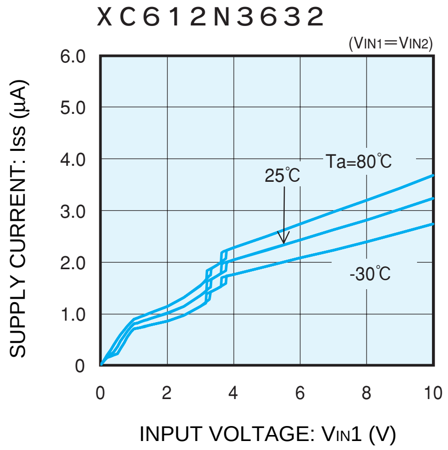
● Voltage detect circuit with delay built-in

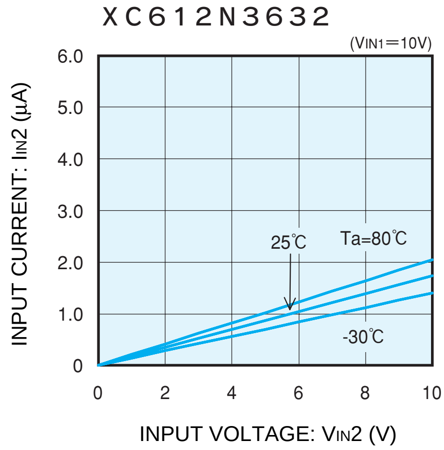


Note : Delay operates at both times of release and detect operations.

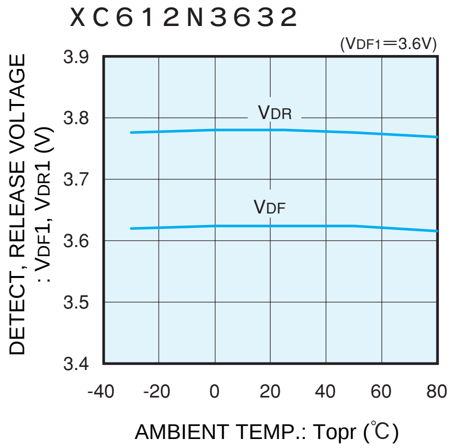
XC612 Electrical Characteristics

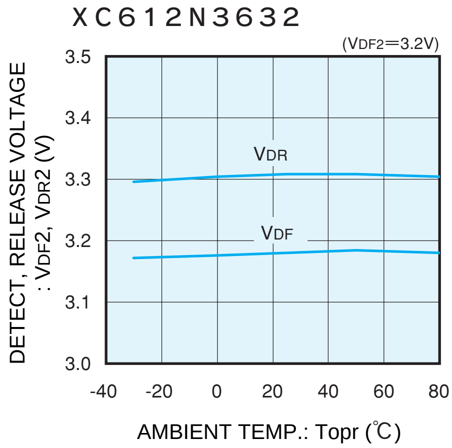
(1) SUPPLY CURRENT vs. INPUT VOLTAGE





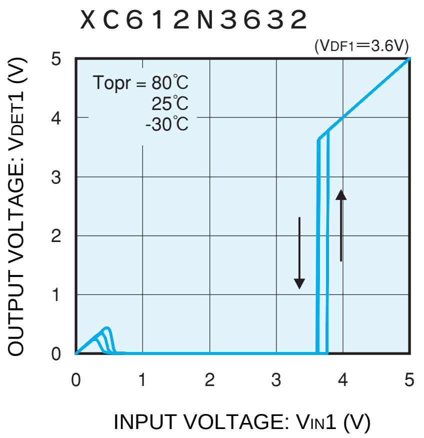
(2) DETECT & RELEASE VOLTAGE vs. AMBIENT TEMPERATURE

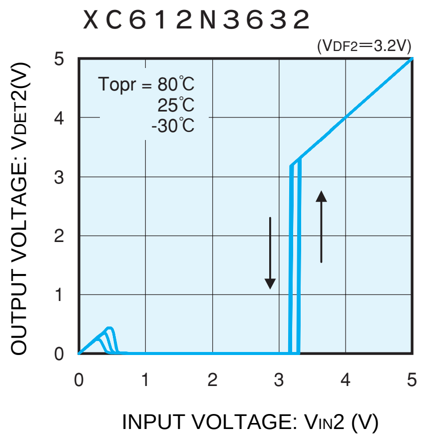




Note : Unless otherwise stated, pull up resistance = 100kΩ with Nch open drain output types.

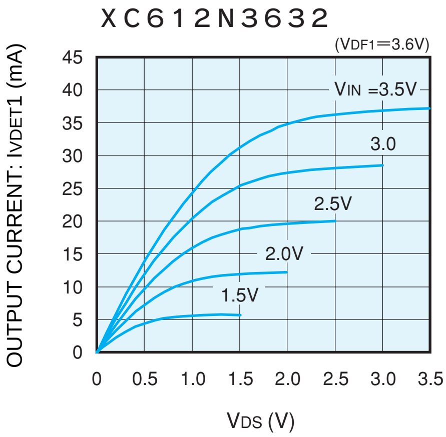
(3) OUTPUT VOLTAGE vs. INPUT VOLTAGE

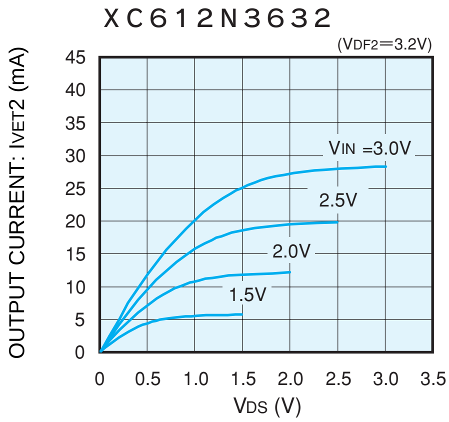


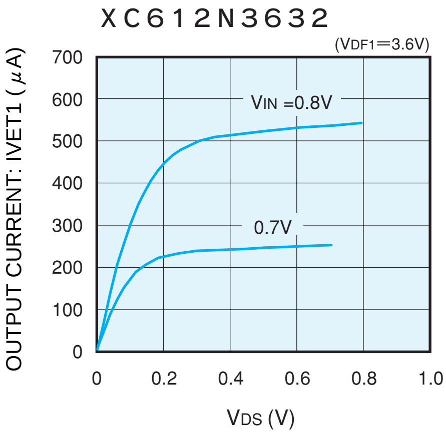


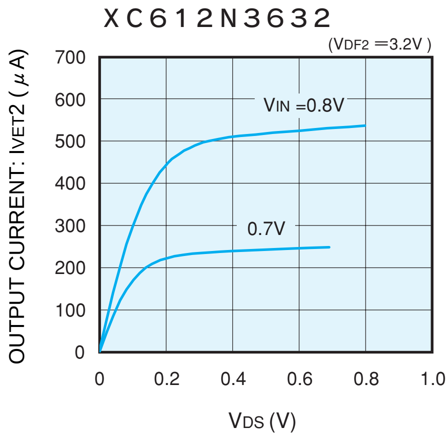
XC612 Electrical Characteristics

(4) N-CH DRIVER OUTPUT CURRENT vs. VDS









(5) N-CH DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE