ADVANCE INFORMATION

Am29LV104B

4 Megabit (512 K x 8-Bit)
CMOS 3.0 Volt-only, Boot Sector 32-Pin Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.35 µm process technology**
- **High performance**
  - — Full voltage range: access times as fast as 70 ns
  - — Regulated voltage range: access times as fast as 55 ns
- **Ultra low power consumption**
  - — Automatic sleep mode: 1 µA (typical values at 5 MHz)
  - — Standby mode: 1 µA
  - — Read mode: 7 mA
  - — Program/erase mode: 15 mA
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors
  - — Any combination of sectors can be erased; supports full chip erase
  - — Sector Protection features:

    Hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked via programming equipment
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Embedded Algorithms**
  - — Embedded Erase algorithms automatically preprogram and erase the entire chip or any combination of designated sectors
  - — Embedded Program algorithms automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write/erase cycles guaranteed**
- **Package option**
  - — 32-pin PLCC
  - — 32-pin TSOP
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase cycle completion
- **Erase Suspend/Resume**
  - — Supports reading data from or programming data to a sector not being erased

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GENERAL DESCRIPTION

The Am29LV104B is a single power supply, 4 Mbit, 3.0 Volt-only Flash memory device organized as 524,288 bytes. The data appears on DQ0-DQ7. The device is available in 32-pin PLCC and 32-pin TSOP packages. All read, erase, and program operations are accomplished using only a single power supply. The device can also be programmed in standard EPROM programmers.

The device offers access times of 55, 70, 90, and 120 ns allowing high speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate control pins—chip enable (CE#), write enable (WE#), and output enable (OE#)—to control normal read and write operations.

The device requires only a **single power supply** (2.7 V–3.6V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This is achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

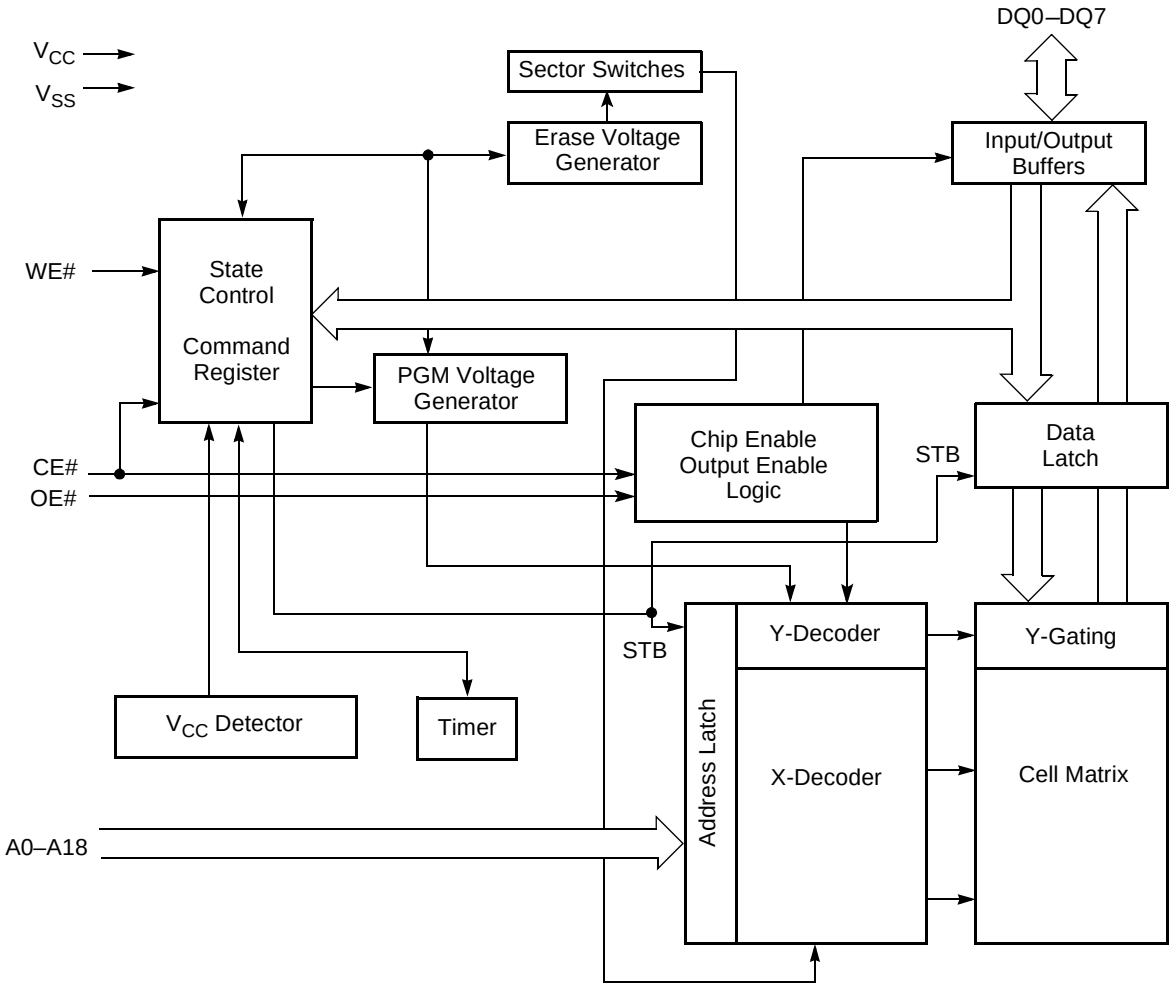
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

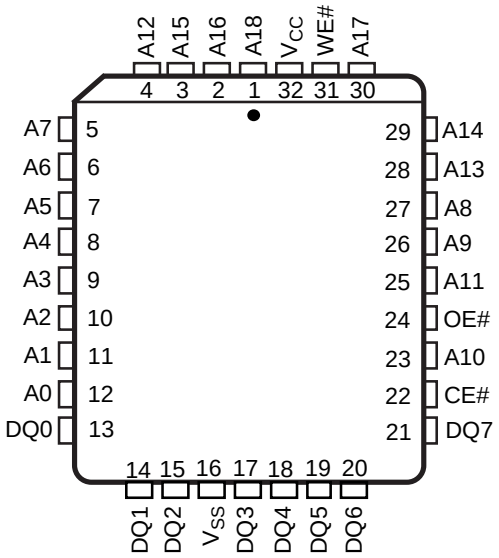
Family Part Number		Am29LV104B			
Speed Options	Regulated Voltage Range: V_{CC} =3.0–3.6 V	**-55R**			
	Full Voltage Range: V_{CC} = 2.7–3.6 V		**-70**	**-90**	**-120**
Max access time, ns (t_{ACC})		55	70	90	120
Max CE# access time, ns (t_{CE})		55	70	90	120
Max OE# access time, ns (t_{OE})		30	30	30	35

Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS



32-Pin PLCC

21353A-2

CONNECTION DIAGRAMS

32-pin Standard TSOP

32-Pin Reverse TSOP

21353A-3

PIN CONFIGURATION

A0–A18 = 19 address inputs

DQ0–DQ7 = 8 data inputs/outputs

CE# = Chip enable

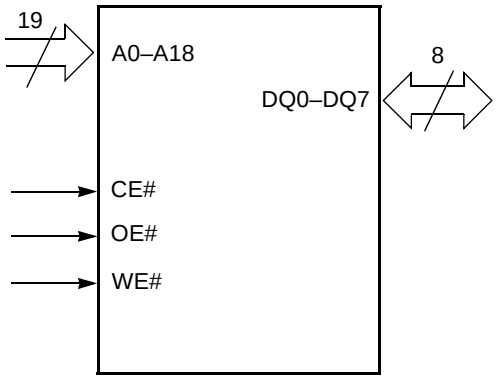
OE# = Output enable

WE# = Write enable

V_{CC} = 3.0 volt-only single power supply
(see Product Selector Guide for speed options and voltage supply tolerances)

V_{SS} = Device ground

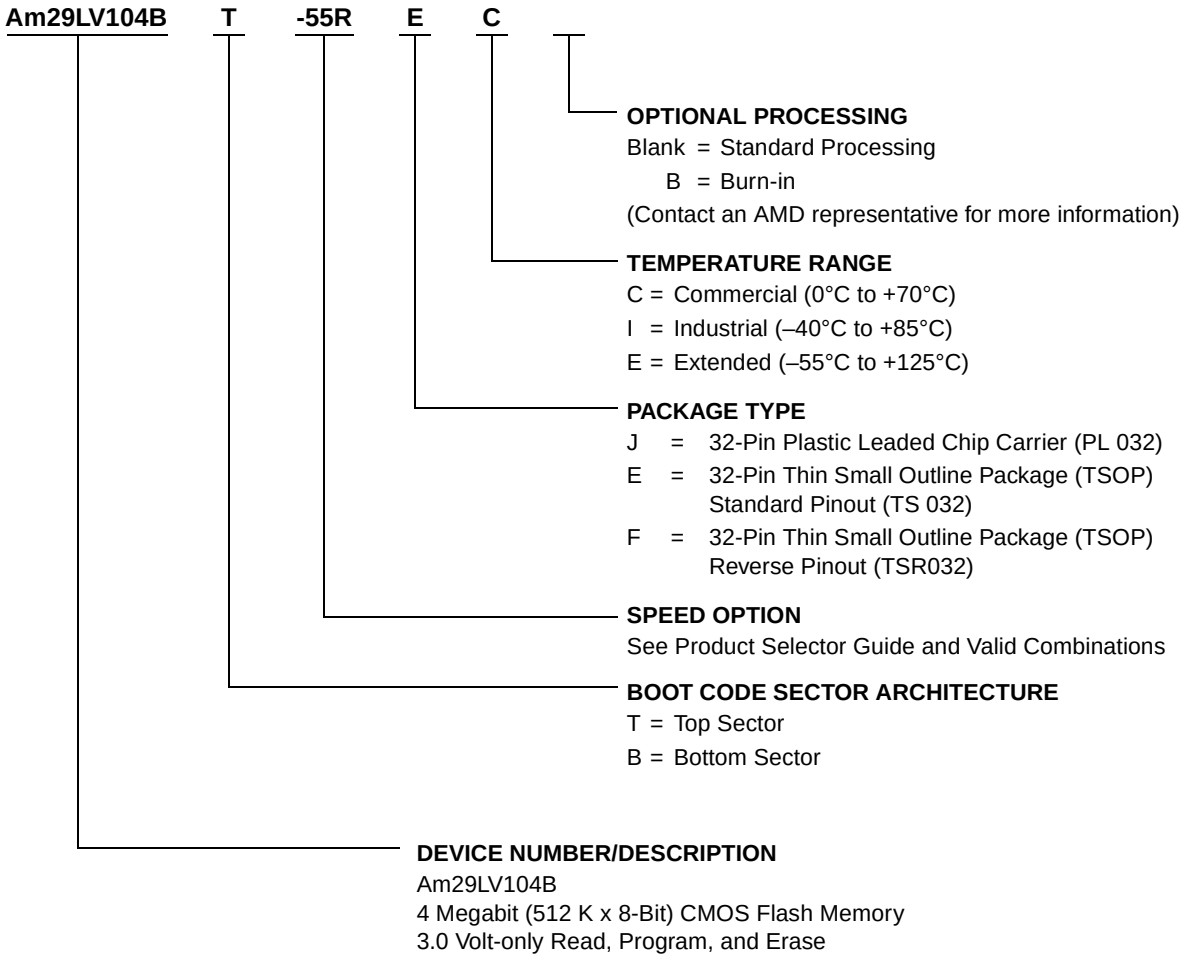
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am29LV104B-55R	JC, JI, EC, EI, FC, FI
Am29LV104B-70	JC, JI, JE, EC, EI, EE, FC, FI, FE
Am29LV104B-90	
Am29LV104B-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Trademarks