Features

- **13.56 MHz ± 7 kHz RFID IC for Cards and Tags**
- **320 Read/Write EEPROM Bits, Divided into 10 Pages of 32 Bits**
- **Supports ISO/IEC 14443-2 Type B**
- **Optional 2-byte CRC**
- **Password and Write Lock Protection**
- **Programmable Send and Receive Protocols**
- **Supports Multiple Tags (Anticollision)**
- **Integrated up to 70 pF Tuning Capacitor (Mask Selectable)**
- **ID Length Programmable from 4 to 19 Bytes**
- **106 Kbits/sec Data Rate**

13.56 MHz RFID Transponder IC

AT88RF256-13

Description

The device is intended to be used in identification applications where one or more ID tags will be in the field at one time. It contains 320 bits of full read/write EEPROM memory, and offers features such as passwords, locking and a variable length ID. It is electrically compatible with ISO/IEC14443-2 for Type B systems, communicating at 106 Kbits/sec. The IC includes an internal tuning capacitor – only an external coil antenna is required to form a complete tag.

Figure 1. Block Diagram

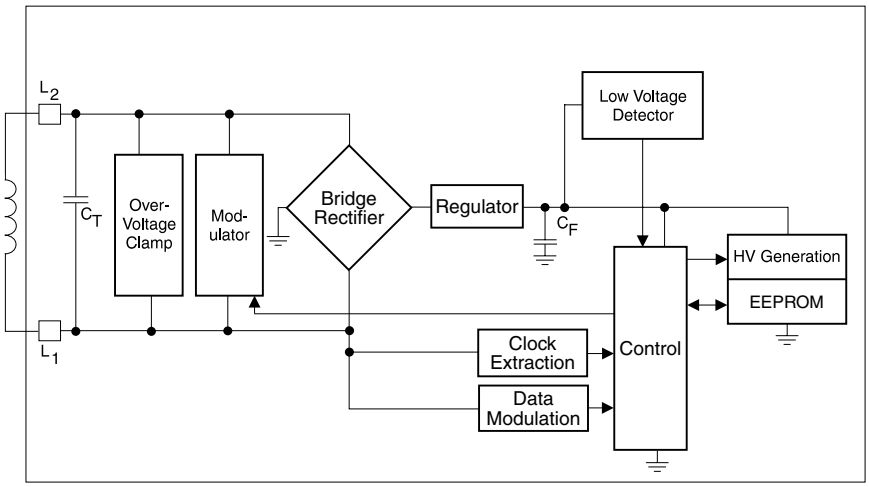
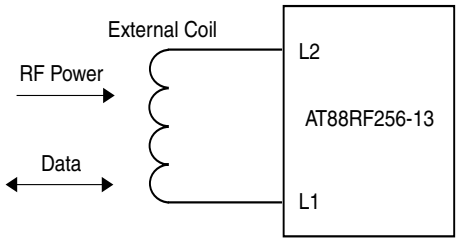


Figure 2. Typical Operating Configuration



Rev. 1944E–RFID–03/02

IC Operation

Upon power-up, the IC will continuously repeat through the following sequence, which includes an ID transmission and possible reception of a command. The sequence is defined as follows:

1. Framed transmission of the ID field:
   - Start of Transmission (see *Data Communications* section)
   - Between 4 and 19 bytes from the EEPROM, which is defined as the ID field
   - Optional 2-byte CRC
   - End of Transmission (see *Data Communications* section)
2. A listening window, during which commands may be sent to the IC

All bits are sent to or read from the IC least significant bit first. Bit fields listed in this document are listed with the LSB on the left and the MSB on the right.

Multi-byte information is sent to the IC least significant byte first. Although not visible to the external system, within the IC the first byte sent to the IC is stored in memory at the lowest address and the address is incremented for subsequent bytes.

Information is read from the EEPROM and transmitted by the IC in exactly the same order in which it was written; the first bit written is the first bit read.

ID Field

The ID sent by the IC can be between 4 and 19 bytes in length, depending on the value of the PU_LEN field in the configuration page. EEPROM bytes not utilized for ID storage may be used by the system for any other purpose.

A serial number is programmed into page 7 of the IC at the Atmel factory. This ID is guaranteed to be unique for all dies, but is not locked and can be changed by the system.

CRC

When enabled by the CRC_ON option bit, a 2-byte CRC code will end all frame transmissions (either from the IC or from the reader/writer). The CRC polynomial used in this IC is identical to CRC_B as defined in ISO/IEC 14443-3: $x^{16} + x^{12} + x^5 + x^0$, or a hex polynomial of 1021.

The CRC register is initialized to 0xFFFF. When receiving information from the system, the IC computes the CRC on the incoming command, data and CRC bytes (start/stop bits, parity bits, SOT, EOT and EGT are ignored). When the last bit of the CRC has been received, the value in the CRC register should be 0. When the IC transmits data, the CRC is computed based on the data bits. The CRC is transmitted as the final 2 bytes of the frame.

Listening Window

After the power-up sequence is transmitted, there is a listening window during which the tag looks for modulation that would initiate the transmission of a command from the reader/writer to the tag. Commands sent at any other time are ignored.

The listening window is 8 bit-times long. The leading modulation edge of the SOT identifier (see *Data Communications* section) must not start within the first and/or last bit-time of the listening window. This restriction is enforced to prevent the IC receiver from seeing its own modulation.

Command Bytes

The explicit commands implemented in this tag permit the reader/writer to directly access individual 4-byte pages within the memory array, prevent future writing of particular pages (locking), temporarily disable the IC or check a password value. These commands are encoded as follows:

Table 1. Command Bytes

LSB	MSB
A_0 A_1 A_2 A_3 0 0 0 1	Read 32-bit Page A A A A (followed by optional CRC)
A_0 A_1 A_2 0 0 0 1 0	Write 32-bit Data Page A A A (followed by 4 bytes of data and optional CRC)
0 0 0 0 0 0 1 1	Write Lock Byte (followed by 1 byte of data, 3 bytes of $AAh and optional CRC)
0 0 0 1 0 0 1 1	Write Configuration Bits (followed by 1 byte of $AAh, 3 bytes of data and optional CRC)
0 0 0 0 0 1 1 1	Write Password (followed by 4 bytes of data and optional CRC)
0 0 0 1 1 0 0 0	Disable (Stop) IC until Power-down (followed by optional CRC)
0 0 0 1 1 1 0 0	Check Password (followed by 4 bytes of data and optional CRC)

For the Read and all four Write commands, the data stored within the corresponding page of the EEPROM to the accessed page is repeatedly transmitted back to the reader by the IC after the command has completed. This permits a verify function for the commands. For the Write Lock and Write Config commands, the entire contents of page 8 are transmitted. Between each frame transmitted, there is a listening window of 8 bit-times to synchronize the reader and/or permit the reader/writer to issue a new command to the IC. The listening window will begin immediately following the transmission of the appropriate EOT (see *Data Communications* section for information regarding EOT).

For the Read command, addresses 0 – 7 are used to select between the 32-bit data pages while an address value of 0x08 addresses the configuration page. Any attempts to read pages with addresses above 0x08 will cause the command to be aborted, and the IC will return to the header transmission sequence.

After the Check Password command, the IC goes back to the ID transmission loop and the reader/writer can issue its commands during the listening window. After the Disable command, the IC is held in reset until power is removed.

There are a number of features that are used to prevent inadvertent writing of the IC:

1. The proper command code plus the proper receive data encoding must be sent to the IC. If either an illegal code or improper encoding is detected, the command is aborted.
2. Optionally, 2 correct CRC bytes may be sent after the command and data bytes, which must also be correct (see below for details).
3. For the Write Lock command, a successful Write Page command must have been previously executed since the last power cycle in order for the Write Lock command to be executed.

If any of these protections are violated, or if there is a transmission or protection failure (lock bit set, password not entered), or if an illegal command is sent, the part will immediately restart its power-up read sequence.

Passwords

If the optional password mode is enabled with PW_ON, command-based Reads and Writes are prohibited until the correct password is sent using the Check Password command. If the transmitted value of the password is correct, then an internal latch is set and subsequent Read, Write and Lock commands (to any page, including the password page, #9) are permitted. If the wrong password is sent (to the password check), then the command is aborted, and the IC reverts to the normal power-up sequence. Writes to locked pages are never permitted regardless of passwords.

There is no command that can be used to directly read the password page, regardless of whether or not the password option (PW_ON) is enabled.

Data Locking

Within the lock byte, each lock bit determines whether the corresponding 4-byte user page can be written to. If it is a “1”, then Writes are prohibited; if “0”, they are allowed. The data sent to the IC with the Write Lock operation is OR’ed with the data already in the lock byte and then rewritten to the EEPROM. Once a user page is locked, it may never be unlocked and may never be written to.

There are two additional lock bits for pages 8 (CONFIG_LOCK) and 9 (PW_LOCK). They operate slightly differently from the user lock bits because there is no OR function. CONFIG_LOCK, if “1”, prevents the execution of the Write Config Bits command, while PW_LOCK, if “1”, prevents execution of the Write Password command. Turning on CONFIG_LOCK does not lock the value of the bits within the lock byte but does prevent further change to the PW_LOCK bit and the configuration page.

Multiple Tags

In order to support multiple tags within the field at the same time, a random delay time between ID transmissions can be enabled. This feature is implemented by having the IC randomly disable its activity (transmission of ID frame *and* enabling the listening window) at selected times. Commands are only honored during a listening window immediately following a frame transmission.

The IC includes a random generator that will generate different sequences of enablement/disablement based on processing, voltage, temperature and power-up time. Depending on the value of the RANDOM option, the transmission of an ID frame will be enabled on average once in eight times. The maximum delay is twice the average, while at the minimum, two ID frames/listening windows may be issued back-to-back.

To implement this feature, the tags must be programmed with error detection information within the ID field so that the reader can detect the condition when two tags transmit their ID at exactly the same time. Because of the random delay feature, in most cases the next transmissions for these two ICs will not overlap.

The Chip Disable command can be used with the random delay feature to permit an increased number of tags to be identified. Once a tag has been properly read by the reader unit, the reader sends the Chip Disable command to the tag during the first listening window after the ID transmission. Until the power is removed, that tag no longer sends its ID frame.

See the *Anticollision Procedures for the AT88RF256-13 Application Note* for additional information on utilizing the anticollision features of the IC.

Data Communications

The electrical signaling of the IC is configurable using configuration bits as in Table 4, page 12. Options exist to allow compatibility with ISO/IEC 14443-2, “Radio Frequency Power and Signal Interface” (version N409, Final Committee Draft 3/12/99) Type B mode. The frame formatting for the various modes of operation is not fully compliant with ISO/IEC 14443 and is defined below.

Data Encoding

The DATA_ENCODE bit determines the outgoing (IC to reader/writer) data encoding format.

Section 5 of ISO 14443 states that the reader shall talk first. The AT88RF256-13 talks first.

Section 9.2.5 of ISO 14443 defines Tr0 and Tr1. These signals are as stated and are not compliant.

Tr0 is the delay from the end of a reader transmission until the card can respond. ISO 14443 asks for 8 B.T. minimum. AT88RF256-13 is 1-2 B.T.

TR1 is the delay from the start of the subcarrier until the first phase change. ISO 14443 asks for 10 B.T. minimum. The AT88RF256-13 is 8 B.T.

Type B Frame Mode

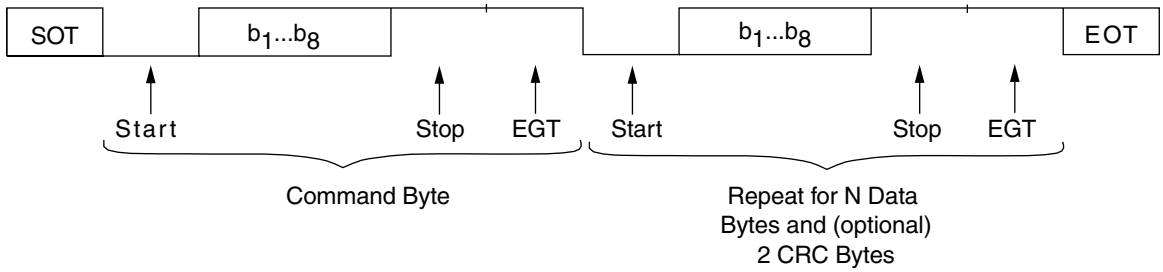
Setting the TYPE_14443 option bit to “1” puts the IC in Type B mode. The following Type B information applies only when TYPE_14443 is “1”.

All commands and data sent to the IC in Type B mode shall be received in the following format:

1. Start of Transmission (SOT) – see below for Type B SOT definition
2. One command byte (1 logic “0” start bit + 8 command bits + 1 logic “1” stop bit + EGT(1))
3. N data bytes – N*(1 logic “0” start bit + 8 data bits + 1 logic “1” stop bit + EGT(1)) $N \geq 0$
4. (Optional) 2 CRC bytes in the same format as (3) above
5. End of Transmission (EOT) – see below for Type B EOT definition

Note: EGT (Extra Guard Time) is an integer 0–6 additional logic “1”s transmitted after stop bit.

Figure 3. Type B Frame Format (Reader/Writer to Card)

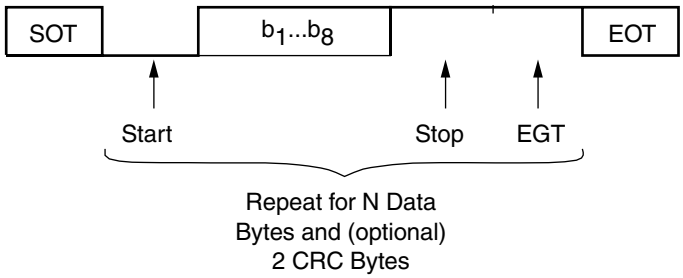


All data sent from the IC to the reader/writer will be transmitted in the following format:

1. Start of Transmission (SOT)
2. N data bytes – N (1 logic “0” start bit + 8 data bits + 1 logic “1” stop bit + 1 EGT(1) bit) $N \geq 4$
3. (Optional) Two CRC bytes in the same format as (2) above
4. End of Transmission (EOT)

Note: The EGT (Extra Guard Time) bit transmitted from the IC to the reader/writer is a logic “1”.

Figure 4. Type B Frame Format (IC to Reader/Writer)



Type B SOT/EOT

The Start of Transmission and End of Transmission sequences for Type B operation are defined below:

Start of Transmission (reader/writer to IC):

1. No carrier modulation.
2. The carrier is modulated (logic “0”) for 10 or 11 bit-times (integer multiples).
3. The carrier is not modulated (logic “1”) for 2 or 3 bit-times (integer multiples).

End of Transmission (reader/writer to IC):

1. No carrier modulation (this is the stop bit or EGT bit of the last data/command byte).
2. The carrier is modulated (logic “0”) for 10 or 11 bit-times.
3. The reader stops modulating the carrier (logic “1”).

Start of Transmission (IC to reader/writer):

1. The carrier is modulated with the subcarrier for 8 bit-times.
2. The subcarrier is phase shifted 180°.
3. The subcarrier is modulated with the carrier for 10 bit-times with no subcarrier phase change.
4. The subcarrier is phase shifted 180°.
5. The subcarrier is modulated with the carrier for 2 bit-times with no subcarrier phase changes.

Note: There will be a 180° phase change of the subcarrier between the end of the SOT and the start bit “0” if the DATA_ENCODE option is set to BPSK-NRZ-L. There will be no phase change of the subcarrier between the end of the SOT and the start bit “0” if the DATA_ENCODE option is set to BPSK-Miller. See Figure 5.

End of Transmission (IC to reader/writer). See Figure 6.

1. A logic “0” (encoded in the format selected by the DATA_ENCODE option bit) is transmitted for 10 bit-times.
2. A logic “1” (encoded in the format selected by the DATA_ENCODE option bit) is transmitted for 2 bit-times.
3. The IC stops the subcarrier modulation.

Figure 5. Type B SOT (IC to Reader)

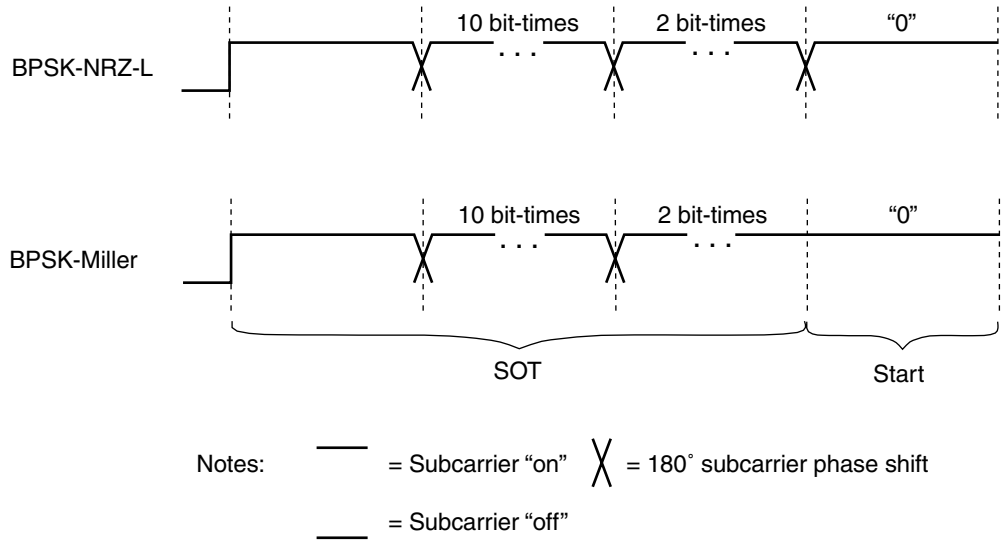
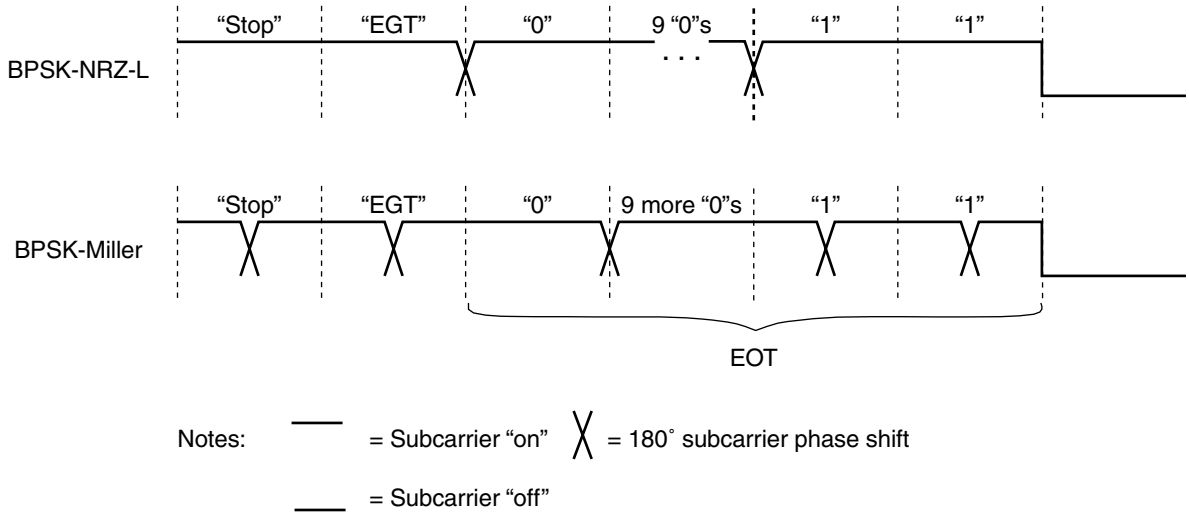


Figure 6. Type B EOT (IC to Reader)

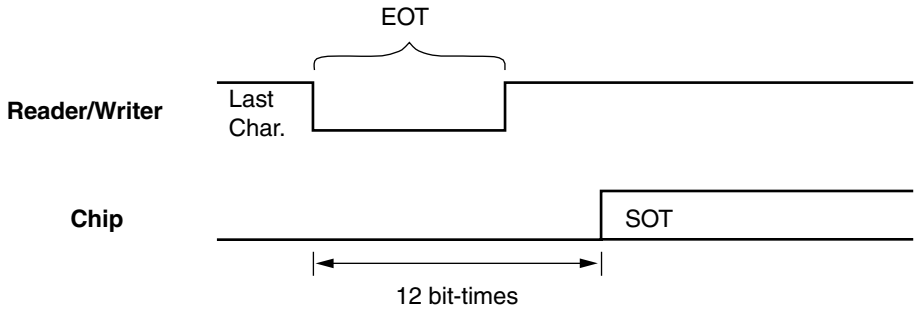


Type B Timing

The IC will begin transmitting the SOT sequence (in response to the reader/writer's Read Page or Check Password command frame) exactly 12 bit-times from the beginning of the reader/writer's EOT. The response to a successful Read Page command will be the requested page data. The response to the Check Password command will be a new framed transmission of the ID field (see page 2).

If there is an error of one sort or another with either of these commands, the IC will also start a new framed transmission of the ID field.

Figure 7. Type B Frame Timing Restrictions



Reset Voltage

The device includes a precision voltage reference to ensure that all Write commands are only performed when the internal power-supply voltage on the IC is above a required level of 2.0V. ID Reads and the Read and Disable commands will take place regardless of voltage (above a minimal POR level), which will result in correct information in most cases. Data transmitted at the lowest voltages may not be valid, and therefore some sort of error detection and/or correction (multiple reads, CRC, hamming code, etc.) must be implemented by the system.

Mechanical Specification

The IC contains two coil input pads with ESD protection, at levels greater than 2 kV, along one end of the IC. These two pads are suitable for wire bonding or solder bumping. All remaining test pads will use a different structure and size, for which production bonding or bumping is not permitted. ESD protection for these pads is 300V.

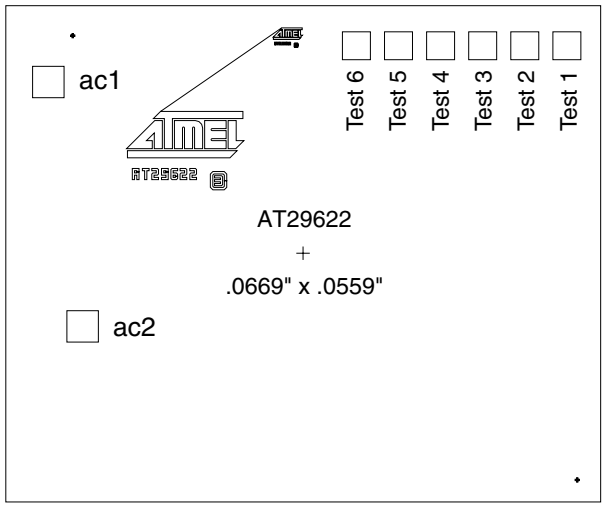
The IC includes a tuning capacitor across the coil input pins. Parasitic capacitance across these pins will be less than 10 pF and will vary with voltage, temperature, and process and read range.

A drawing of the IC is shown on the next page.

Ordering Information

Ordering Code	Package	Operation Range
AT88RF256-13-WBC-10	Bumped Wafer, 10pf	Commercial (0°C to 70°C)
AT88RF256-13-WC-10	Die on Wafer, 10 pf	
AT88RF256-13-WBC-30	Bumped Water, 30 pf	
AT88RF256-13-WC-30	Die on Wafer, 30 pf	

Figure 8. AT88RF256-13 Die



Overall Die Size:	1.611 mm x 1.331 mm			
(Center to Center)	1.700 mm x 1.420 mm		66.93 mils x 55.91 mils	
Pad Size:	80 µm		3.1 mils	
Pad Location				
ac2	X=	–630.40 µm	X=	–24.819 mils
	Y=	–209.96 µm	Y=	–8.266 mils
ac1	X=	–728.48 µm	X=	–28.680 mils
	Y=	491.24 µm	Y=	19.340 mils
Test 1	X=	740.45 µm	X=	29.152 mils
	Y=	595.30 µm	Y=	23.437 mils
Test 2	X=	640.45 µm	X=	25.215 mils
	Y=	595.30 µm	Y=	23.437 mils
Test 3	X=	540.45 µm	X=	21.278 mils
	Y=	595.30 µm	Y=	23.437 mils
Test 4	X=	397.41 µm	X=	15.646 mils
	Y=	595.30 µm	Y=	23.437 mils
Test 5	X=	275.01 µm	X=	10.827 mils
	Y=	595.30 µm	Y=	23.437 mils
Test 6	X=	152.61 µm	X=	6.008 mils
	Y=	595.30 µm	Y=	23.437 mils

Memory Map

The EEPROM is composed of 10 pages of 32 bits each for a total of 320 bits. Pages 0–7 are the user pages, which include ID information and other user-defined bytes. Page 8 is the configuration page, which includes the lock and option bits. Page 9 is the password page.

Table 2. Memory Map

	Byte 0	Byte 1	Byte 2	Byte 3
Page 0	First ID Byte	Second ID Byte	Third ID Byte	Fourth ID Byte
Page 1	Fifth ID Byte/User Data	Sixth ID Byte/User Data	Seventh ID Byte/User Data	Eighth ID Byte/User Data
Page 2	ID/User Data	ID/User Data	ID/User Data	ID/User Data
Page 3	ID/User Data	ID/User Data	ID/User Data	ID/User Data
Page 4	ID/User Data	ID/User Data	ID/User Data	User Data
Page 5	User Data	User Data	User Data	User Data
Page 6	User Data	User Data	User Data	User Data
Page 7	User Data	User Data	User Data	User Data
Page 8	LOCK0…LOCK7	OPTIONS	OPTIONS	Reserved
Page 9	First Byte Password	Second Byte Password	Third Byte Password	Fourth Byte Password

Option Page

Bits are listed below in the order in which they must be sent to the IC when the Write Lock Byte or Write Config Bits command is sent to the IC.

When reading this page, all 32 bits are read in this order. This page cannot be written with a single 4-byte frame; the Write Lock Byte command is used for the first byte only, and the Write Config Bits command is used for the last 3 bytes.

Changes to the options page do not take effect until the IC is reset by removing power or by sending an invalid command to the IC.

The Default column reflects the default value that the options have upon shipment from the Atmel factory.

Table 3. Lock Byte

Name	Number of Bits	Default Value	Description
LOCK[0:7]	8	0	If “1”, locks the corresponding user page against further writes. 10000000 Locks page 0 01000000 Locks page 1 ...and so on...

Table 4. Configuration Bits

Name	Number of Bits	Default Value	Description
PU_LEN[0:3]	4	0000	Number of ID bytes after first four. Total ID size range: 4–19 bytes. 0000 4 bytes ... 1000 5 bytes 0111 18 bytes 0100 6 bytes 1111 19 bytes
TEST	1	–	Ignored by IC.
RANDOM	1	0	Frames (ID + 8 bit-time listening window) between ID transmissions: 0 Continuous frames 1 Random null frames, mean number = 8
PW_ON	1	0	Password enable; if “1”, password is page 9 of EEPROM
TYPE_14443	1	1	If “1”, use ISO/IEC 14443-2 (Type B) for those areas not controlled by the options listed below. “0” is reserved for future use.
DATA_RATE[0:1]	2	00	Transmit and receive rate. If TYPE_14443 is “1” (Type B), then this field is ignored and the data rate is fixed at 106 Kbits/sec.
DATA_ENCODE	1	0	Always “0”.
PW_LOCK	1	0	If “1”, locks the password page against further writes.
CONFIG_LOCK	1	0	If “1”, locks the configuration page (but not LOCK[7:0]) against further writes.
CRC_ON	1	1	If “1”, enables 2-byte CRC at the end of each frame transmission.
MSB	2	N/A	Don’t Care (ignored by IC).
RESERVED	8	–	These bits are for internal use. They return unpredictable values on a read and cannot be written to.

Configuration Page Example

To write the configuration page, send the write configuration command and dummy AA byte, followed by the configuration bits and the 2-byte (if the optional CRC is enabled). In the following example, the configuration is being written to: PU_LEN = 8 ID bytes (0010), RANDOM = Continuous Frames (0), PW_ON = enabled (1), TYPE_14443 = Type B (1), CRC_ON = enabled (1). All other configuration bits are set to their default value of 0. The CRC_B bytes shown are correct for this data.

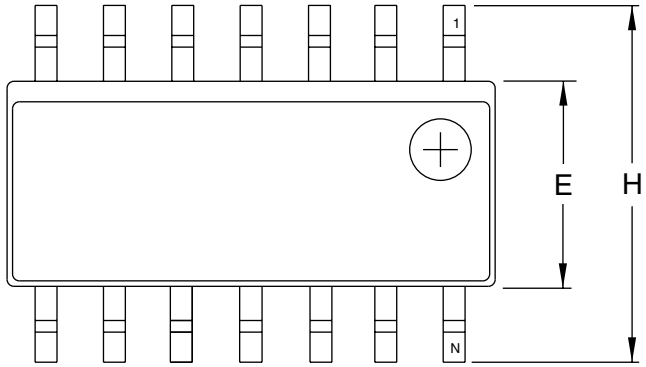
After sucessfully writing the configuration page, the IC will continuously transmit the contents of page 8. The changes in configuration will not take effect until the IC is reset by powering it down or by sending an invalid command to the IC.

Table 5. Configuration Page Example

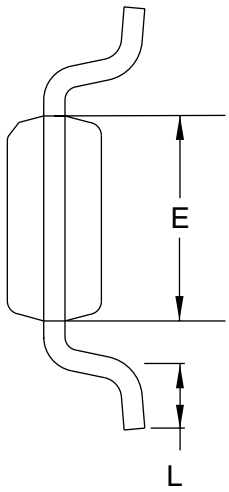
Write Config Command	Dummy Byte AA	Configuration			CRC_B Byte 1	CRC_B Byte 2
		Byte 1	Byte 2	Reserved		
00010011	01010101	00100011	00000100	00000000	11011110	01010111
L S B						M S B

Package Drawing

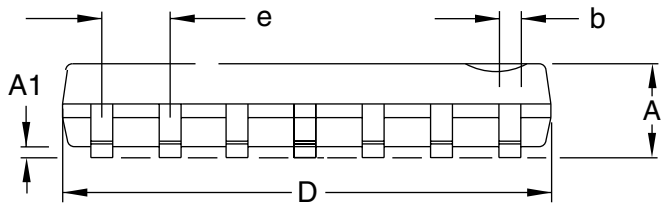
14S1 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.0532	–	0.0688	
A1	0.0040	–	0.0098	
b	0.0130	–	0.0200	5
C	0.0075	–	0.0098	
D	0.3367	–	0.3444	2
E	0.1497	–	0.1574	3
H	0.2284	–	0.2440	
L	0.0160	–	0.0500	4
e	0.050 BSC			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-012, Variation AB for additional information.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusion and gate burrs shall not exceed 0.15 mm (0.006") per side.
3. Dimension E does not include inter-lead Flash or protrusion. Inter-lead flash and protrusions shall not exceed 0.25 mm (0.010") per side.
4. L is the length of the terminal for soldering to a substrate.
5. The lead width B, as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.

2/5/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**14S1**, 14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	14S1	A

Pin Connections

L1 is connected to pin 10.

L2 is connected to pin 11.

All the remaining pins should float.

Engineering samples come with a 30 pF tuning capacitor. If no additional capacitance is added (including parasitics), a 4.54 µH nominal antenna inductance should be used. The antenna should be tuned to 13.56 MHz for maximum performance.

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