DS04-21208-3E

FUJITSU

DATA SHEET

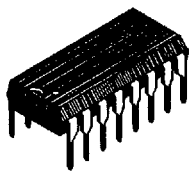
ASSP
CMOS PLL FREQUENCY SYNTHESIZER
MB87086A

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

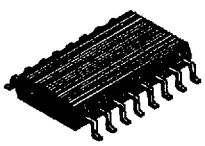
The Fujitsu MB87086A, fabricated in advanced CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer. The MB87086A contains an inverter for oscillator, programmable reference divider (binary 16-bit programmable reference counter), programmable divider (binary 10-bit programmable counter), phase detector, charge pump.

The MB87086A can make up PLL synthesizer up to 95MHz operation.

- Single Power Supply Voltage: V_{DD} = 4.5V to 5.5V
- Wide Temperature Range: T_A = -30 to 60°C
- On-chip Inverter for oscillator
- Divide factor of programmable divider and programmable divider are set by serial data input. (The last data bit is a control bit.)
- 3-type of phase detector outputs
  On-chip charge pump output for active LPF
  On-chip charge pump output for passive LPF
  Output for external charge pump
- 16-pin Standard Dual-in-line Package (Suffix: -P)
  16-pin Standard Flat Package (Suffix: -PF)
- 95MHz input capability @5V (fin input)
- fin, Clock, Data input circuits involve schmitt circuit
- The divide factor is selected according to the following equation:
  $f_{VCO} = N \times (f_{OSC} \div R)$
  f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
  N : Preset divide factor of programmable divider (5 to 1023)
  f_{OSC} : Output frequency of the external oscillator
  R : Preset divide factor of binary programmable reference divider (5 to 65535)

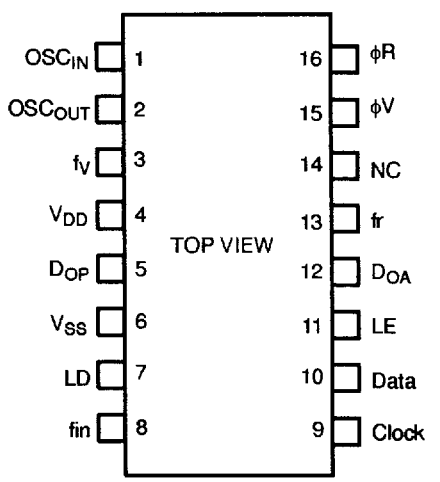


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



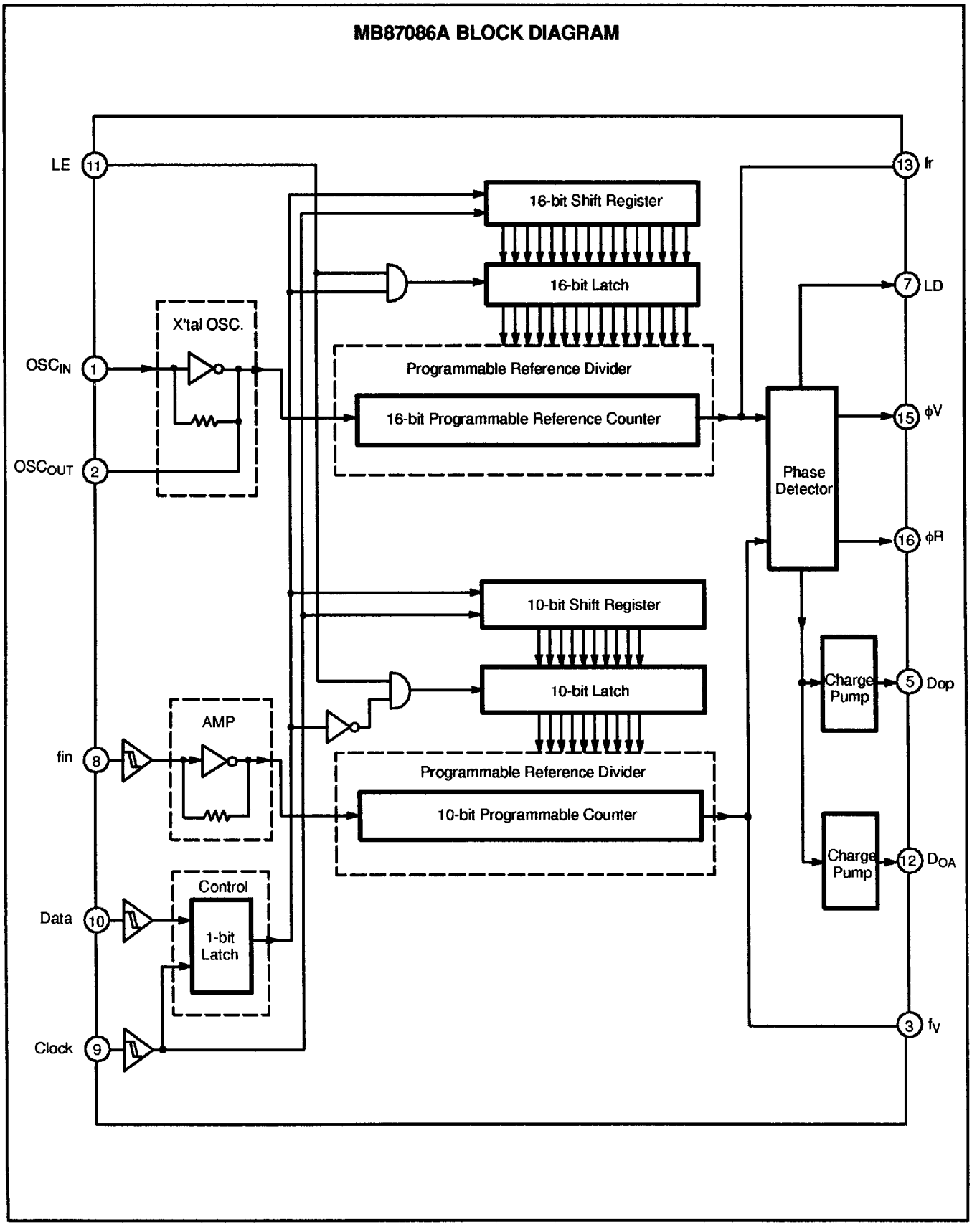
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} -0.3 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3 to V_{DD} +0.3	V
Output Voltage	V_{OUT}	V_{SS} -0.3 to V_{DD} +0.3	V
Output Current	I_{OUT}	±10	mA
Operating Ambient Temperature	T_A	-30 to +80	°C
Storage Temperature	T_{STG}	-40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB87086A BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be connected to open when an external oscillator is used.
3	f_V	O	Monitor pin for the phase detector input. This pin is tied to the programmable divider output.
4	V_{DD}	-	Power supply voltage input.
5	D_{OP}	O	Output pin for low pass filter (Passive type). The mode of D_{OP} is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: fr > f_V: Drive mode (D_{OP} - High level) fr = f_V: High-impedance fr < f_V: Sink mode (D_{OP} = Low level)
6	V_{SS}	-	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are coherent, and when the loop is locked. Otherwise it outputs low pulse signal.
8	fin	I	Frequency input to programmable divider from VCO or prescaler output. (This input has an internal feed back resistor.)
9	Clock	I	Clock signal input for shift registers. Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	I	Serial data input for shift registers. The last bit of the data is the control bit. The control data determines which latch is activated.
11	LE	I	Load enable input. When this pin is high level, the data stored in the shift registers is transferred to 16-bit latch, or 10-bit latch depending on the control bit setting.
12	D_{OA}	O	Output pin for low pass filter (Active type). The mode of D_{OA} is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: fr > f_V: Drive mode (D_{OA} - Low level) fr = f_V: High-impedance fr < f_V: Sink mode (D_{OA} = High level)
13	fr	O	Monitor pin for the phase detector input. This pin is tied to the programmable reference divider output.
14	NC	-	No connection.
15 16	ϕV ϕR	O O	Output pins for low pass filter (differential filter type). Outputs for external charge pump are changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below. ϕV / ϕR fr > f_V: High level / Low level fr = f_V: High level / High level fr < f_V: Low level / High level

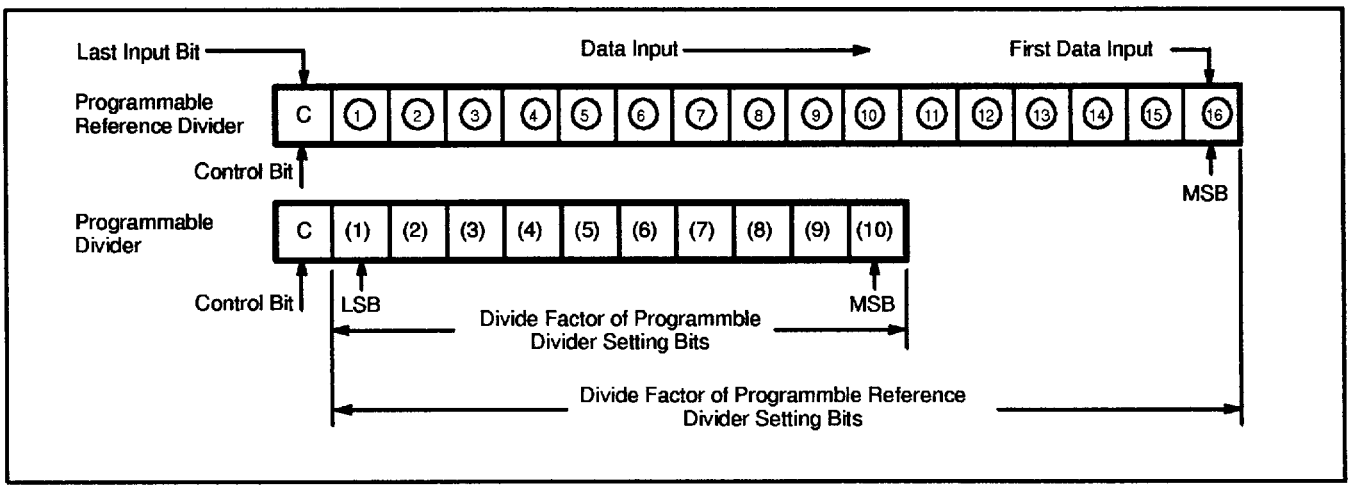
FUNCTIONAL DESCRIPTIONS

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

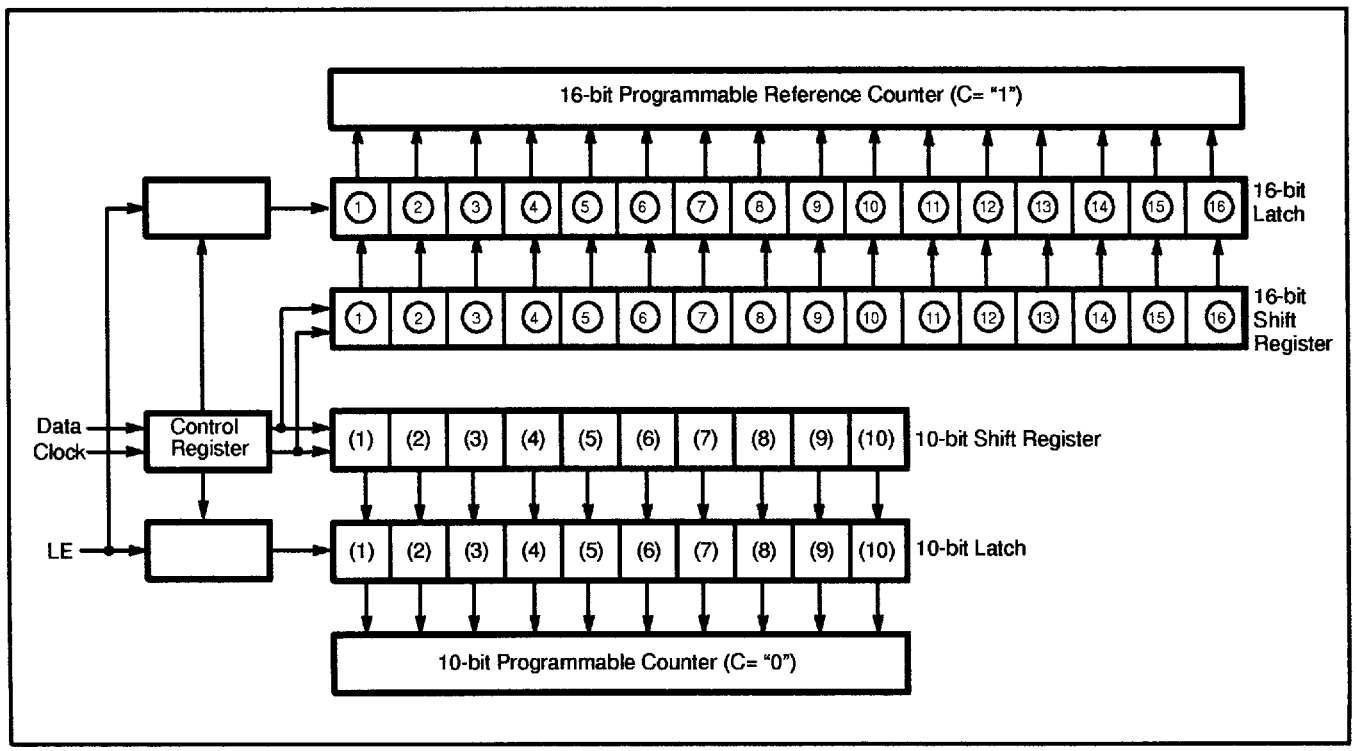
Serial data of binary code is input to Data pin. Each rising edge of clock makes one bit of the data shift into the shift registers and control register. Input data consists of 16-bit or 10-bit data and 1-bit of control bit data. The 16-bit data is used for setting the divide factor of programmable reference divider. The 10-bit data is used for setting the divide factor of programmable divider.

The last bit of the data stored in control register is a control bit. Control data determines which latch is activates. When this bit is at high level, 16-bit latch is selected. when this is at low level, 10-bit latch is selected.

The data format is shown below.



When LE is high level and control bit is high level, the data stored in 16-bit shift register is transferred to 16-bit latch. When LE is high level and control bit is at low level, the data stored in 10-bit shift register is transferred to 10-bit latch.



BINARY 10-BIT PROGRAMMABLE DIVIDER DATA INPUT

(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	Divide Factor
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

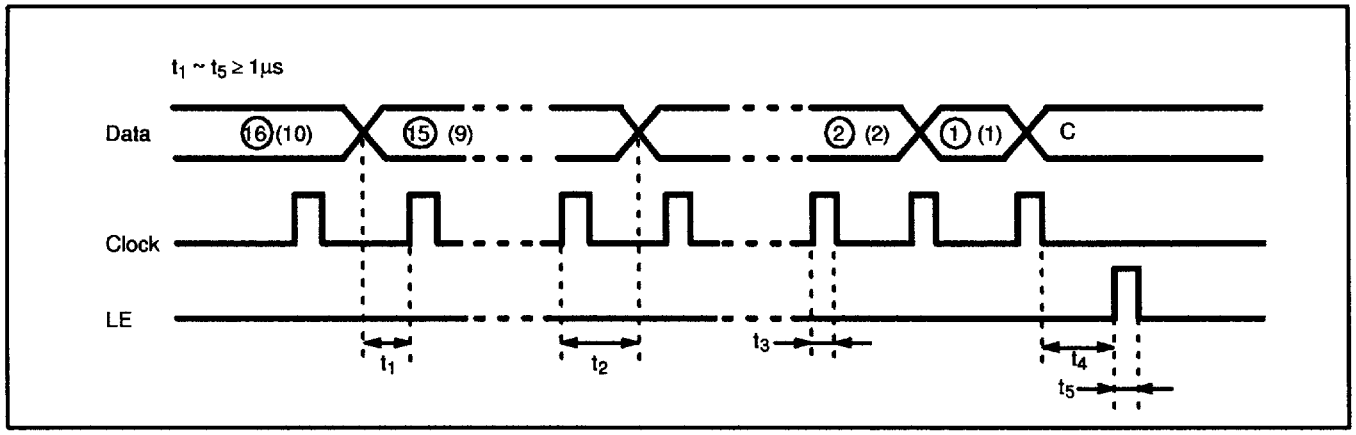
Note: Divide factor less than 5 is prohibited.
Divide factor N: 5 to 1023

BINARY 16-BIT PROGRAMMABLE REFERENCE DIVIDER DATA INPUT

⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	⑦	⑥	⑤	④	③	②	①	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	65535

Note: Divide factor less than 5 is prohibited.
Divide factor R: 5 to 65535

SERIAL DATA INPUT TIMING



Notes: ○ Data input for programmable reference divider.

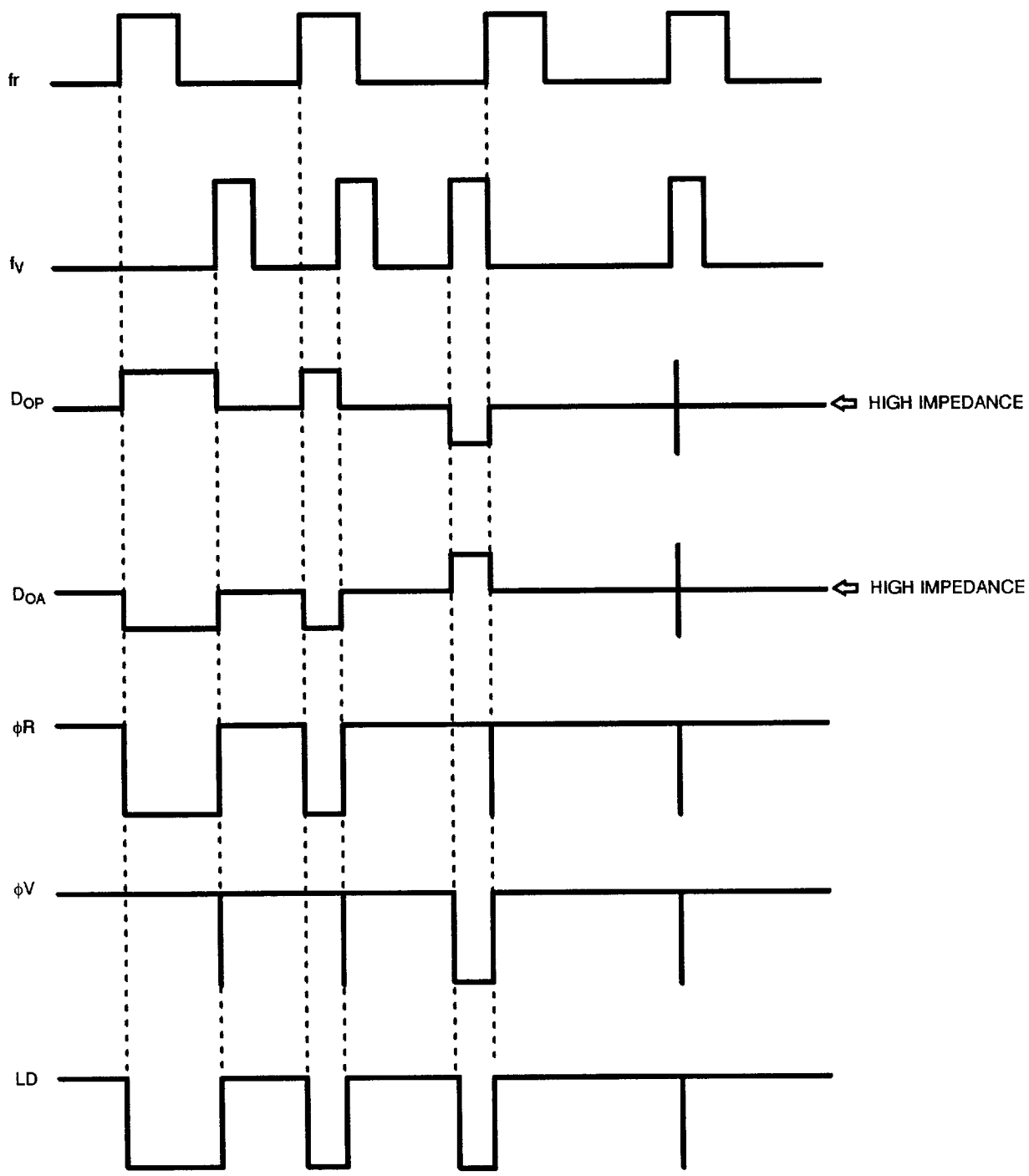
( ) Data input for programmable divider.

Data Serial data input is used for setting divide factor of programmable reference divider or progranmable divider.
Data is input from MSB and last bit data is control bit.
Control bit is set high level when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock Clock input for 10-bit shift register, 16-bit shift register and control register. Data is input into internal shift registers by rising edge of the clock.

LE Load enable input:
When LE is high level, the data stored in shift registers is transferred to 16-bit latch, or 10-bit latch depending on the control bit setting.

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	-30		+60	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 5V, T_A = -30 to 60°C)

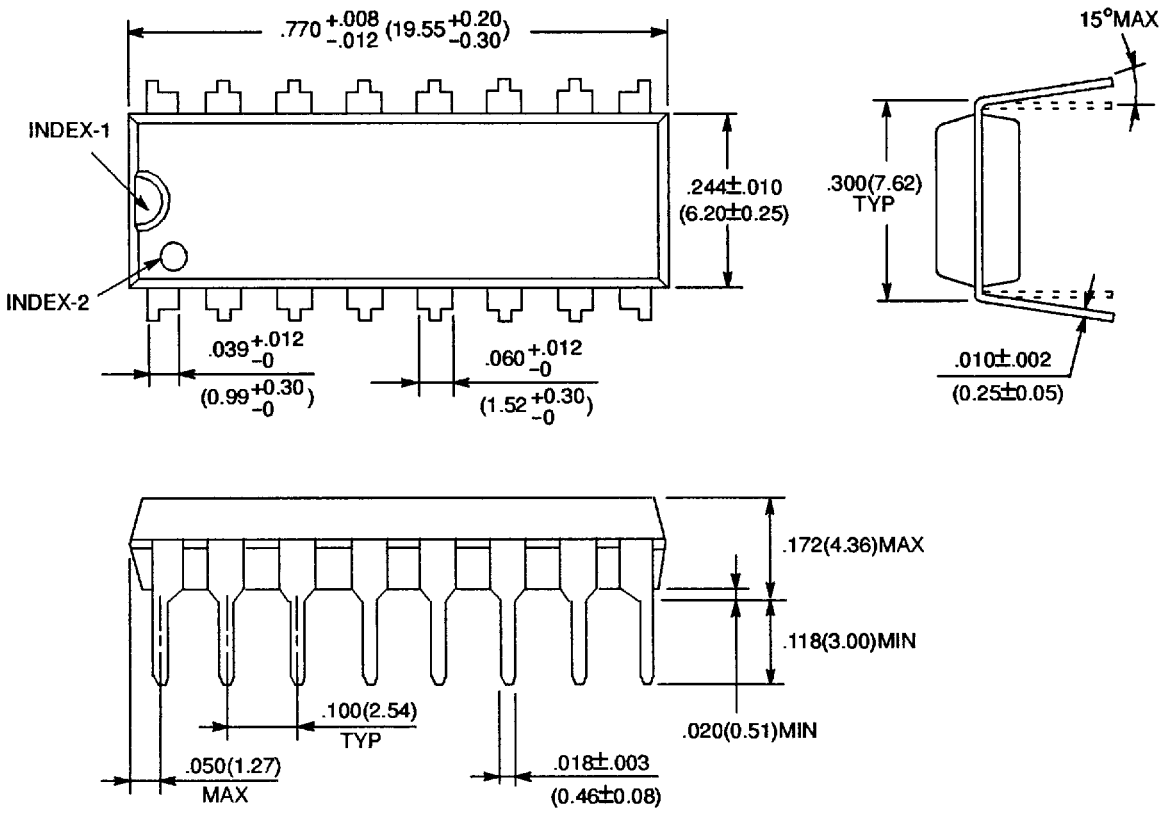
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, Sine wave	1.0			V_{P-P}
	OSC_{IN}	Vsin		1.0			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IH} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IL} = V_{SS}$		-1.0		
Input Current	fin	Ifin	$V_{IN} = V_{SS}$ to V_{DD}		±50		µA
	OSC_{IN}	Iosc	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	-1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
Power Dissipation*1		I_{DD}			8.0		mA
Maximum Operating*2 Frequency	REF Section	fmaxd		40	60		MHz
	PD Section	fmaxp		95	130		MHz

Notes: *1: fin 100MHz, 22MHz cystal is connected between OSC_{IN} and OSC_{OUT} pins.
Inputs are grounded except fin and OSC_{IN}. Outputs are open.

*2 REF Section: Maximum operating frequency of programmable reference divider.
PD Section: Maximum operating frequency or programmable divider.

PACKAGE DIMENSIONS

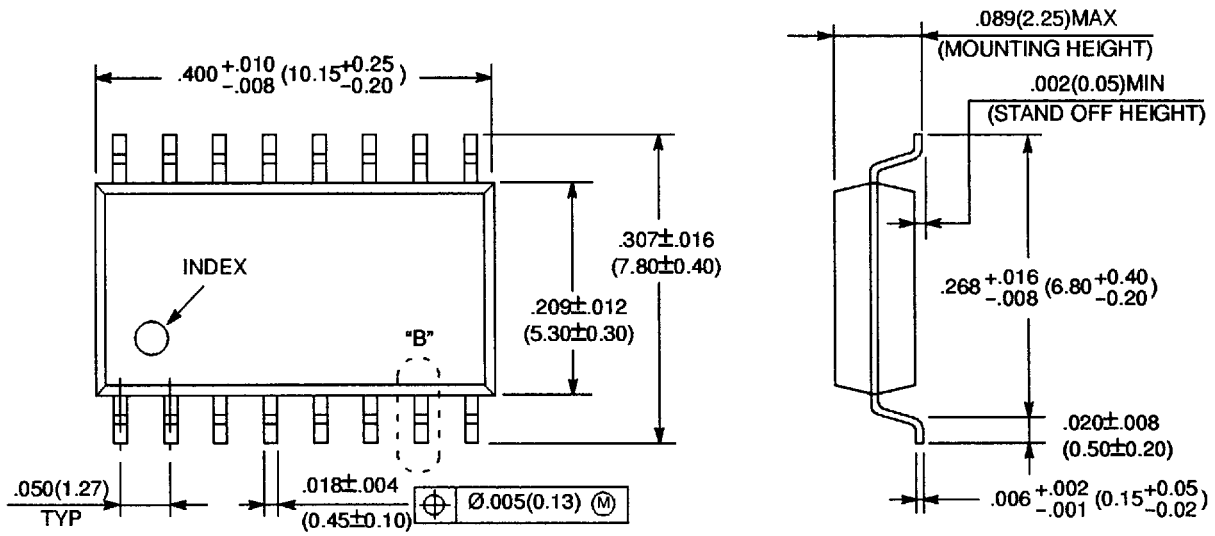
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)

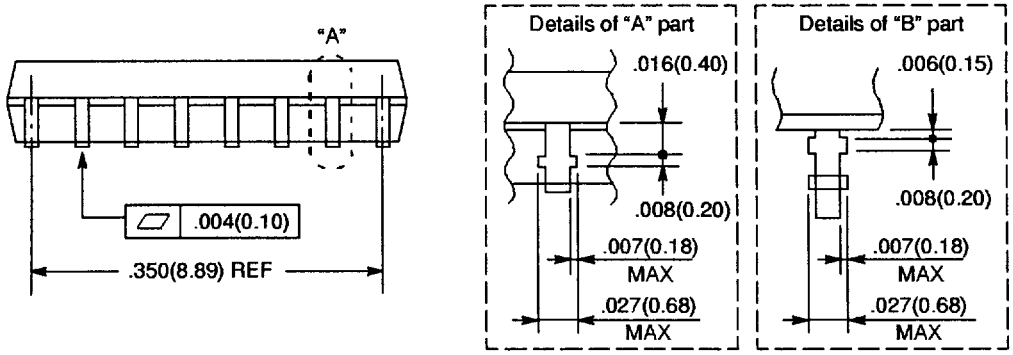


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)





Dimensions in
inches (millimeters)