SINO WEALTH

SH66P22A

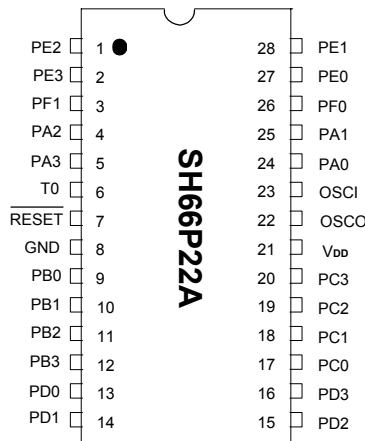## *OTP 4-bit Microcontroller*

Features

- SH6610C-based single-chip 4-bit micro-controller
- OTPROM: 4K X 16 bits
- RAM: 160 X 4 bits (data memory)
- Operation voltage: 2.4V - 6.0V (typical 3.0V or 5.0V)
- 22 CMOS bi-directional I/O pins
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-load timer/counter
- Warm-up timer for power on reset
- Powerful interrupt sources:
  - Internal interrupt (Timer0)
  - External interrupts: PortB & PortC (falling edge)

- Oscillator (OTP option)
  - X`tal oscillator: 32.768KHz - 4MHz
  - Ceramic resonator: 400K - 4MHz
  - RC oscillator：   400K - 4MHz
  - External clock: 30K - 4MHz
- Instruction cycle time:
  - 4/32.768KHz(122us) for 32.768KHz OSC clock
  - 4/4MHz (1us) for 4MHz OSC clock
- Two low power operation modes: HALT and STOP
- Built-in watch dog timer (OTP option)
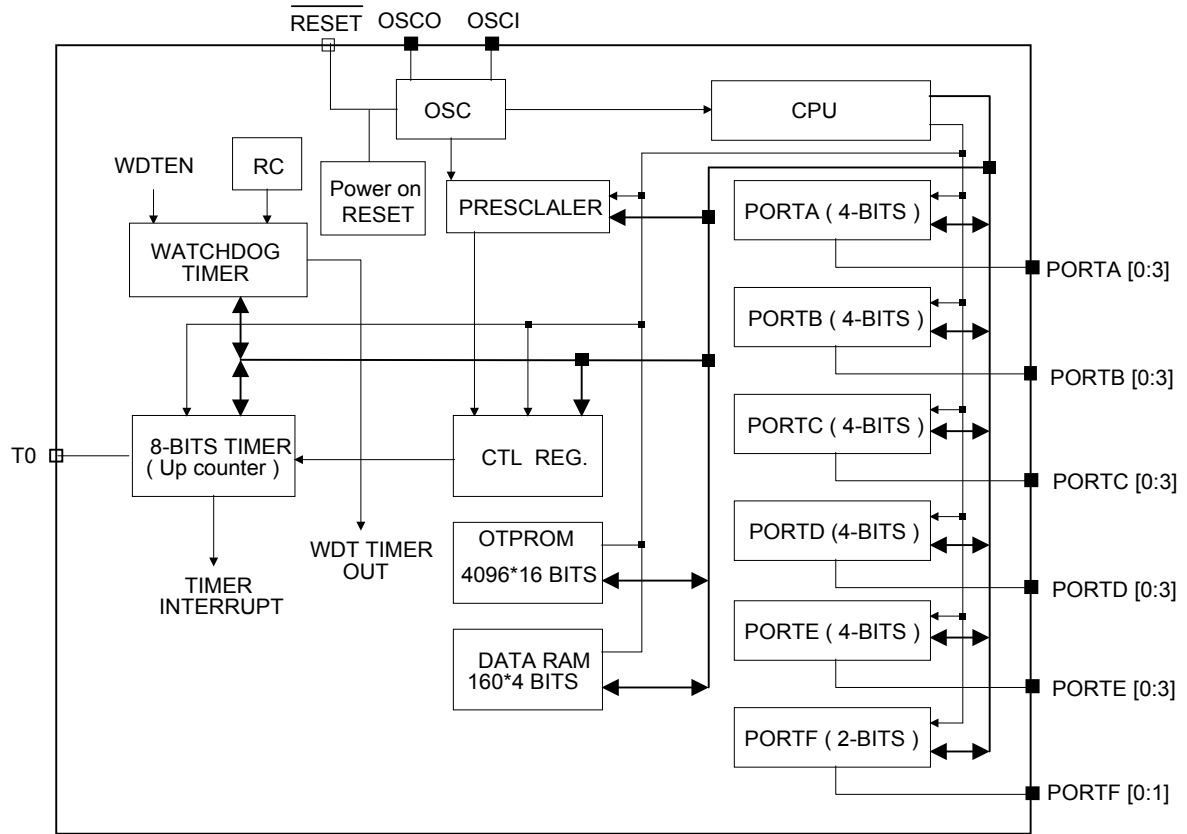- Built-in power on reset

General Description

SH66P22A is a 4-bit micro controller. This chip integrates the SH6610C 4-bit CPU core with SRAM, 4K OTPROM, Timer and I/O Ports.

Pin Configuration

PE2	1	28	PE1
PE3	2	27	PE0
PF1	3	26	PF0
PA2	4	25	PA1
PA3	5	24	PA0
T0	6	23	OSCI
RESET	7	22	OSCO
GND	8	21	V_{DD}
PB0	9	20	PC3
PB1	10	19	PC2
PB2	11	18	PC1
PB3	12	17	PC0
PD0	13	16	PD3
PD1	14	15	PD2

SH66P22A

Block Diagram

Pin Description

Pin No.	Designation	I/O	Descriptions
27, 28, 1, 2	PE.0 - PE.3	I/O	Bit programmable I/O
26, 3	PF.0 - PF.1	I/O	Bit programmable I/O
24, 25, 4, 5	PA.0 - PA.3	I/O	Bit programmable I/O
6	T0	I	Timer Clock/Counter input pin. (Schmitt trigger input)
7	$\overline{RESET}$	I	Reset input (active low, Schmitt trigger input)
8	GND	P	Ground pin
9 - 12	PB.0 - PB.3	I/O	Bit programmable I/O. Vector Interrupt (active falling edge)
13- 16	PD.0 - PD.3	I/O	Bit programmable I/O
17 - 20	PC.0 - PC.3	I/O	Bit programmable I/O. Vector Interrupt (active falling edge)
21	V**DD**	P	Power supply pin
22	OSCO	O	OSC output pin. Output a frequency of Fosc/4 for RC mode
23	OSCI	I	OSC input pin, connected to a crystal, ceramic or external resistor

Function Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and the Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 4K program ROM. It consists of 12-bits: the Page Register (PC11), and the Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BAC),

(2) When executing a subroutine call instruction (CALL),

(3) When an interrupt occurs,

(4) When the chip is in the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decision (BA0, BA1, BA2, BA3, BAZ, BAC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and retrieved back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

The Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data transfer between the accumulator and system register or data memory can be performed.

1.4. Stack

A group of registers are used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized into 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of the Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). The stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceed 4, and the bottom of the stack will be shifted out.

2. OTPROM

The SH66P22A can address up to 4096 X 16 bit words of program area from $000 to $FFF.
Service routine as starting vector address.

Address	Instruction	Remarks
$000H	JMP Instruction	Jump to RESET service routine
$001H	NOP	Reserved
$002H	JMP Instruction	Jump to TIMER0 service routine
$003H	NOP	Reserved
$004H	JMP Instruction	Jump to PBC service routine

3. RAM

The built-in RAM consists of general-purpose data memory and the system register. Direct addressing in one instruction can access both data memory and the system register.

The following is the memory allocation map:

$000 - $01F: System register and I/O.
$020 - $0BF: Data memory (160 X 4 bits, divided into 2 banks. $020 - $07F: bank0, $080 - $0BF: bank1).

The Configuration of the System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06	-	-	-	-	-	Reserved
$07	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 - 0): 1010: LPD Enabled (Default); 0101: LPD Disabled
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	-	-	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12		DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13 - $15						Reserved
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA as an output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB as an output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC as an output port
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	W	Set PORTD as an output port
$1A	PE3OUT	PE2OUT	PE1OUT	PE0OUT	W	Set PORTE as an output port
$1B	-	-	PF1OUT	PF0OUT	W	Set PORTF as an output port
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge; Bit1: T0 signal source
$1D	-	-	-	-	-	Reserved
$1E	WDT	-	-	-	W	Bit3: Watchdog timer reset (write 1 to reset WDT)
$1F	-	-	-	-	-	Reserved

* System Register $00 - $12 (except $07H) refer to "SH6610C User manual".

Low Power Detection (LPD)

The LPD function is used to monitor the supply voltage and applies an internal reset in the micro-controller at the time of battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated using software control.

- High reliability is not required
- Power supply voltage V_{DD} = 2.4 to 6.0 V
- Operating ambient temperature T_A = -10℃ to + 60℃

Functions of the LPD Circuit

The LPD circuit has the following functions:

- It generates an internal reset signal when $V_{DD} \leq V_{LPD}$
- It cancels the internal reset signal when $V_{DD} > V_{LPD}$

Here, V_{DD}: power supply voltage, V_{LPD}: LPD detect voltage, about 1.6 - 1.7V and lower than V_{DD-MIN} (2.4V)

LPD Control Register

The LPD circuit is controlled by the software enable flag

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$07	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 - 0): 1010: LPD Enable (Default); 0101: LPD Disable

LPD3、	LPD2、	LPD1、	LPD0:	LPD Enable/Disable flag
1	0	1	0	Enable LPD circuit (Power-on initial)
0	1	0	1	Disable LPD circuit

System Register $16 - $1B

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA as an output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB as an output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC as an output port
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	W	Set PORTD as an output port
$1A	PE3OUT	PE2OUT	PE1OUT	PE0OUT	W	Set PORTE as an output port
$1B	-	-	PF1OUT	PF0OUT	W	Set PORTF as an output port

Equivalent Circuit for a Single I/O Pin

PAXOUT, PBXOUT, PCXOUT, PDXOUT, PEXOUT (X = 0, 1, 2, 3), PFXOUT (X = 0, 1)

 1: Use as an output buffer

 0: Use as an input buffer (Power on initial)

T0 & WDT

System Register $1C

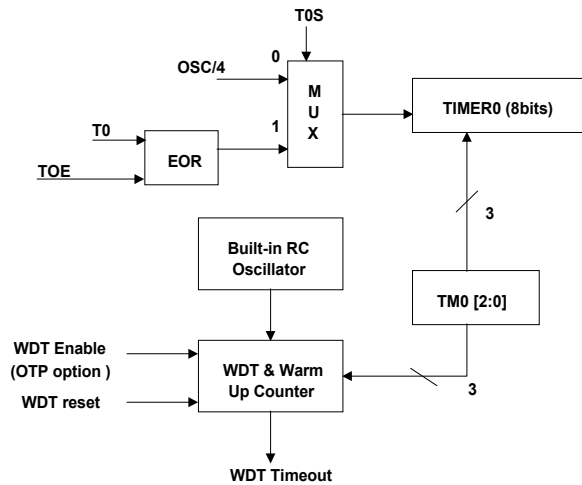| Address	BIT3	BIT2	BIT1	BIT0	R/W	Remark
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge Bit1: T0 signal source

T0E: T0 signal edge

0: Increment on low-to-high transition T0 pin (Power on initial)
1: Increment on high-to-low transition T0 pin

T0S: T0 signal source.

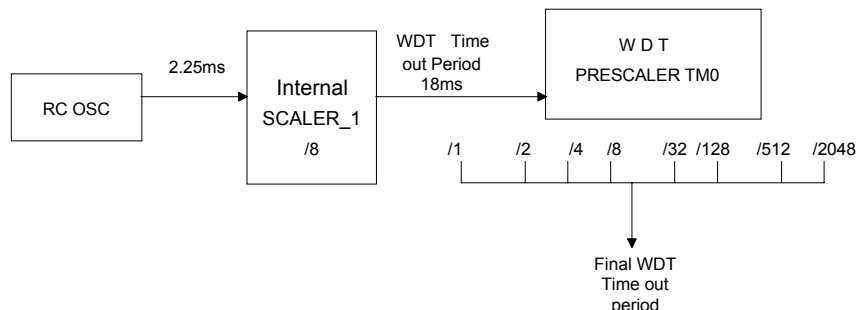0: OSC 1/4 (Power on initial).
1: Transition on T0 pin.

System Register $1E

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$1E	WDT	-	-	-	W	Bit3: Watchdog timer reset. (write 1 to reset WDT)

The input clock of the watchdog timer is generated by a built-in RC oscillator so that the WDT will always run even in the STOP mode. SH66P22A generates a RESET condition when the watchdog times-out. The watchdog can be enabled or disabled permanently by using the OTP option. To prevent it timing out and generating a device RESET condition, you should write this bit as "1" before timing-out. The WDT has a time-out period of more than 7ms.If longer time-out periods are desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the WDT under software controll by writing to the TM0 register.

Prescaler divide ratio:

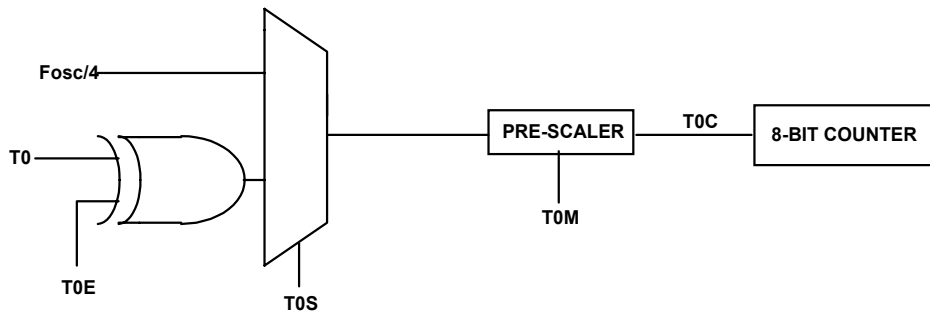| TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Timer-out Period
1	1	1	1:1	7ms
1	1	0	1:2	14ms
1	0	1	1:4	28ms
1	0	0	1:8	56ms
0	1	1	1:32	224ms
0	1	0	1:128	896ms
0	0	1	1:512	3,584ms
0	0	0	1:2048 (Power on initial)	14,336ms

4. Timer0

SH66P22A has one 8-bit timer. The time/counter has the following features:

. 8-bit timer/counter
. Readable and writeable
. Automatic reloadable counter
. 8-prescaler scale is available
. Internal and external clock select
. Interrupt on overflow from $FF to $00
. Edge select for external event

Following is a simplified timer block diagram:

4.1. Configuration and Operation

Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter. Load register programming: Write the low-order digit first and then the high-order digit. The timer counter is loaded with the contents of the load register automatically when the high order digit is written or the counter counts overflow from $FF to $00.
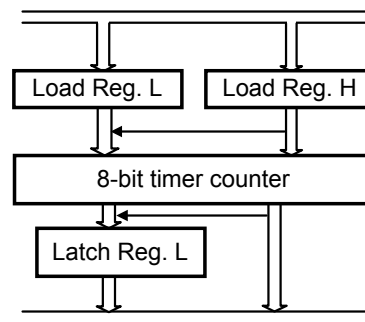
Timer Load Register: Since the register H controls the physical READ and WRITE operation, please follow these rules:

Write Operation:

First write Low nibble,
Then write High nibble to update the counter.

Read Operation:

High nibble first;
Followed by Low nibble.

4.2. Timer0 Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will proceed. This can also be used to waken the CPU from HALT mode.

4.3. Timer0 Mode Register

The timer can be programmed in several different prescaler ratios by setting the Timer Mode register (TM0). The 8-bit counter counts prescaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in table1. These mode registers select the input pulse sources into the timer.

Table 1. Timer 0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^9$	512
0	1	0	$/2^7$	128
0	1	1	$/2^5$	32
1	0	0	$/2^3$	8
1	0	1	$/2^4$	4
1	1	0	$/2^1$	2
1	1	1	$/2^0$	1

4.4. External Clock/Event T0 as Timer0 Source

When an external clock/event input is used for the TM0, it is synchronized with the CPU system clock. Therefor the external source must follow certain constraints. The output from the T0M multiplex is T0C. It is sampled by the system clock in instruction frame cycle. Therefore it is necessary for the T0C to be high (at least 2 t_{osc}) and low (at least 2 t_{osc}). When the prescaler ratio selects $/2^0$, the T0C is the same as the system clock input. Therefore the requirement is as follows

$$T0H = T0CH = T0 \text{ high time} \geq 2\ t_{osc} + \Delta T$$

$$T0L = T0CL = T0 \text{ low time} \geq 2\ t_{osc} + \Delta T$$

$$\text{Note: } \Delta T = 40ns$$

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical.

Then:

$$T0C \text{ high time} = T0C \text{ low time} = \frac{N * T0}{2}$$

Where

T0 = Timer0 input period

N = prescaler value

The requirement is, therefore:

$$\frac{N * T0}{2} \geq 2\ t_{osc} + \Delta T, \text{ or } T0 \geq \frac{4 * t_{OSC} + 2\ T}{N}$$

The limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * t_{OSC} + 2\Delta T}{N}$$

5. Port Interrupt

The PBC interrupt (PORTB & PORTC, 8bits) is falling edge active. This means that if an interrupt request (IEx is set to 1 and one port bit goes from high to low) is been touched, then the condition is the other port bits are high level. Only input port bits could cause interrupt.
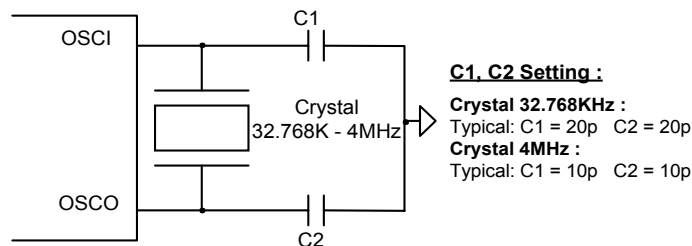
6. System Clock and Oscillator

System clock generator produces the basic clock pulses that provide the system clock to the CPU and any peripherals. Instruction cycle time
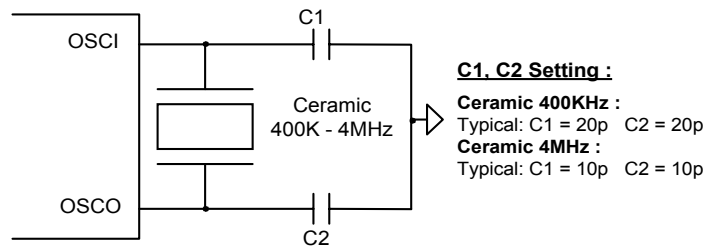
(1) 4/32.768KHz (≈122us) for 32.768KHz system clock

(2) 4/4MHz (1us) for 4MHz system clock

Oscillator

(1) Crystal oscillator: 32.768KHz - 4MHz.

OSCI
C1
Crystal
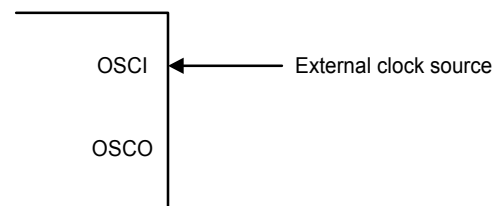32.768K - 4MHz
OSCO
C2

C1, C2 Setting :

Crystal 32.768KHz :
Typical: C1 = 20p   C2 = 20p
Crystal 4MHz :
Typical: C1 = 10p   C2 = 10p

(2) Ceramic resonator: 400KHz - 4MHz.

OSCI
C1
Ceramic
400K - 4MHz
OSCO
C2

C1, C2 Setting :

Ceramic 400KHz :
Typical: C1 = 20p   C2 = 20p
Ceramic 4MHz :
Typical: C1 = 10p   C2 = 10p

(3) RC oscillator: 400KHz - 4MHz.

V$_{DD}$
R
OSCI
OSCO → Fosc/4
C1 = 1000p

(4) External input clock: 30KHz - 4MHz.

OSCI ← External clock source
OSCO

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Initial State

Hardware	After Power on Reset
Program counter	$000
CY	Undefined
Data memory	Undefined
System register	Undefined
AC	Undefined
Pseudo index register	Undefined
DPL, DPM, DPH	Undefined
Table Branch Register	Undefined
Interrupt enable flag register	0
Interrupt request flag register	0
Timer mode register	0
Timer counter	0
Timer load register	0
WDT counter	0
WDT prescaler	0
I/O ports	Input
LPD3 - 0	1010 (Enable LPD)

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.
Arithmetic and Logical Instruction
Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] →CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, the EORIM mnemonic is EORI. However, EORI has the identical operation to EORIM. The same is true for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjustment for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjustment for sub.	CY

Transfer Instructions

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instructions

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not including p)	
RTNW H, L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Including p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank. Every $7F as one RAM bank.
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . -0.3V to + 7.0V

Input Voltage . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . -10℃ to + 60℃

Storage Temperature . . . .-55℃ to + 125℃

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5		6	V	
Operating Current	I_{OP}		1	2	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}			0.5	mA	All output pins unloaded
Stand by Current (STOP)	I_{SB2}		1	2	μA	All output pins unloaded, LPD off (If LPD on, I_{SB2X} = I_{SB2} + 3μA) WDT off (If WDT on, I_{SB2X} = I_{SB2} + 15μA)
Input Low Voltage	V_{IL1}	GND		0.2 X V_{DD}	V	I/O ports, pins tri-state
Input Low Voltage	V_{IL2}	GND		0.15 X V_{DD}	V	$\overline{RESET}$, T0
Input Low Voltage	V_{IL3}	GND		0.15 X V_{DD}	V	OSCI (Driven by external clock)
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD}	V	I/O ports, pins tri-state
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD}	V	$\overline{RESET}$, T0
Input High Voltage	V_{IH3}	0.85 X V_{DD}		V_{DD}	V	OSCI (Driven by external Clock)
Input Leakage Current	I_{IL1}	-1		1	μA	I/O ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5			μA	$V_{\overline{RESET}}$ = GND + 0.25V
Input Leakage Current	I_{IL3}		1	5	μA	$V_{\overline{RESET}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < V_{t0} < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Output High Voltage	V_{OH}	V_{DD} - 0.7			V	I/O ports, I_{OH} = -10mA, OSCO$_{RC}$, I_{OH} = -0.7mA
Output Low Voltage	V_{OL}			GND + 0.6	V	I/O ports, I_{OL} = 20mA, OSCO$_{RC}$, I_{OL} = 1.6mA

AC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	T_{OSC1}			1	s	X'tal osc = 32.768KHz
Oscillator Start Time	T_{OSC2}			20	ms	Ceramic osc = 400KHz
Oscillator Start Time	T_{OSC3}			2	ms	RC Osc = 400KHz
Oscillator Start Time	T_{OSC4}			2	ms	RC Osc = 4MHz
WDT Period	T_{WDT}	7	18		ms	V_{DD} = 5.0V
Frequency Stability (crystal)	$\Delta F/F$			1	ppm	Crystal Oscillator: [F(5.0)-F(4.5)]/F(5.0)
Frequency Variation (crystal)	$\Delta F/F$			10	ppm	Crystal Oscillator: C1 = C2 = 5 - 30p
Frequency Stability (ceramic)	$\Delta F/F$			0.1	%	Ceramic Resonator Osc: [F(5.0)-F(4.5)]/F(5.0)
Frequency Variation (RC)	$\Delta F/F$			$\pm$ 20	%	Include supply voltage and chip to chip variation
Frequency Stability (RC)	$\Delta F/F$			5	%	RC Oscillator: [F(5.0)-F(4.5)]/F(5.0)

User Notice:

Max. Current into V_{DD} = 50mA;
Max. Current out of V_{SS} = 150mA
Max. Output current sunk by any I/O port = 25mA;

Max. Output current sourced by any I/O port = 20mA
Max. Output current sunk by all ports (A, B, C, D, E, F) = 50mA;
Max. Output current sourced by all ports (A, B, C, D, E, F) = 40mA

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4		4.5	V	
Operating Current	I_{OP}		0.7	1.3	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}			0.2	mA	All output pins unloaded
Stand by Current (STOP)	I_{SB2}		1	2	μA	All output pins unloaded, LPD off (If LPD on, I_{SB2X} = I_{SB2} + 3μA) WDT off (If WDT on, I_{SB2X} = I_{SB2} + 5μA)
Input Low Voltage	V_{IL1}	GND		0.2 X V_{DD}	V	I/O ports, pins tri-state
Input Low Voltage	V_{IL2}	GND		0.15 X V_{DD}	V	$\overline{RESET}$, T0
Input Low Voltage	V_{IL3}	GND		0.15 X V_{DD}	V	OSCI (Driven by external clock)
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD}	V	I/O ports, pins tri-state
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD}	V	$\overline{RESET}$, T0
Input High Voltage	V_{IH3}	0.85 X V_{DD}		V_{DD}	V	OSCI (Driven by external Clock)
Input Leakage Current	I_{IL1}	-1		1	μA	I/O ports, GND < Vi/o < V_{DD}
Input Leakage Current	I_{IL2}	-5			μA	$V_{\overline{RESET}}$ = GND + 0.25V
Input Leakage Current	I_{IL3}		1	5	μA	$V_{\overline{RESET}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < Vt0 < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Output High Voltage	V_{OH}	V_{DD} - 0.7			V	I/O ports, I_{OH} = -7mA, V_{DD} = 3V OSCO$_{RC}$, I_{OH} = -0.7mA, V_{DD} = 3V
Output Low Voltage	V_{OL}			GND + 0.4	V	I/O ports, I_{OL} = 8mA, V_{DD} = 3V OSCO$_{RC}$, I_{OL} = 1.0mA, V_{DD} = 3V

AC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, unless otherwise specified)

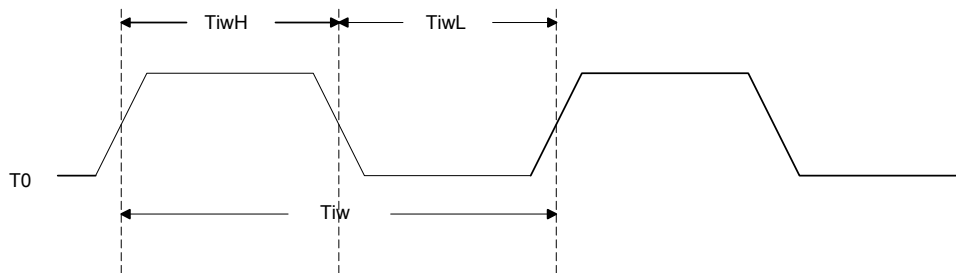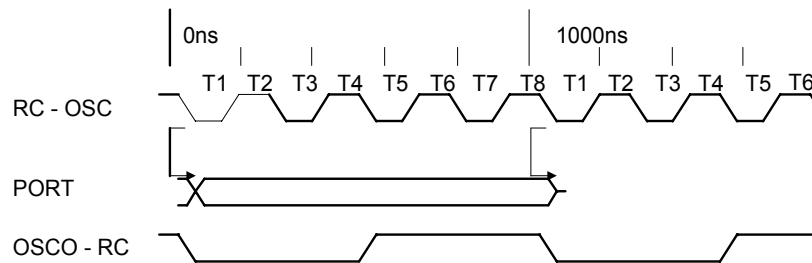| Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	T_{OSC1}			1	s	Crystal Osc = 32.768KHz, V_{DD} = 3.0V
Oscillator Start Time	T_{OSC2}			35	ms	Ceramic Osc = 400KHz, V_{DD} = 3.0V
Oscillator Start Time	T_{OSC3}			5	ms	RC Osc = 400KHz, V_{DD} = 3.0V
WDT Period	T_{WDT}	7	18		ms	V_{DD} = 3.0V
Frequency Stability (crystal)	Δ F/F			1	PPM	Crystal oscillator: [F(3.0)-F(2.7)]/F(3.0)
Frequency Variation (crystal)	Δ F/F			10	PPM	Crystal oscillator: C1 = C2 = 5 - 30P
Frequency Stability (ceramic)	Δ F/F			0.1	%	Ceramic resonator OSC:[F(3.0)-F(2.7)]/F(3.0)
Frequency Variation (RC)	Δ F/F			$\pm$ 20	%	Include supply voltage and chip to chip variation
Frequency Stability (RC)	Δ F/F			5	%	RC oscillator (1MHz): [F(3.0)-F(2.7)]/F(3.0)

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T$_{CY}$	Instruction Cycle Time	1		122	μs	
T$_{IW}$	T0 Input Width	(T$_{CY}$ + 40)/N			ns	N = Prescaler divide ratio
T$_{IWH}$	High Pulse Width	1/2 t$_{IW}$			ns	
T$_{IWL}$	LOW Pulse Width	1/2 t$_{IW}$			ns	

Timing Waveform

T0 Input Waveform

RC OSCO Timing Waveform

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Typical RC oscillator Resistor vs. Frequency: (V_{DD} = 5V, for reference only)

Typical RC Oscillator Resistor vs. Frequency: (V_{DD} = 3V, for reference only)
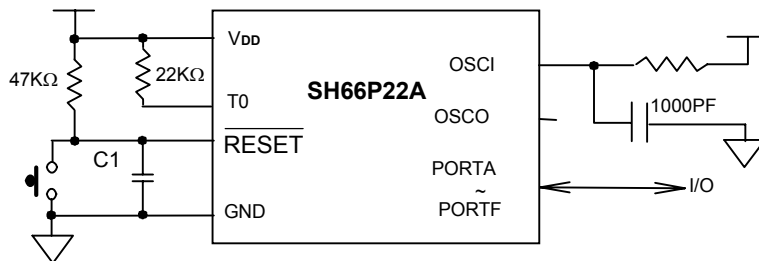
Application Circuit (for reference only)

AP1

(1) Operating voltage: 5.0V
(2) Oscillator: Ceramic resonator 400KHz
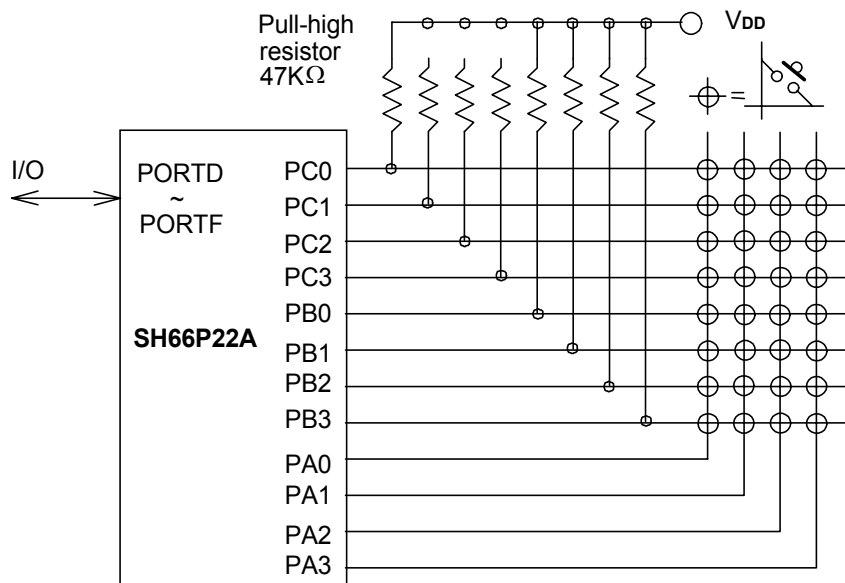(3) T0 input timer clock / counter
(4) PORTA - F: I/O

AP2

(1) Operating voltage: 5.0V.
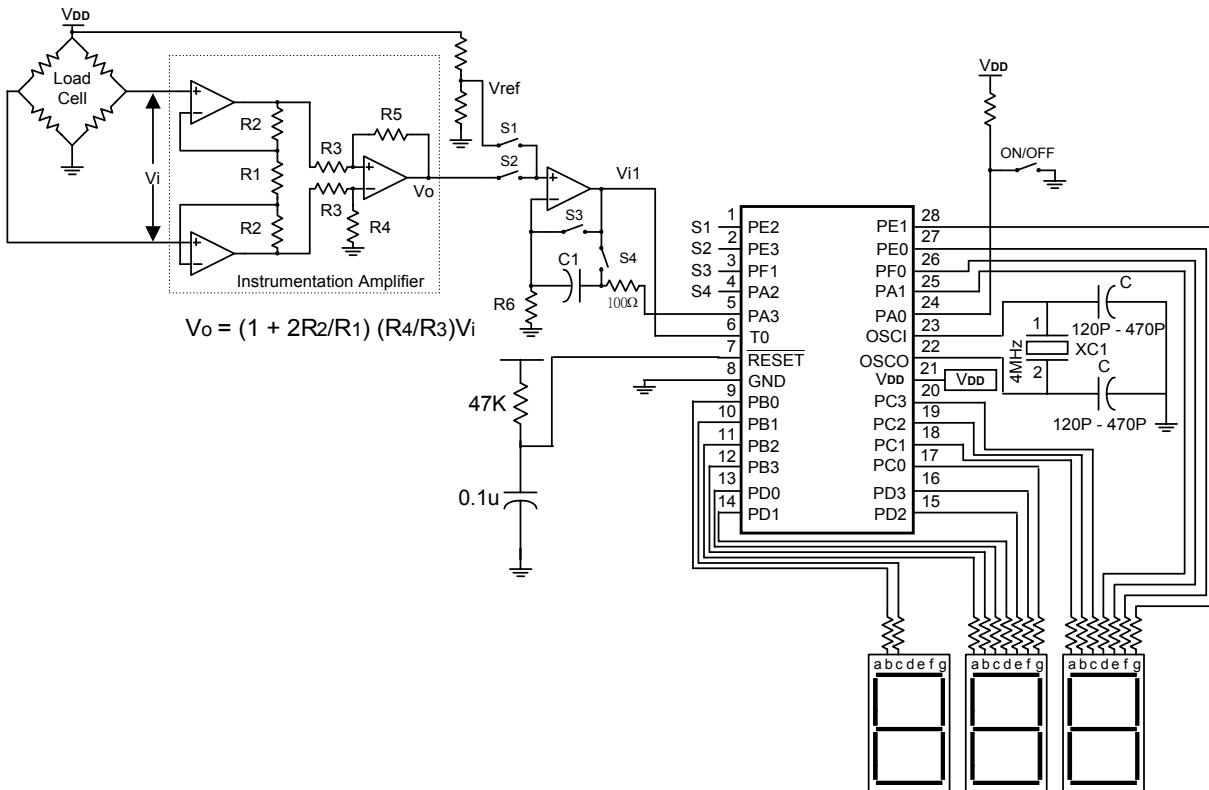(2) Oscillator: RC 400KHz.
(3) PORTA - E: I/O

AP3

(1) PORTA - C: as scan KEY BOARD (32 keys)
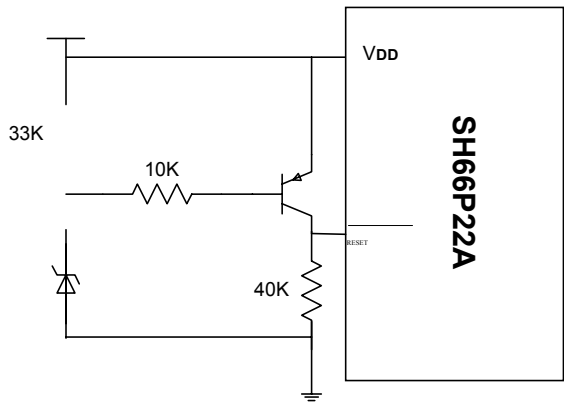(2) PORTD - F: I/O

Ap4 (Weight Scale)

(1) Operating voltage: 5.0V

(2) Oscillator: Ceramic resonator 4MHz

(3) Port A0: External interrupt input for ON/OFF switch

(4) Port E2, E3, F1, A2: S4 - S1 analog switch control signals that control Vil is being charged or discharged by both the reference voltage (Vref) and the amplified voltage (Vo). The charging and discharging times are determined by the values of C1, R4 and the threshold voltage of the T$_0$ input pin and the ADC resolution can be up to 8 bit

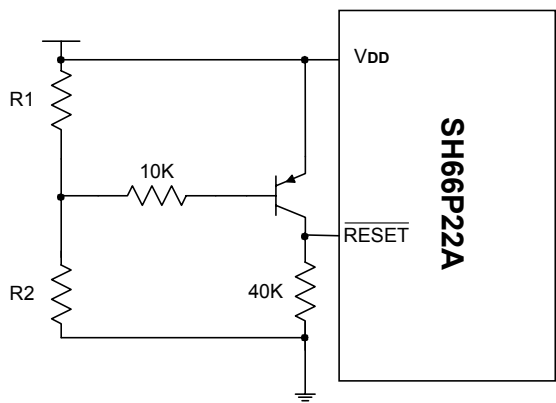(5) Other Ports: Sink seven-segment LED current directly. 0 - 199 can be displayed in this configuration

$$V_O = (1 + 2R_2/R_1) (R_4/R_3)V_i$$

AP5:

Reset Protection Circuit 1

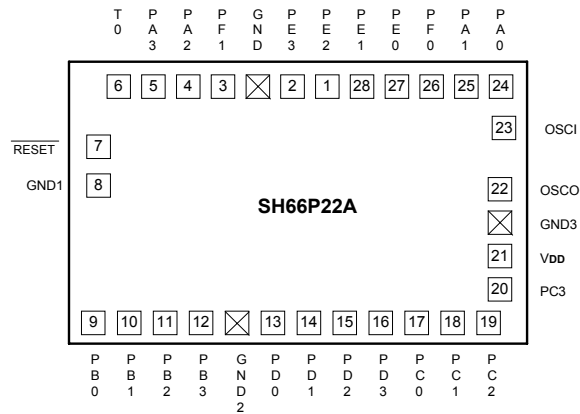$\overline{RESET}$ will be pulled to GND when V**DD** goes lower than Zener voltage + 0.7V.

AP6:

Reset Protection Circuit 2

$\overline{RESET}$ will be pulled to GND when (V**DD** X R1/(R1 + R2)) is lower than 0.7V

Bonding Diagram

NOTE:

1. GND1, GND2&GND3 BONDING TO GROUND.

2. SUBSTRATE CONNECT TO GROUND.

unit: µm

Pad No	Designation	X	Y
1	PE 2	63.00	725.35
2	PE 3	-67.00	725.35
	GND1	-199.70	725.35
3	PF 1	-332.40	725.35
4	PA 2	-462.40	725.35
5	PA 3	-592.40	725.35
6	T0	-752.95	725.35
7	$\overline{RESET}$	-818.85	481.85
8	GND	-818.15	350.90
9	PB 0	-792.15	-725.30
10	PB 1	-662.15	-725.30
11	PB 2	-532.15	-725.30
12	PB 3	-402.15	-725.30
12	GND2	-269.45	-725.30
13	PD 0	-136.75	-725.30
14	PD 1	-6.75	-725.30

Pad No	Designation	X	Y
15	PD 2	123.25	-725.30
16	PD 3	253.25	-725.30
17	PC 0	386.95	-725.30
18	PC 1	516.95	-725.30
19	PC 2	646.95	-725.30
20	PC 3	775.80	-506.95
21	VDD	780.55	-328.00
21	GND3	771.05	-196.60
22	OSCO	780.55	-65.65
23	OSCI	780.55	462.60
24	PA 0	716.70	725.35
25	PA 1	586.70	725.35
26	PF 0	456.70	725.35
27	PE 0	323.00	725.35
28	PE 1	193.00	725.35

Ordering Information

Part No.	Package	Packing
SH66P22AH-yyxxx/000HR	Chip Form	Tray
SH66P22AK-yyxxx/028KU	28L SKINNY	Tube
SH66P22AM-yyxxx/028MU	28L SOP	Tube
SH66P22A-yyxxx/028DU	28L DIP	Tube

Note:

(1) "-yyxxx": "yy" means 2 bits option and "xxx" means 3 bits code seriary number. If the product is OTP type and in blank order, those bits should be none.
(2) The data after mark "/" in Part No. block is the package and packing information for ordering.
(3) The size of those package types are showed in "Package Information" (Page24 - Page26).
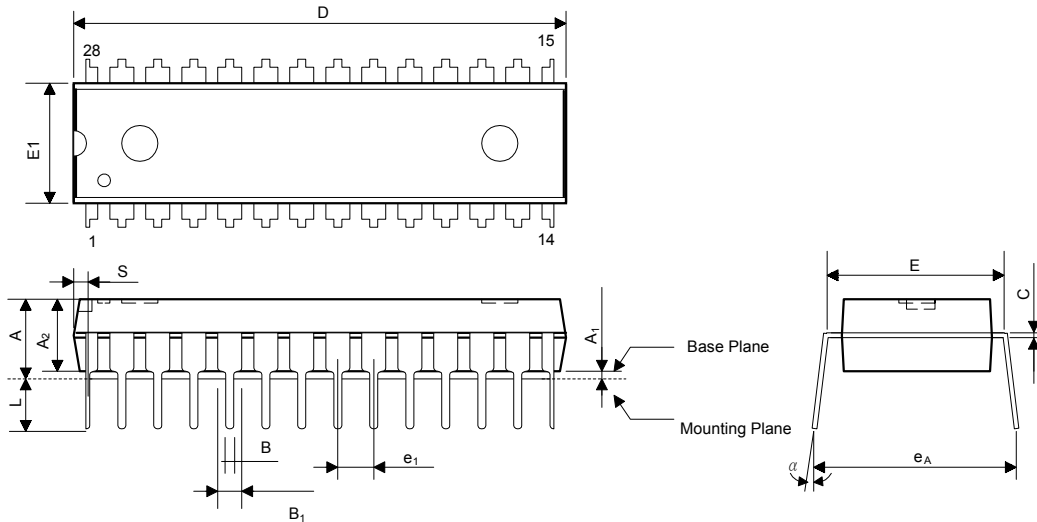(4) Any other package or packing request, please refer to following table.

	Package		Packing
D	DIP	R	Normal package size and in tray packing
F	QFP	U	Normal package size and in tube packing
H	CHIP	A	Normal package size and in tape & reel packing
J	CER-DIP	D	Larger package size and in tray packing
K	SKINNY	L	Larger package size and in tube packing
L	PLCC	B	Larger package size and in tape & reel packing
M	SOP	T	Smaller package size and in tray packing
N	OTHER	S	Smaller package size and in tube packing
Q	GOOD DIE ON WAFER	N	Smaller package size and in tape & reel packing
S	SOJ		
T	TO92		
V	VSOP/TSOP		
W	WAFER		
X	TSSOP		

Package Information

SKINNY_28L Outline Dimensions

unit: inches/mm

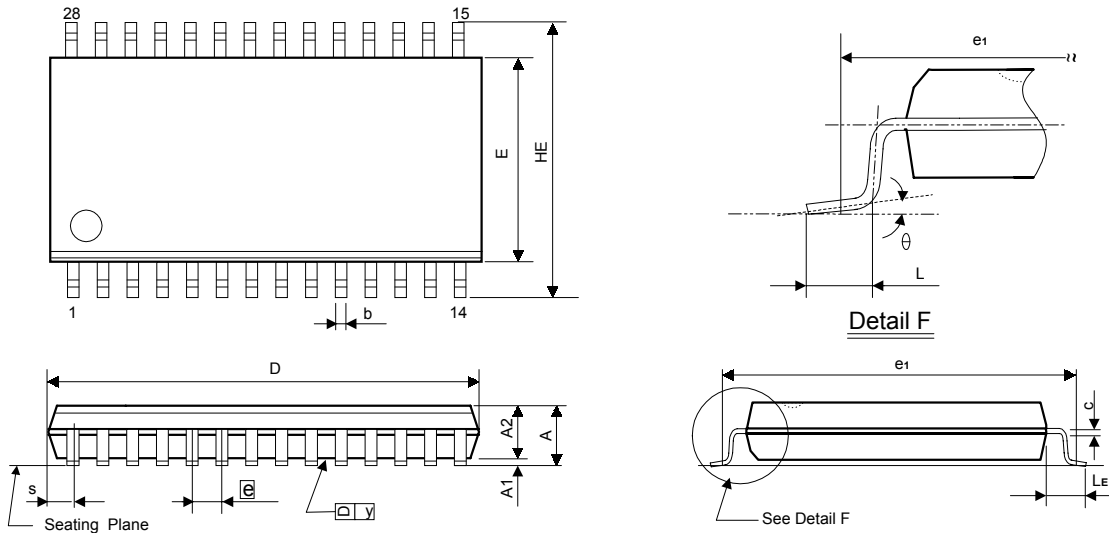| Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.005	3.30 ± 0.13
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.388 Typ. (1.400 Max.)	35.26 Typ. (35.56 Max.)
E	0.310 ± 0.010	7.87 ± 0.25
E_1	0.288 ± 0.005	7.32 ± 0.13
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.350 ± 0.020	8.89 ± 0.51
S	0.055 Max.	1.40 Max.

Notes:

1. The maximum value of dimension D includes the end flash.
2. Dimension E_1 does not include the resin fins.
3. Dimension S includes the end flash.

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SOP 28L Outline Dimensions   unit: inches/mm

Detail F

See Detail F

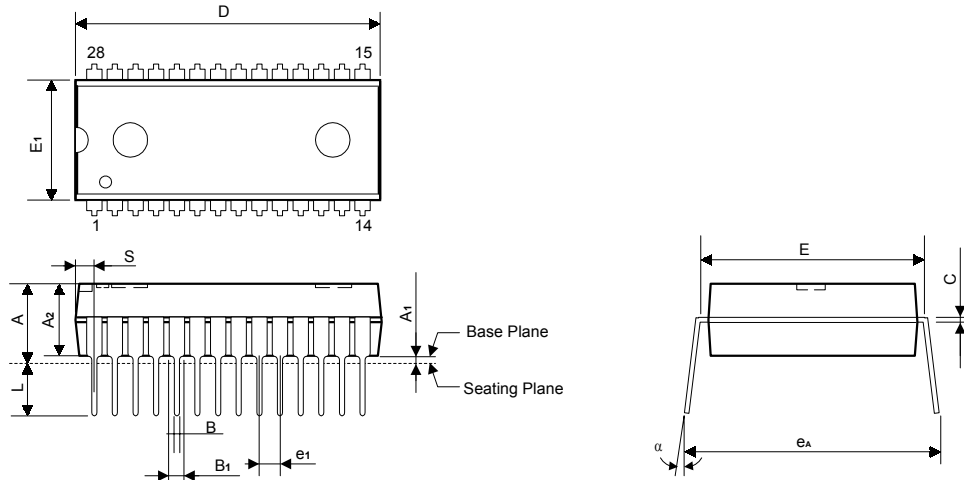| Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A1	0.004 Min.	0.10 Min.
A2	0.093 ± 0.005	2.36 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
c	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.705 ± 0.020	17.91 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e1	0.376 NOM.	9.40 NOM.
HE	0.406 ± 0.012	10.31 ± 0.31
L	0.036 ± 0.008	0.91 ± 0.20
LE	0.055 ± 0.008	1.40 ± 0.20
S	0.043 Max.	1.09 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

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DIP 28L Outline Dimensions   unit: inches/mm

Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A$_1$	0.010 Min.	0.25 Min.
A$_2$	0.155 ± 0.010	3.94 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B$_1$	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.460 Typ. (1.480 Max.)	37.08 Typ. (37.59 Max.)
E	0.600 ± 0.010	15.24 ± 0.25
E$_1$	0.550 Typ. (0.562 Max.)	13.97 Typ. (14.27 Max.)
e$_1$	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e$_A$	0.655 ± 0.035	16.64 ± 0.89
S	0.090 Max.	2.29 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E$_1$ does not include resin fins.
3. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
2.4	Add package and packing information in ordering information	Jul.2004
2.3	Add P-DIP 28L package	Oct. 2002
2.2	Change RC Frequency Variation to ±20%	Apr. 2002
2.1	Add Reset Protection Circuit (AP5 and AP6)	Dec. 2001
2.0	Change SOP (W.B.) 28L package to SOP (N.B.) 28L package	Nov. 2001
1.0	Original	Jul. 2000