Advance Data Sheet

T-75-11-29

T7290 DS1/T1/CEPT Line Interface

Features

- Fully integrated ISDN DS1/T1/CEPT line interface
- Compatibility with CB119, Pub 43801, Pub 43802, Pub 62411, TR-TSY-000170, TR-TSY-000009, CCITT G.703, G.735, G.823, and I.431 specifications
- Dual-rail system interface
- On-chip transmit equalization
- On-chip jitter attenuator
- Monolithic clock recovery with acquisition aide
- Low-power CMOS in a 28-pin, plastic DIP or SOJ package
- High jitter accommodation (>0.4 U.I.)
- Two on-chip phase-lock loops (PLLs) to facilitate clock synchronization without external crystals
- Three clocking modes to accommodate any system clocking requirements
- Multiple link status and alarm features
- Microprocessor interface option for control features
- AIS (Blue Alarm) transmission
- Loopback modes for fault isolation
- Minimal external circuitry required

Description

The T7290 ISDN DS1/T1/CEPT Line Interface is a single-chip, CMOS line transceiver capable of operation at the domestic DS1/T1 carrier rate (1.544 Mbits/s) or the international CEPT1 rate (2.048 Mbits/s). The T7290 device combines features found in existing line-interface devices and adds other desirable features.

The on-chip, low-impedance output drivers provide shaped waveforms to the transformer, guaranteeing template conformance. The T7290 device interfaces to the digital cross-connect (DSX) at lengths up to 655 feet during DS1 operation and interfaces to line impedances of 75 Ω or 120 Ω during CEPT operation. T7290 line interface is also capable of transmitting waveforms compatible with T1 lines.

The T7290 line interface provides phase-locked loop clock recovery and data retiming on received data. Also, on-chip, selectable, jitter attenuation is available. The jitter attenuator can be placed in the receive or transmit data path. No external crystals are required with the T7290 device.

Digital control circuitry allows for multiple loopbacks, testing, and alarm status monitoring. A microprocessor interface option allows for either control via a microprocessor or direct pin-selectable control (hardware mode).

The T7290 device is manufactured by using a low-power CMOS technology. The block diagram is shown in Figure 1.

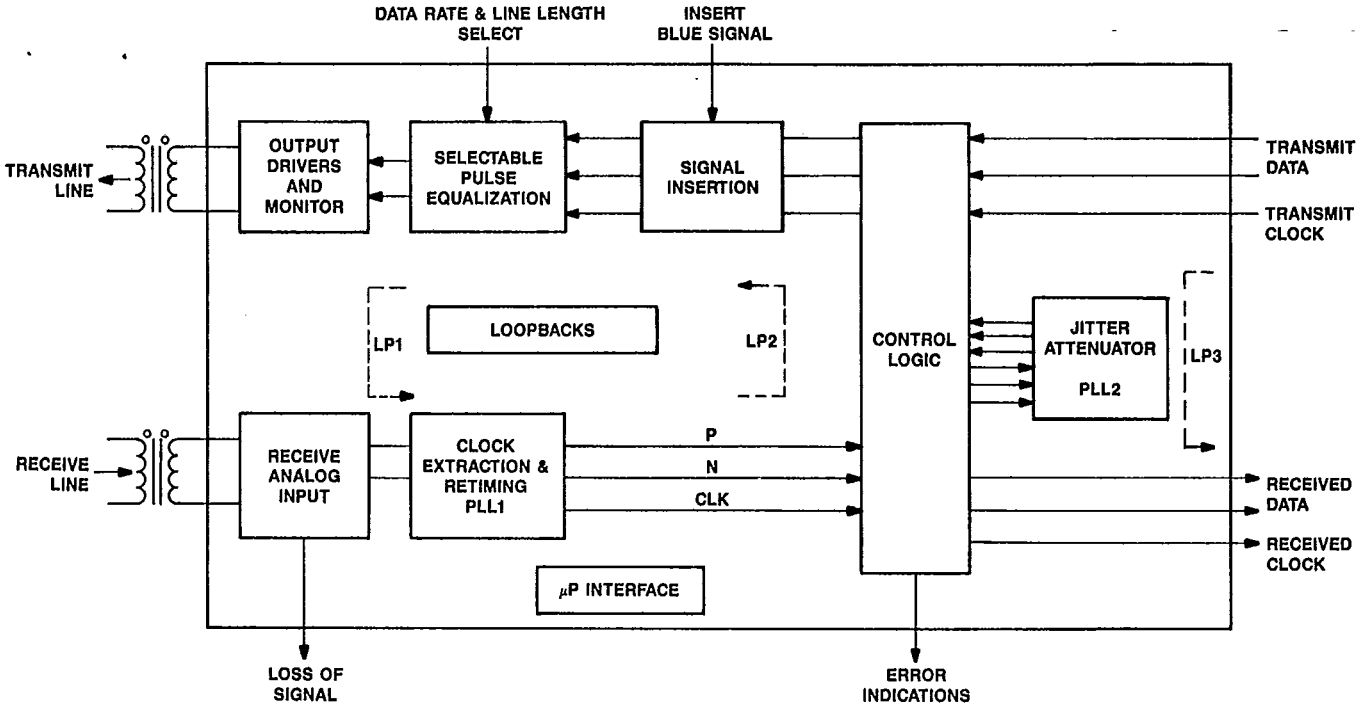


Figure 1. Block Diagram

User Information

Pin Descriptions

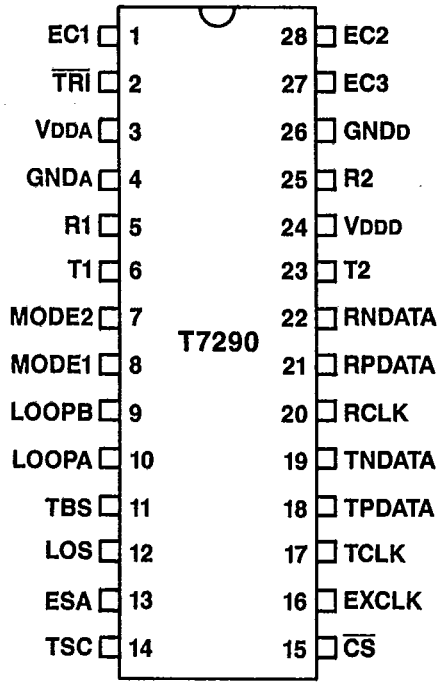


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1,27,28	EC1—EC3	I	**Equalizer/Rate Control 1—3.** Three control leads for selecting transmit equalizers.
2	$\overline{TRI}$	I	**3-State (Active-Low).** This pin is set low to 3-state all digital output buffers. This control should be used during in-circuit testing.
3	VDDA	—	**5 V ± 10% Analog Supply.**
4	GNDA	I	**Analog Ground.**
5	R1	I	**Receive Bipolar Ring.** Negative bipolar receive data.
6	T1	I	**Receive Bipolar Tip.** Positive bipolar receive data.
7, 8	MODE2, MODE1	I	**Mode Select 2 and 1.** Two control leads for selecting clock and data paths through the jitter attenuator.
9, 10	LOOPB, LOOPA	I	**Loopback Control B and A.** Two control leads for selecting clock and data loopback paths.
11	TBS	I	**Transmit Blue Signal.** This pin is set high to transmit the blue signal. A remote loopback has priority over the transmit blue signal if the remote loopback and transmit blue signal are operated simultaneously.
12	LOS	O	**Loss of Signal.** This pin is set high upon the loss of the data signal at the receiver inputs. LOS can be tied directly to TBS to initiate a transmit blue signal upon loss of signal.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
13	ESA	O	**Jitter Attenuator Underflow/Overflow Alarm.** This pin is set high if the phase jitter of the incoming signal exceeds the limits of the jitter attenuator.
14	TSC	O	**Transmitter Short-Circuit.** This pin is set high if either T2 or R2 is shorted to the power supply or ground or if T2 and R2 are shorted together.
15	$\overline{CS}$	I	**Chip Select for Microprocessor Interface (Active-Low).** $\overline{CS}$ loads data into the device during its falling edge and latches the data during its rising edge. $\overline{CS}$ is set low for hardware mode.
16	EXCLK	I	**External Clock.** DS1/T1 clock signal (1.544 MHz ± 130 ppm) or CEPT clock signal (2.048 MHz ± 50 ppm) for transmit blue signal, loss of signal clock insertion, jitter attenuator calibration, and PLL1 acquisition aide. This clock should be void of jitter.
17	TCLK	I	**Transmit Clock.** DS1/T1 clock signal (1.544 MHz ± 130 ppm) or CEPT clock signal (2.048 MHz ± 50 ppm).
18	TPDATA	I	**Transmit Positive Data.** DS1/T1 (1.544 Mbits/s) or CEPT (2.048 Mbits/s) positive bipolar data.
19	TNDATA	I	**Transmit Negative Data.** DS1/T1 (1.544 Mbits/s) or CEPT (2.048 Mbits/s) negative bipolar data.
20	RCLK	O	**Receive Clock.** Receive clock signal for the terminal equipment.
21	RPDATA	O	**Receive Positive Data.** DS1/T1 (1.544 Mbits/s) or CEPT (2.048 Mbits/s) positive data.
22	RNDATA	O	**Receive Negative Data.** DS1/T1 (1.544 Mbits/s) or CEPT (2.048 Mbits/s) negative data.
23	T2	O	**Transmit Bipolar Tip.** Positive bipolar transmit data.
24	V_{DDD}	—	**5 V ± 10% Digital Supply.**
25	R2	O	**Transmit Bipolar Ring.** Negative bipolar transmit data.
26	GND_D	—	**Digital Ground.**

Architecture

Receive Path

Data Interface. The receive line-interface transmission format of the T7290 device is alternate mark inversion (AMI). The receive digital output format is dual-rail, non-return to zero (NRZ). (See Receiver Specifications under the Electrical Characteristics section.)

Clock Recovery and Data Retiming. The bipolar input signals from T1 and R1 are peak-detected and sliced by the receiver front-end. Timing recovery is performed by a phase-locked loop (PLL1). An acquisition aide circuit for PLL1 trains an internal oscillator to either the DS1/T1 or CEPT1 frequency by using EXCLK as a reference. EC1, EC2, and EC3 rate control inputs must be set appropriately for DS1 or CEPT operation.

Jitter. PLL1 is designed to accommodate large amounts of input jitter with high power-supply rejection for operation in noisy environments. PLL1 has a minimum input jitter tolerance exceeding all requirements shown in Figure 7. The receiver transfers incoming jitter to RCLK with no more than 2 dB of gain at any frequency.

Data Patterns. Any data pattern with a minimum long-term 1s density of 12.5% with 15 or less consecutive 0s is allowed.

Loss-of-Signal. Both digital and analog loss-of-signal detection is used in the T7290 device. The digital signal detector is described later under the Digital Logic section. The analog signal detector uses the output of the receiver peak detector to determine if a signal is present at T1 and R1. If the input amplitude drops below approximately 0.48 V for DS1/T1 operation or 0.28 V for CEPT operation, the analog detector output becomes active. Hysteresis (250 mV) is provided in the analog detector to eliminate LOS chattering. In normal operation, either the analog or the digital detector sets LOS high; however, in full local loopback (LP1), only the digital signal detector is used to monitor the looped signal.

Transmit Path

Output Pulse Shape. A summary of the transmitter specifications are given under the Electrical Characteristics section. The T1 output pulse shape is shown in Figure 3. Pulse overshoot variations are allowed according to the limits shown in Figure 4. The DS1 pulse shape template is specified at the DSX and is illustrated in Figure 5. CEPT transmit waveforms at the device output conform to the template shown in Figure 6.

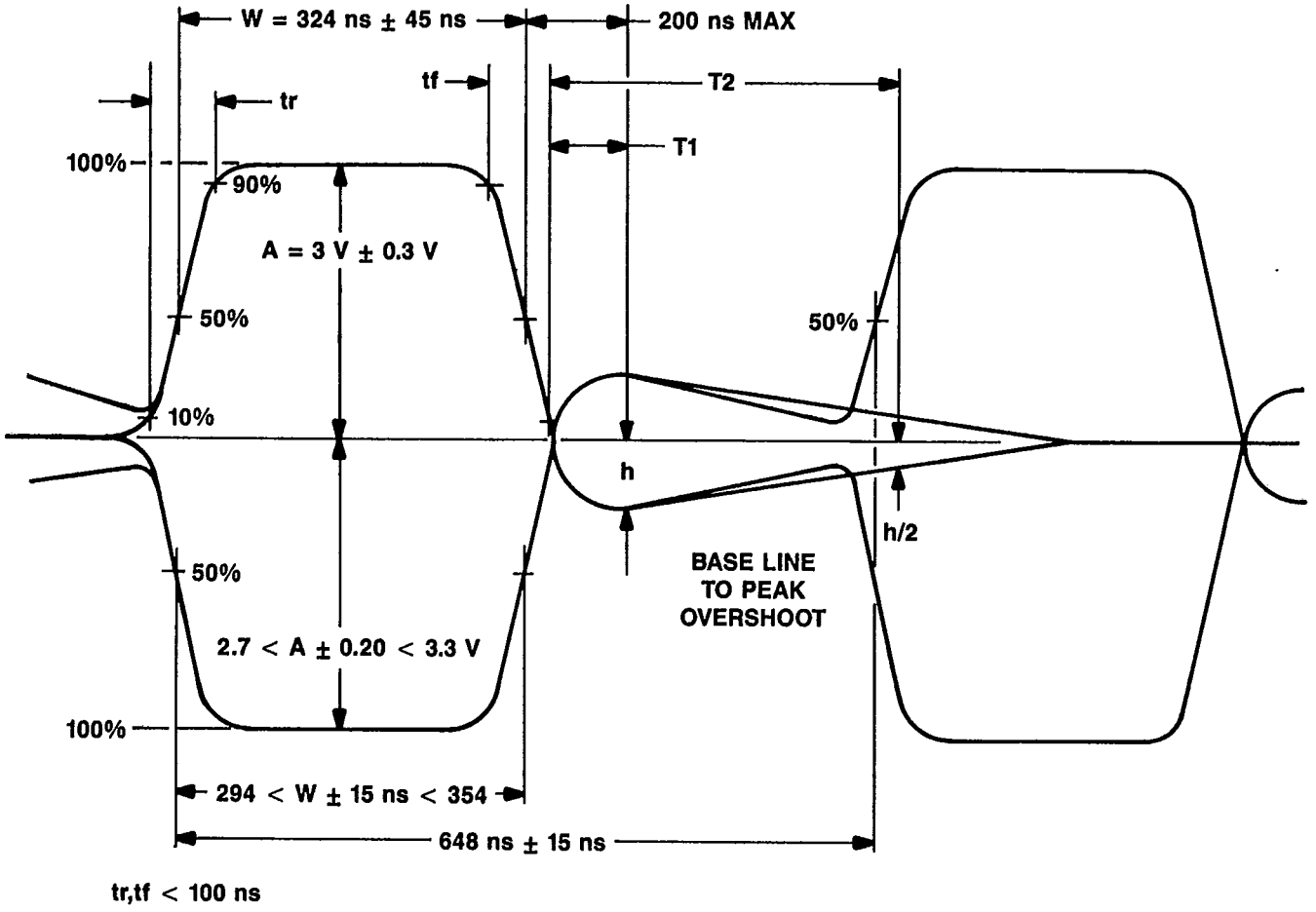
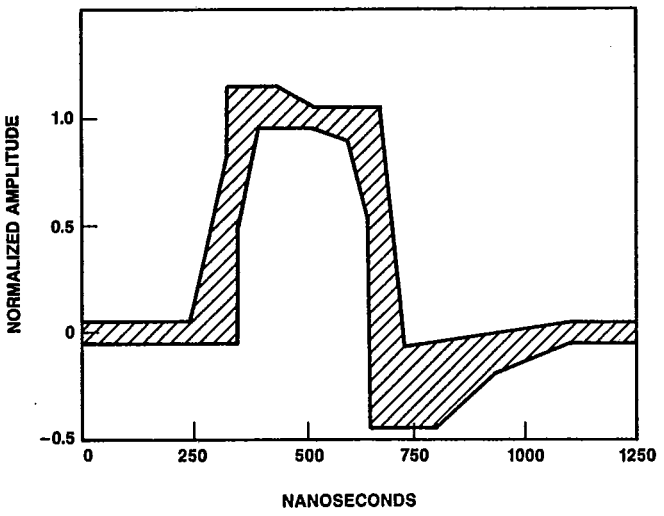


Figure 3. T1 Output Pulse Characteristics

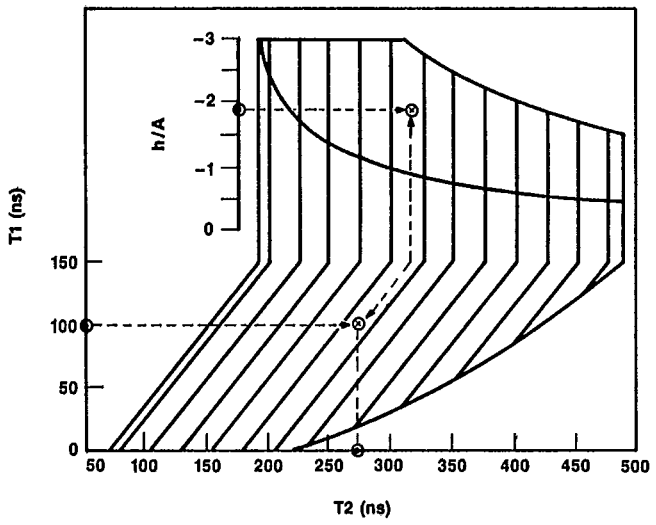


DSX-1 Pulse Template Corner Points

Maximum Curve		Minimum Curve	
ns	Normalized Voltage	ns	Normalized Voltage
0	0.05	0	−0.05
250	0.05	350	−0.05
325	0.80	350	0.50
325	1.15	400	0.95
425	1.15	500	0.95
500	1.05	600	0.90
675	1.05	650	0.50
725	−0.07	650	−0.45
875	0.05	800	−0.45
1250	0.05	925	−0.20
		1100	−0.05
		1250	−0.05

Note: Successive corner points are joined by straight lines.

Figure 5. DSX-1 Isolated Pulse Template



⊗ INDICATES EXAMPLE WHICH CONFORMS WITH LIMITS

Figure 4. T1 Pulse Overshoot Limits

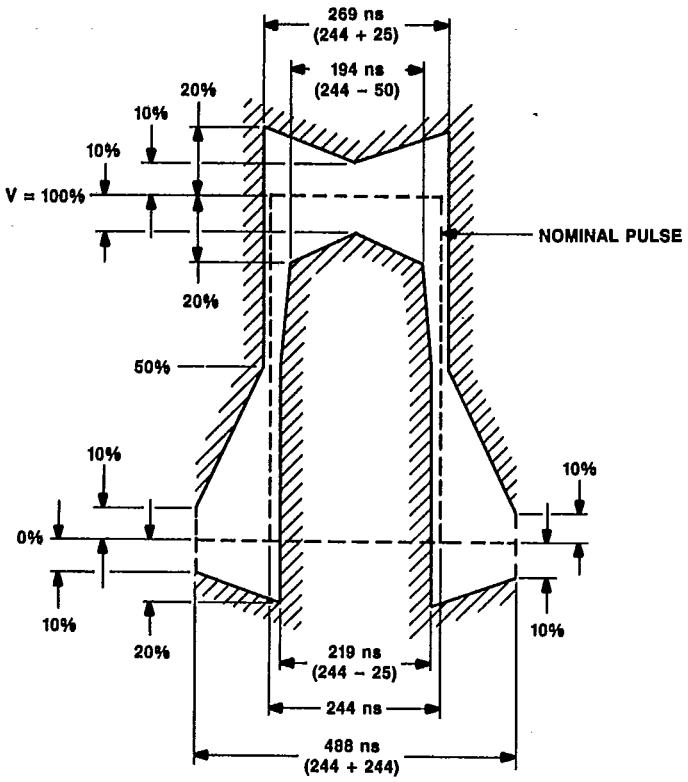


Figure 6. CCITT G.703 Pulse Template

Output Pulse Generation. The transmitter accepts a clock with positive and negative data (dual-rail NRZ format) and converts the signal to a balanced bipolar data signal (AMI format). Positive 1s are produced by a positive pulse on T2, and negative 1s are produced by a positive pulse on R2. Binary 0s are converted to null pulses. All pulse shapes are controlled on-chip according to equalizer control inputs as defined in Table 2. Transmitter specifications are listed under the Electrical Characteristics section.

Table 2. Equalizer/Rate Control

Service	Equalization*	Maximum† Cable Loss	EC1	EC2	EC3
T1	—	22‡	0	0	0
DS1	0' — 131'	0.6	0	0	1
DS1	131' — 262'	1.2	0	1	0
DS1	262' — 393'	1.8	0	1	1
DS1	393' — 524'	2.4	1	0	0
DS1	524' — 655'	3.0	1	0	1
CEPT	75 Ω	—	1	1	0
CEPT	120 Ω	—	1	1	1

* Distance to DSX in feet for 22-Ga. PIC (ABAM) Cable [DS1 only]. Use maximum loss figures for other cable types.
† dB at 772 kHz.
‡ According to *FCC Part 68, Subpart D, Option A* for 0 dB line build-out.

Jitter Attenuation.

Jitter transfer functions describe the amount of jitter that is delivered from the input to the output of specified equipment. The jitter attenuator circuit can be placed in the receive data path or the transmit data path, or it can be omitted altogether. Placement of this circuit is controlled as described in Table 3. When attenuation is selected, the T7290 device exhibits a jitter transfer function which has no peaking and a single 14.5 Hz pole frequency. Figure 8 displays a typical jitter transfer function.

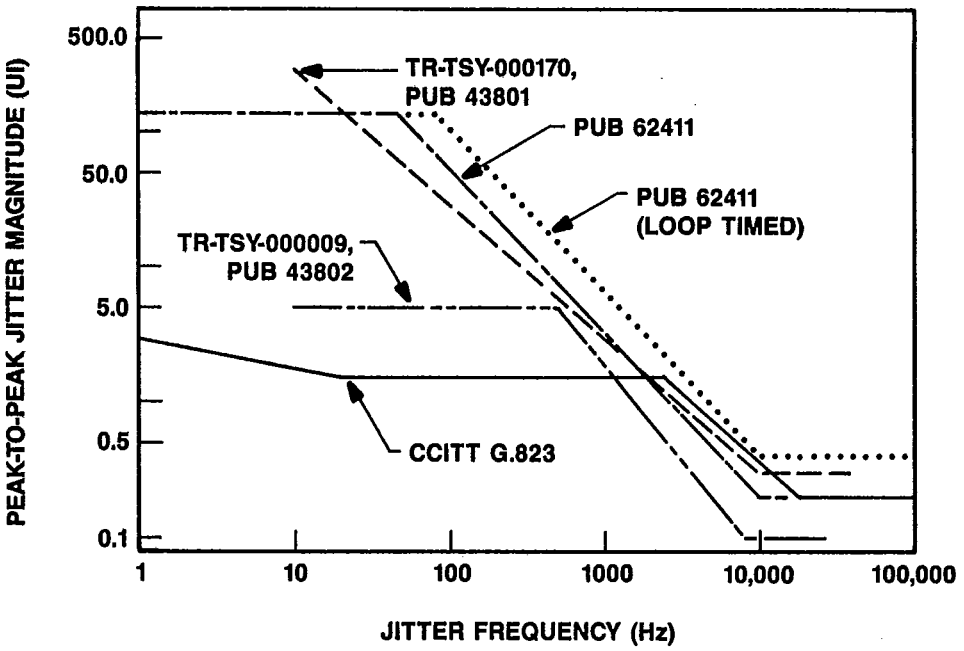
The amount of generated output jitter when no input jitter is present is measured by using the scheme shown in Figure 9. The jitter filters depicted represent the PUB 62411 specification for a 1.544 MHz data rate. The jitter produced at the labeled points does not exceed the following peak-to-peak levels: 0.05 U.I. at point 1, 0.025 U.I. at point 2, 0.025 U.I. at point 3, and 0.02 U.I. at point 4. A similar test can be performed for CCITT I.431 qualification at the 2.048 MHz data rate. The two jitter filters of interest include 20 Hz — 100 kHz (0.125 U.I.) and 700 Hz — 100 kHz (0.02 U.I.).

The jitter tolerance of the attenuator meets the requirements of the TR-TSY-000009, PUB43802, and CCITT G.823 (see Figure 7). The attenuator also ensures that jitter accommodation is a minimum of 22 U.I. peak-to-peak (1 U.I. = 1 bit = 360°) during attenuation. The jitter attenuator function is the same for both transmit and receive paths.

Table 3. Connectivity of Jitter Attenuator

Connectivity of Jitter Attenuator	MODE1	MODE2
Bypass*	0	0
Transmit Path	0	1
Receive Path	1	0
Test Mode†	1	1

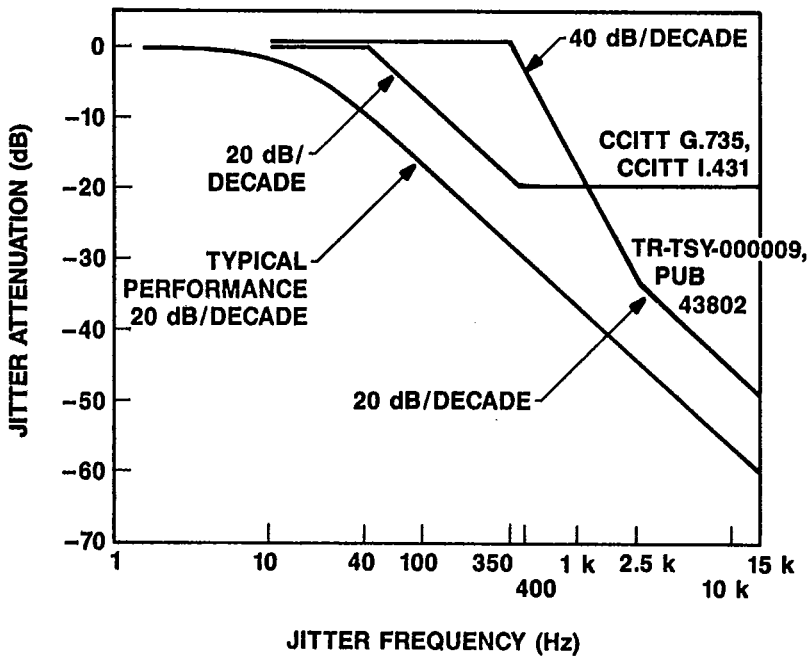
* Jitter attenuator is powered down during this mode (see Operating Conditions under the Electrical Characteristics Section).
† Not to be used for normal operation.



Data Points (Hz, U.I.)

CCITT G.823	TR-TSY-000170, PUB 43801	TR-TSY-000009, PUB 43802	PUB 62411	PUB 62411 Loop Timed
1, 2.9	10, 300	10, 5	1, 138	1, 138
20, 1.5	10k, 0.3	500, 5	48, 138	85, 138
2.4k, 1.5	50k, 0.3	8k, 0.1	10k, 0.2	10k, 0.4
18k, 0.2	—	40k, 0.1	100k, 0.2	100k, 0.4
100k, 0.2	—	—	—	—

Figure 7. Jitter Tolerance Requirements



Data Points (Hz, dB)

TR-TSY-000009, PUB 43802	CCITT G.735, CCITT I.431
10, 0.5	10, 0.5
350, 0.5	40, 0.5
2.5k, −33.6	400, −19.5
15k, −49.2	15k, −19.5

Figure 8. Jitter Transfer Function of the Jitter Attenuator

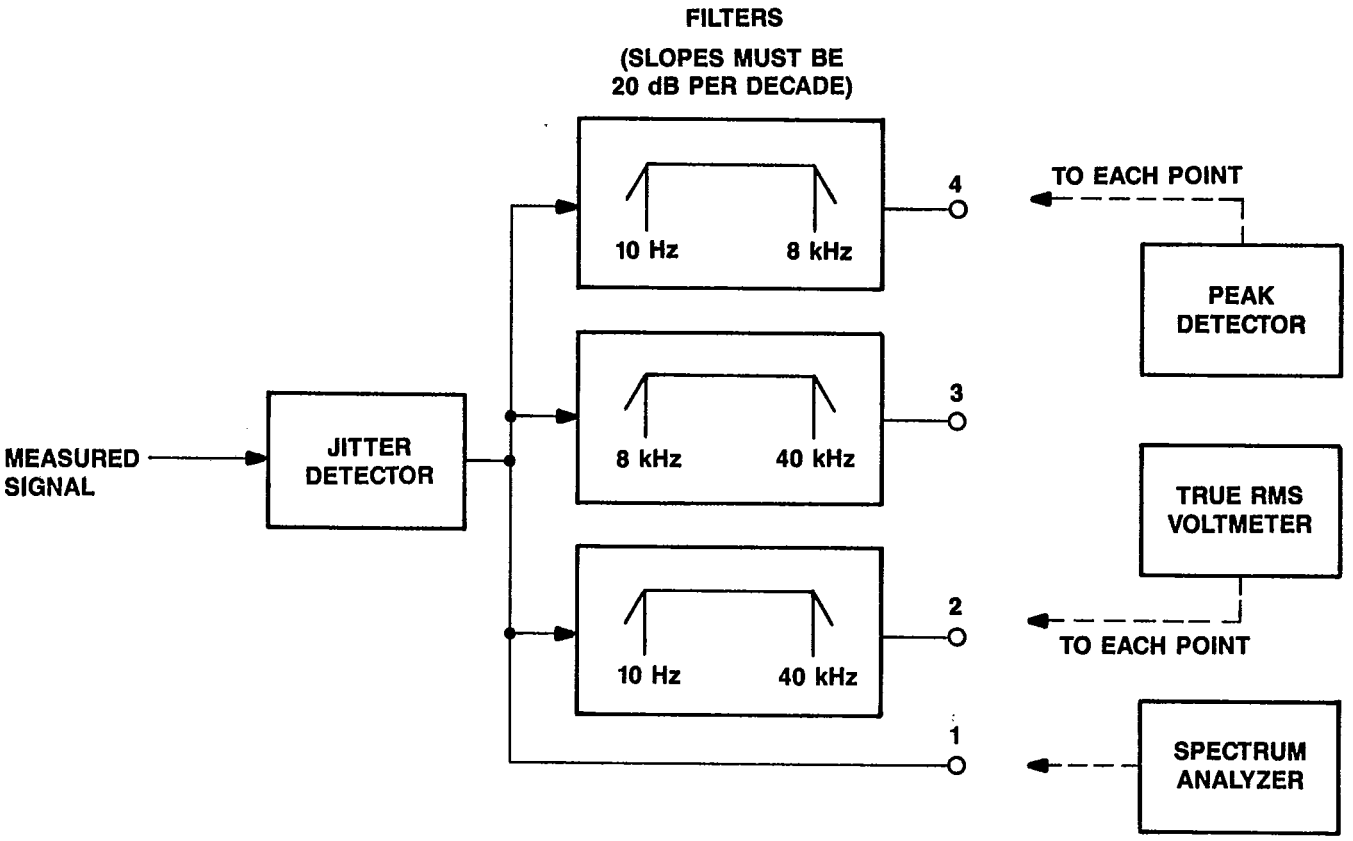


Figure 9. Measurement of Generated Jitter

Digital Logic

Alarms. There are three alarms: digital loss of signal (LOS), jitter attenuator underflow/overflow alarm (ESA), and transmitter short circuit (TSC).

A digital loss of signal (LOS = 1) is indicated if 128 or more consecutive 0s occur in the receive data stream during DS1/T1 operation. During CEPT operation, an LOS is indicated when 32 or more consecutive 0s occur in the receive data stream. LOS is then deactivated when four or more 1s occur in 32 bits of data (T1, DS1, and CEPT). This hysteresis effect eliminates LOS chattering. Upon LOS detection, the external clock (EXCLK) is automatically inserted for RCLK so that other system devices slaved to the line clock continue to operate.

A jitter attenuator underflow/overflow (ESA = 1) is indicated if the phase jitter exceeds the limits of the jitter attenuator. This signal is asserted until error-free operation resumes.

A transmitter monitor is provided to detect nonfunctioning links and protect the device from damage. If one of the transmitter's line drivers (T2 or R2) is shorted to the power supply or ground or if T2 and R2 are shorted together, a transmitter short-circuit (TSC = 1) is indicated, during which internal circuitry protects the device from damage. After a minimum of 32 clock cycles, the transmitter is powered up in its normal operating mode. If the error is still present, TSC remains set (eliminating TSC chattering), and the transmitter is again buffered for a minimum of 32 clock cycles. This process is continuously repeated until the error has disappeared, thus deactivating TSC.

AIS (Blue Signal) Generator. An all-1s insertion is provided by the transmitter synchronous with EXCLK. When transmit blue signal is set (TBS=1), a continuous stream of bipolar 1s is sent onto the line. The TPDATA and TNDATA inputs are ignored during this mode. If the LOS output is externally connected to the TBS input, an LOS error initiates a transmit blue signal as long as LOS=1. Also, TBS input is ignored when a remote loopback is selected.

Microprocessor Interface. A chip select input ($\overline{CS}$) configures the device in either hardware mode or microprocessor mode. The chip-select function applies to the following inputs: MODE1, MODE2, EC1, EC2, EC3, TBS, LOOPA, and LOOPB. Hardware mode is used when no microprocessor is available in the system, and these inputs need not be synchronous with any specific system clock. Any change on these input pins is directly fed into the device. To maintain hardware mode, set $\overline{CS}$=0. In microprocessor mode, new digital control inputs are loaded into the T7290 device during the falling edge of $\overline{CS}$ and are latched during the rising edge of $\overline{CS}$. A timing diagram of this function is shown in Figure 15.

In-Circuit Testing. The device has the ability to allow for in-circuit testing by activating 3-state mode ($\overline{TRI}$ = 0). During this mode, all digital output buffers (RCLK, RPDATA, RNDATA, LOS, ESA, and TSC) are 3-stated.

Loopbacks. The T7290 device has three independent loopback paths, which are activated according to Table 4.

A full local loopback (LP1) connects the transmitter output data to the input of the receiver front-end, producing a loopback which exercises the maximum amount of device circuitry. The external input from T1 and R1 is ignored and LOS is indicated if no signal is looped from the transmitter. Valid transmit output data continues to be sent to the network.

A remote loopback (LP2) loops the recovered clock and retimed data from the receive bipolar inputs into the transmitter and back onto the line. The receive front-end, receive PLL1, jitter attenuator (if engaged), and transmit driver circuitry are all exercised. The external transmit clock and data and TBS input are ignored. Valid receive output data continues to be sent to RPDATA and RNDATA. This loop can be used to isolate failures between systems.

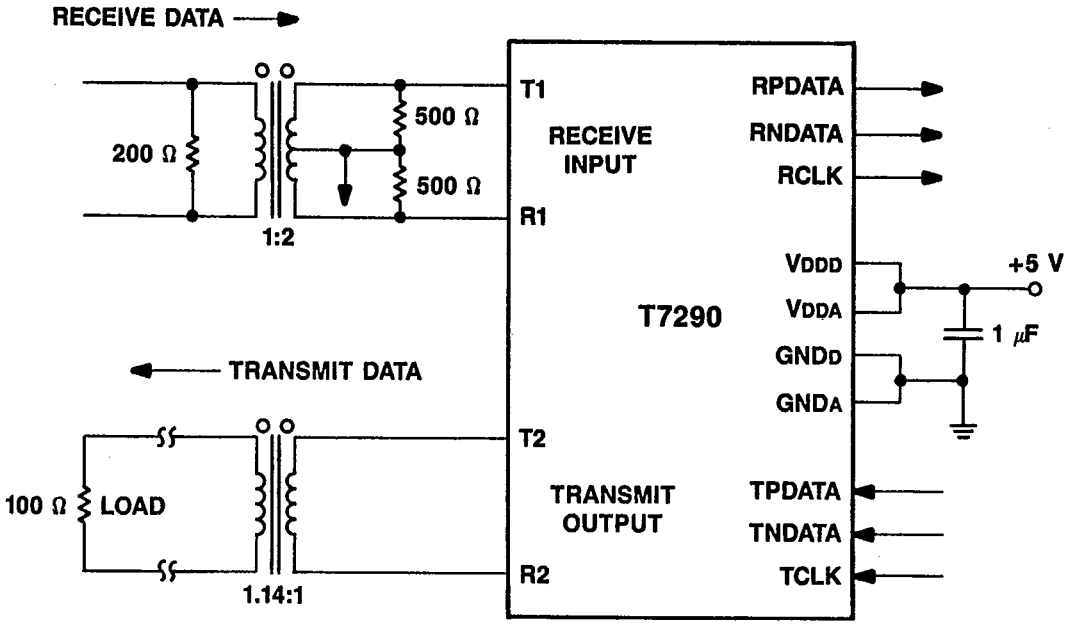
A digital local loopback (LP3) directly loops the transmit clock and data to the receive clock and data output pins. The blue signal can be transmitted when in this loopback.

Table 4. Loopback Control

Operation	Symbol	LOOPA	LOOPB
Normal	—	0	0
Digital Local Loopback	LP3	0	1
Remote Loopback	LP2	1	0
Full Local Loopback	LP1	1	1

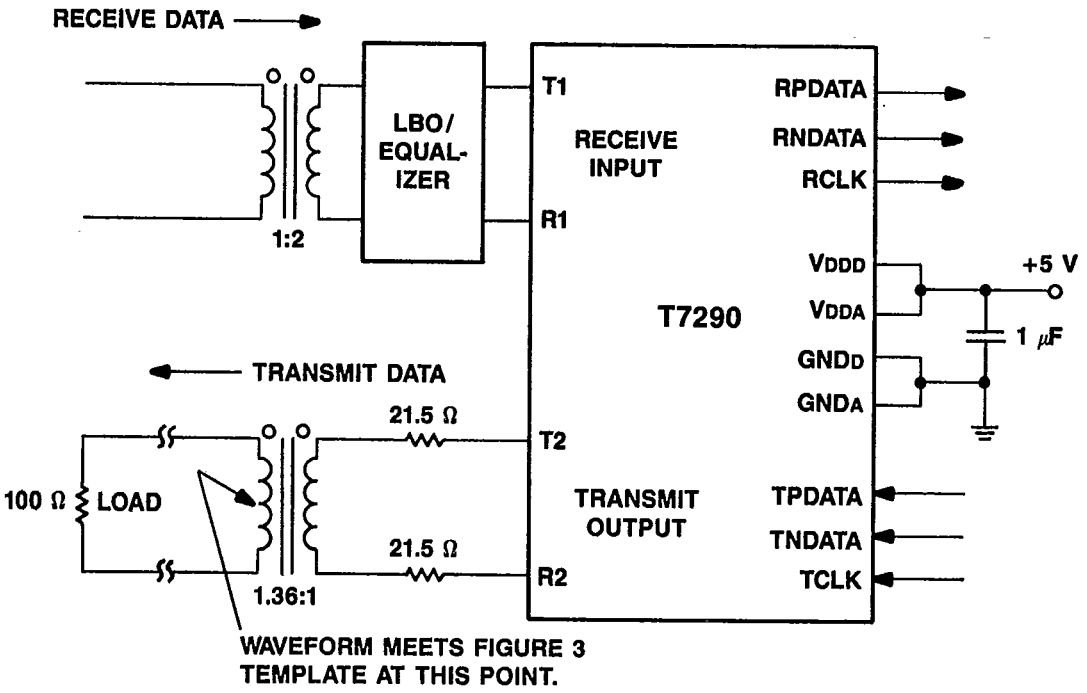
Applications

The following figures are applications for the T7290 device.



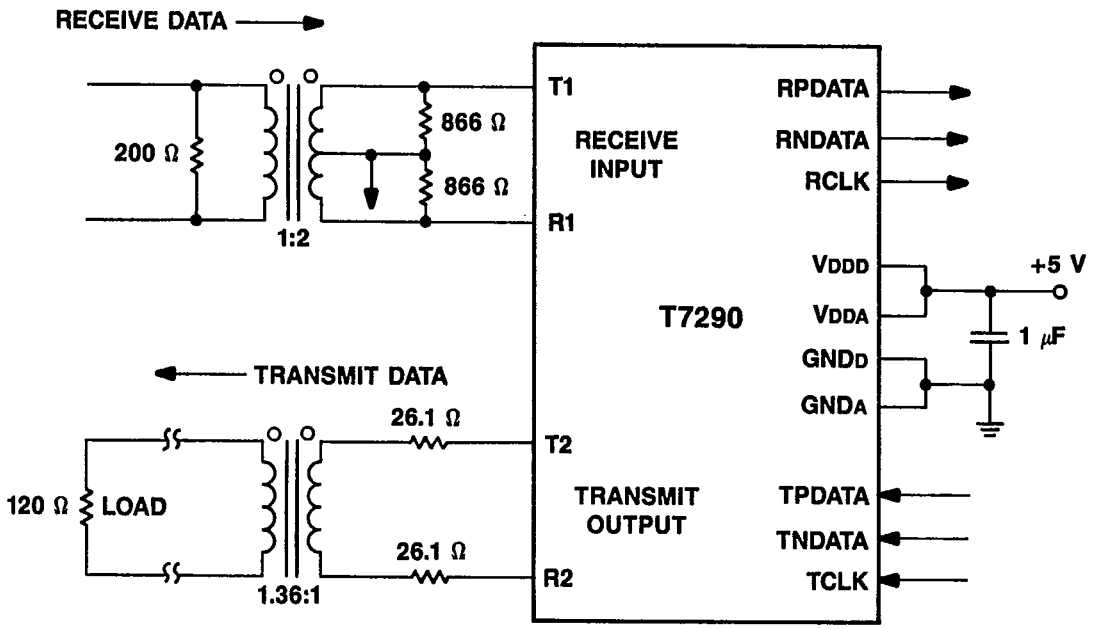
Note: Recommended transformers are the AT&T 2741 and 2745 Series.

Figure 10. DS1 Application for Twisted-Pair Interface



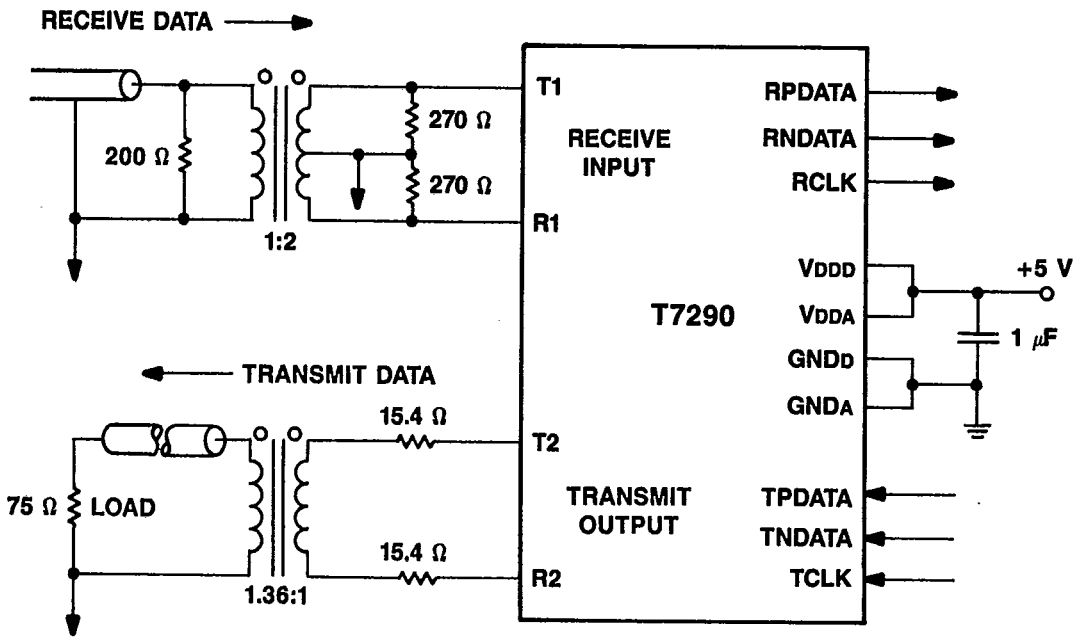
Note: Recommended transformers are the AT&T 2741 and 2745 Series.

Figure 11. T1 Application Diagram



Note: Recommended transformers are the AT&T 2741 and 2745 Series.

Figure 12. CEPT Application for Twisted-Pair Interface



Note: Recommended transformers are the AT&T 2741 and 2745 Series.

Figure 13. CEPT Application for Coaxial Interface

Characteristics

Electrical Characteristics

Operating Conditions

$-40\ °C \leq T_A \leq +85\ °C$, except as noted.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Power Dissipation* (without jitter attenuator)	PD				
T1		—	125	138	mW
DS1†		—	132	145	mW
CEPT (75 Ω)		—	126	139	mW
CEPT (120 Ω)		—	120	132	mW
(with jitter attenuator)					
T1		—	165	182	mW
DS1†		—	172	189	mW
CEPT (75 Ω)		—	174	191	mW
CEPT (120 Ω)		—	168	185	mW

* Conditions with 50% 1s on the transmit side, V_{DD} = 5 V, T_A = 25 °C.
† Equalizer settings: EC1 = 0, EC2 = 1, EC3 = 1.

Maximum Ratings

dc Supply Voltage (V_{DD}) Range ..... –0.5 V to +6.5 V
Power Dissipation (PD) ..... 1 W
Storage Temperature (T_{stg}) Range ..... –65 °C to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be soldered safely at temperatures up to 300 °C.

Table 5. Logic Interface Characteristics

An internal pull-up resistor is provided on the $\overline{TRI}$ lead. Internal pull-down devices are provided on the following leads: $\overline{CS}$, MODE1, MODE2, EC1, EC2, EC3, TBS, LOOPA, and LOOPB. The internal pull-up or pull-down devices require the input to source or sink no more than 20 μA.

$-40\ °C \leq T_A \leq +85\ °C$; $V_{DD} = 5\ V \pm 10\%$

Parameter	Symbol	Min	Max	Unit
Input Voltage:				
Low	V_{IL}	GND_D	0.8	V
High	V_{IH}	2.0	V_{DDD}	V
Output Voltage:				
Low	V_{OL}	GND_D	0.4	V
High	V_{OH}	2.4	V_{DDD}	V
Input Capacitance	C_I	—	20	pF
Load Capacitance	C_L	—	40	pF
Source Current	Isource	—	4.9	mA
Sink Current	Isink	—	4.9	mA

All duty cycle and timing relationships for receive and transmit data signals are referenced to a TTL, 1.4 V threshold level. Figure 14 shows this timing.

Table 6. Receiver Specifications

Parameter	Min	Typ	Max	Unit
Receiver Sensitivity				
DS1	0.85	—	—	Vp
CEPT	0.7	—	—	Vp
Analog LOS Level				
DS1	—	0.48	—	Vp
CEPT	—	0.28	—	Vp
PLL1*				
3 dB bandwidth	—	33	—	kHz
Peaking	—	1.2	2	dB
VCO frequency error	—	—	± 3	%
Input Density (1s)†	12.5	—	—	%
Return Loss:‡				
51 kHz – 102 kHz	12	—	—	dB
102 kHz – 2.048 MHz	18	—	—	dB
2.048 MHz – 3.072 MHz	14	—	—	dB

* Transfer characteristics (1/8 input).
† The maximum number of consecutive 0s = 15.
‡ According to *CCITT G.703/RC6367A* return loss specifications (CEPT only).

Table 7. Transmitter Specifications

Parameter	Min	Typ	Max	Unit
Output Pulse Amplitude:				
T1	2.7	3.0	3.3	V
DS1 (at DSX)	2.4	3.0	3.6	V
CEPT (into 75 Ω)	2.13	2.37	2.61	V
CEPT (into 120 Ω)	2.7	3.0	3.3	V
Output Pulse Width:				
T1	279	324	369	ns
DS1	330	350	370	ns
CEPT	219	244	269	ns
Output Power Levels:				
T1 (3 kHz band at 772 kHz)	12.0	16.5	19.0	dBm
T1 (3 kHz band at 1544 kHz)*	–25	–39	—	dB
DS1 (2 kHz band at 772 kHz)	12.6	16.5	17.9	dBm
DS1 (2 kHz band at 1544 kHz)*	–29	–39	—	dB
Positive/Negative Pulse Imbalance:				
DS1	–	–	0.5	dB
CEPT†	–	–	±5	%
CEPT Zero Level†	–	–	10	%
Return Loss:‡				
51 kHz — 102 kHz	8	—	—	dB
102 kHz — 2.048 MHz	14	—	—	dB
2.048 MHz — 3.072 MHz	10	—	—	dB

* Below the power at 772 kHz.
† Percentage of the pulse amplitude.
‡ According to *CH-PTT* return loss specifications (CEPT only).

Timing Characteristics

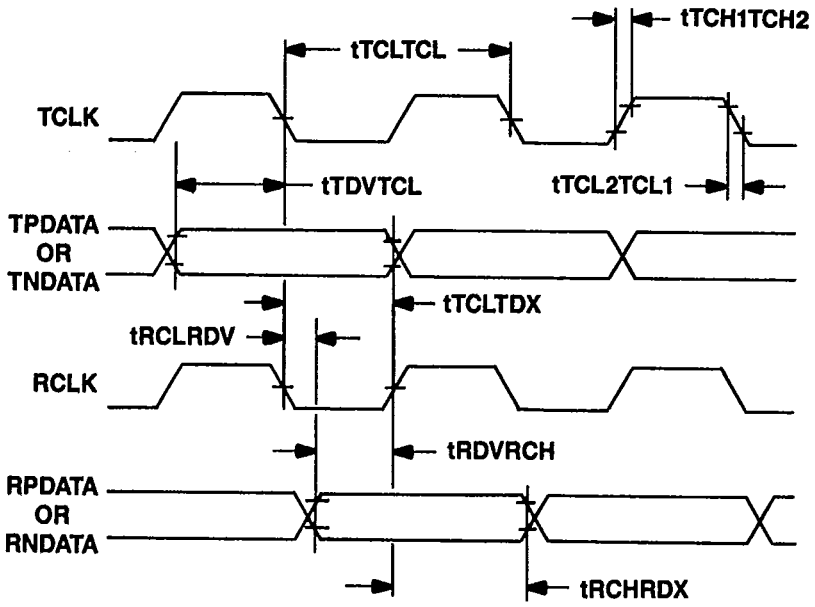


Figure 14. Interface Data Timing

Table 8. Interface Data Timing (See Figure 14.)

Symbol	Parameter	Min	Typ	Max	Unit
tTCLTCL	TCLK Clock Period: DS1/T1 CEPT	 * †	 647.7 488	 * †	 ns ns
tTDC	TCLK Duty Cycle	40	50	60	%
tTDVTCL	Transmit Data Setup Time	50	—	—	ns
tTCLTDX	Transmit Data Hold Time	40	—	—	ns
tTCH1TCH2	Clock Rise Time (10% — 90%)	—	—	40	ns
tTCL2TCL1	Clock Fall Time (10% — 90%)	—	—	40	ns
tRDVRCH	Receive Data Setup Time	140	—	—	ns
tRCHRDX	Receive Data Hold Time	180	—	—	ns
tRCLRDV	Receive Propagation Delay	—	—	40	ns

* A tolerance of ± 130 ppm.
† A tolerance of ± 50 ppm.

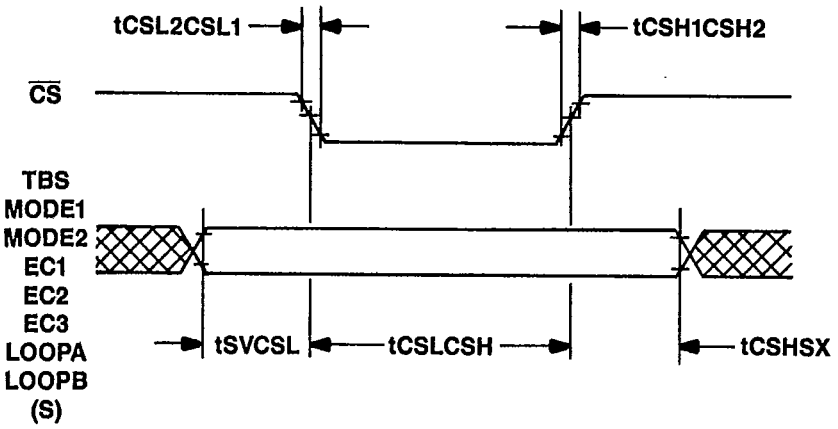


Figure 15. Microprocessor Interface Timing

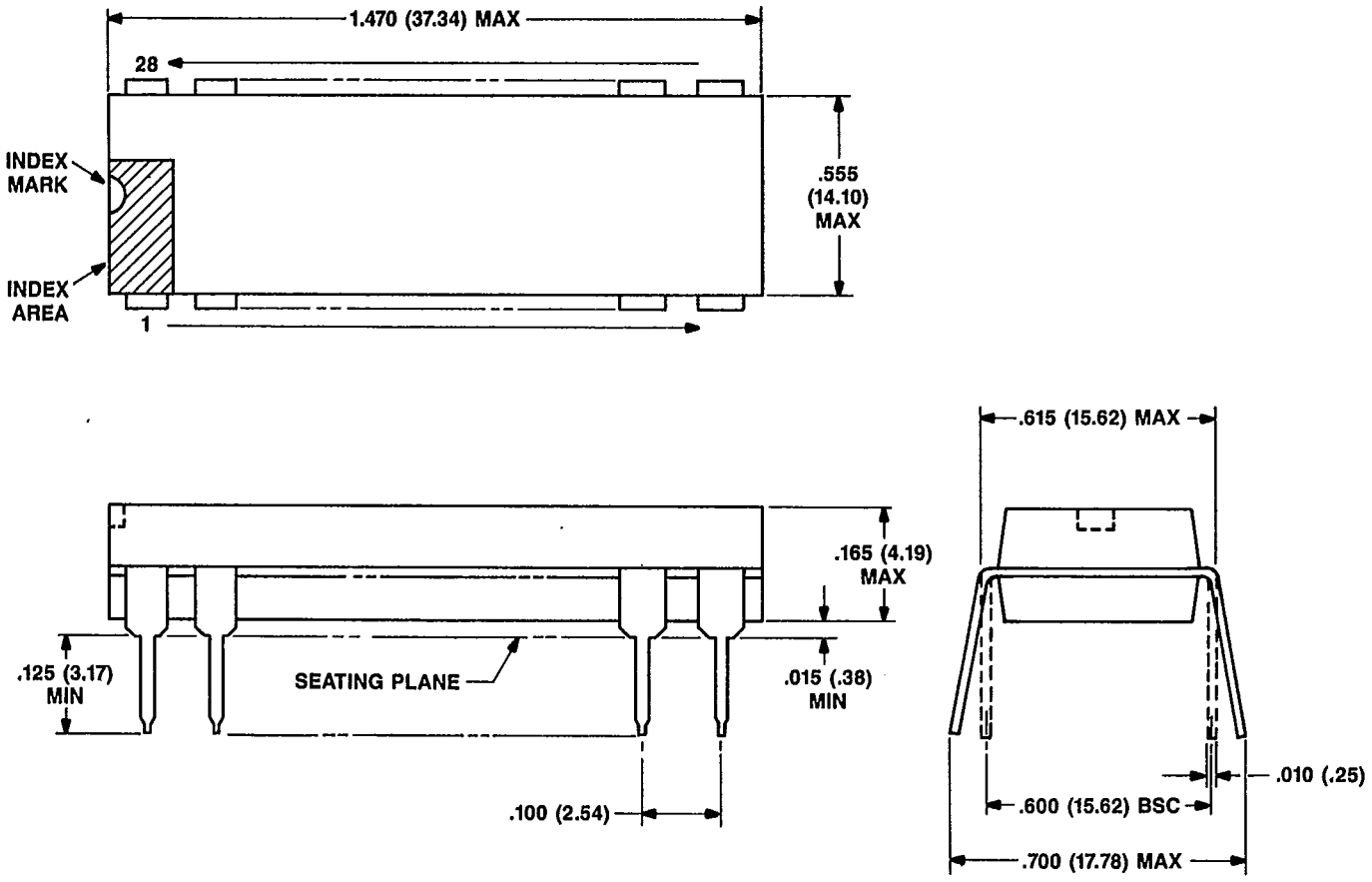
Table 9. Microprocessor Interface Timing (See Figure 15.)

Symbol	Parameter	Min	Max	Unit
tSVCSL	Control Signal Setup Time	50	—	ns
tCSLCSH	Control Signal Pulse Width Time	40	—	ns
tCSHSX	Control Signal Hold Time	40	—	ns
tCSH1CSH2	Control Signal Rise Time (10% — 90%)	—	40	ns
tCSL2CSL1	Control Signal Rise Time (10% — 90%)	—	40	ns

Outline Diagrams

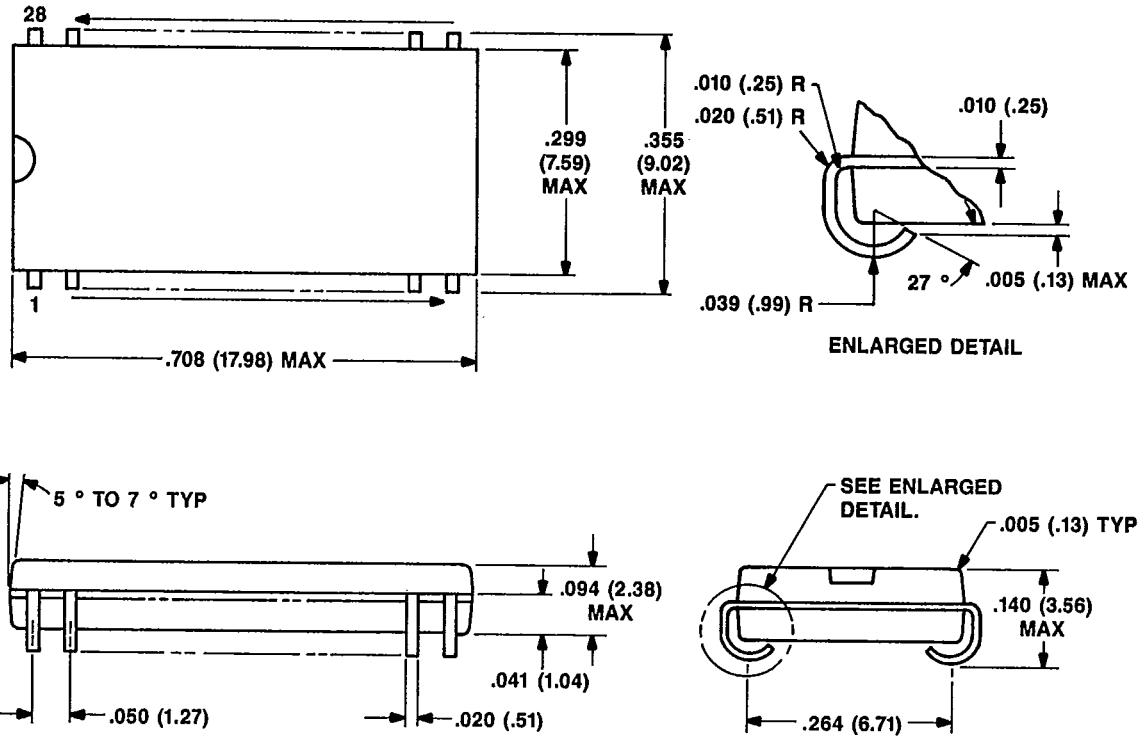
28-Pin, Plastic DIP

All dimensions are in inches and (millimeters).



28-Pin, Plastic SOJ

All dimensions are in inches and (millimeters).



Ordering Information

Code	Package	Temperature
T7290-PL	28-Pin, Plastic DIP	−40 °C to +85 °C
T7290-EL	28-Pin, Plastic SOJ	−40 °C to +85 °C