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ECL Products	

100175

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FEATURES

- **Typical propagation delay from D_n to Q_n: 2.2ns**
- **Typical propagation delay from $\overline{E}_n$ to Q_n: 2.7ns**
- **Typical supply current ($-I_{EE}$): 67mA**

DESCRIPTION

The 100175 is composed of five latches, each with one data input and one data output. A Master Reset input (MR) and two Enable inputs ($\overline{E}_0$, $\overline{E}_1$) preside over all the latches. A Q_n output follows its D_n input when both $\overline{E}_0$ and $\overline{E}_1$ are Low. When either $\overline{E}_0$ or $\overline{E}_1$ (or both) go High, the latches store the last valid data present on their D_n inputs. The MR input forces the Q_n outputs Low if either $\overline{E}_0$ or $\overline{E}_1$ (or both) are High. The inputs are 100K compatible and the outputs are 10K compatible.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

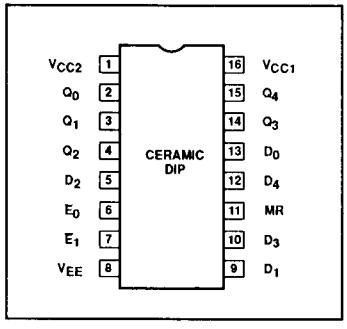
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_4$	Data inputs (100K ECL compatible)
MR	Master reset input (100K ECL compatible)
$\overline{E}_0$, $\overline{E}_1$	Enable input (100K ECL compatible)
$Q_0 - Q_4$	Data outputs (10K ECL compatible)

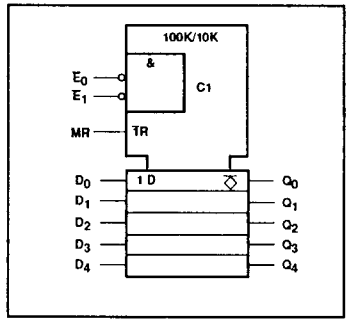
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Ceramic DIP (300 mils wide)	100175F

PIN CONFIGURATION



IEC/IEEE



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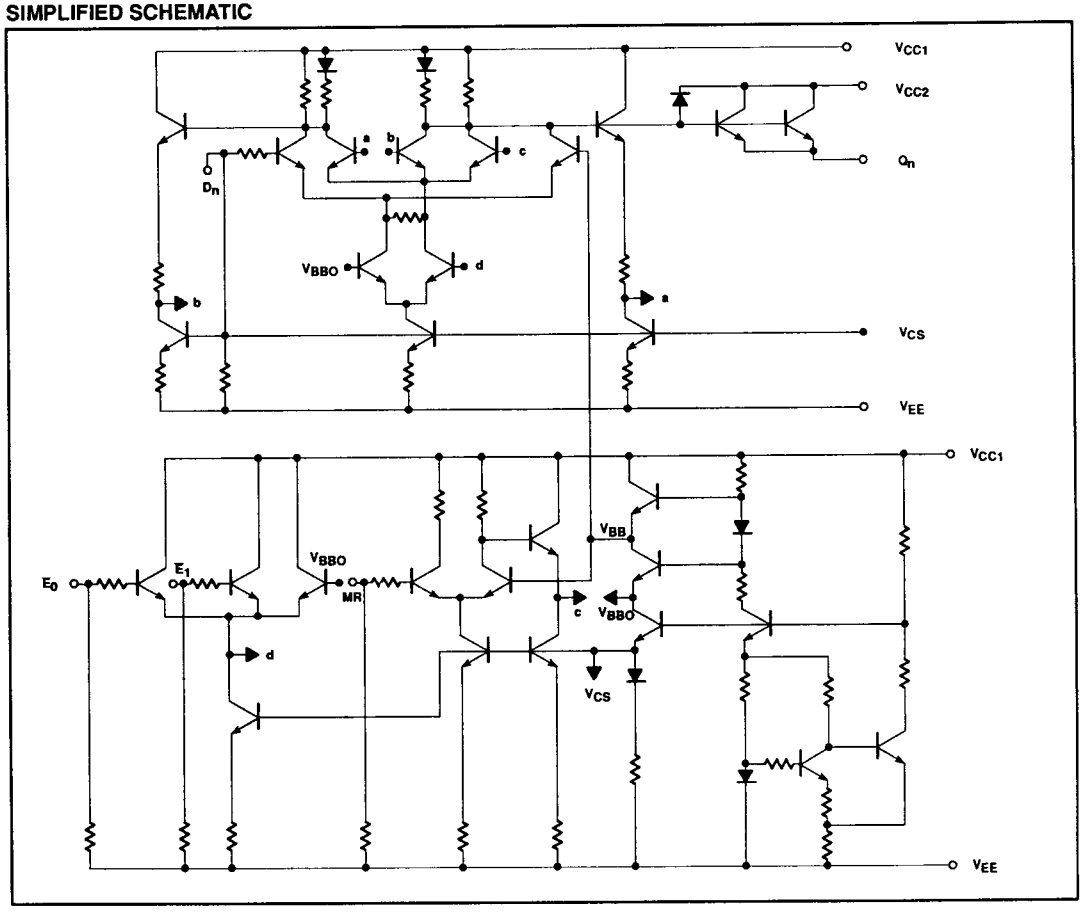
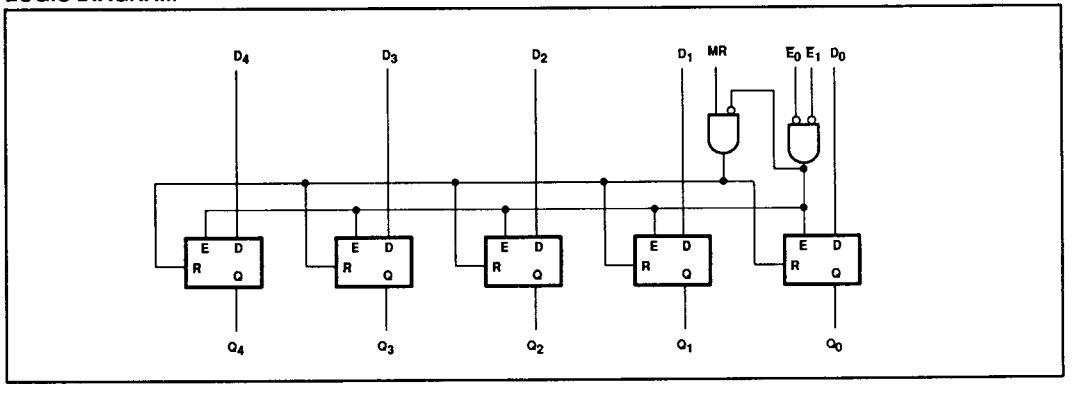
SIMPLIFIED SCHEMATIC



LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS				OUTPUT
D_n	E_0	E_1	MR	Q_n
H	L	L	X	H
L	L	L	X	L
X	H	X	L	NC
X	X	H	L	NC
X	H	X	H	L
X	X	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
NC = No change

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–5.7	–5.2		V
V_{IH}	High level input voltage	V_{EE} = –5.2V ± 0.010V	–1165		–880	mV
V_{IL}	Low level input voltage	V_{EE} = –5.2V ± 0.010V	–1810		–1475	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

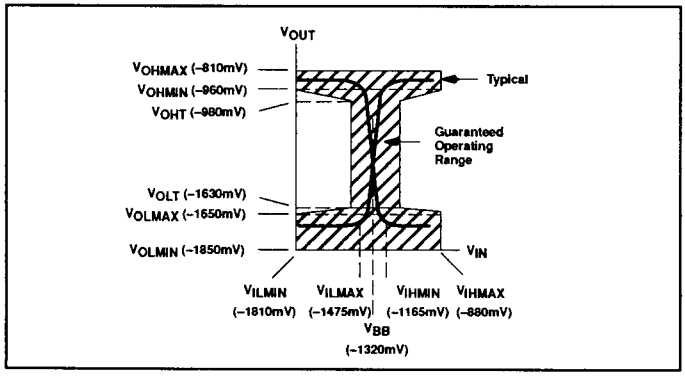
$V_{CC1} = V_{CC2}$ =ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to −2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$	−1000		−840	mV
					$T_A = +25°C$	−960		−810	mV
					$T_A = +85°C$	−890		−700	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$	−1020			mV
					$T_A = +25°C$	−980			mV
					$T_A = +85°C$	−910			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$			−1645	mV
					$T_A = +25°C$			−1630	mV
					$T_A = +85°C$			−1595	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$	−1870		−1665	mV
					$T_A = +25°C$	−1850		−1650	mV
					$T_A = +85°C$	−1825		−1615	mV
I_{IH}	High level input current	MR input	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					650	µA
		All others						290	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			50	67	102	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$V_{EE} = -4.68V$, $T_A = +25°C$				0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation						0.250		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

TRANSFER CHARACTERISTIC



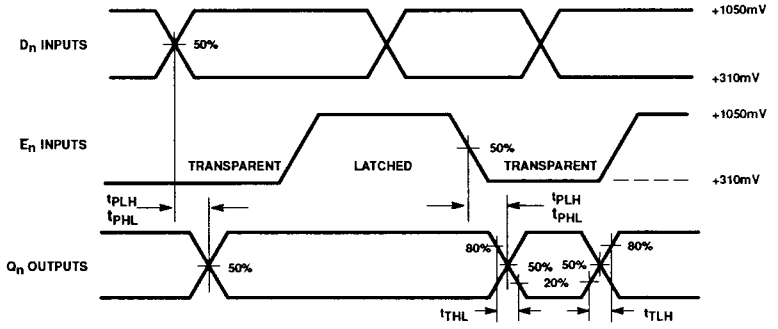
AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 0.010V$

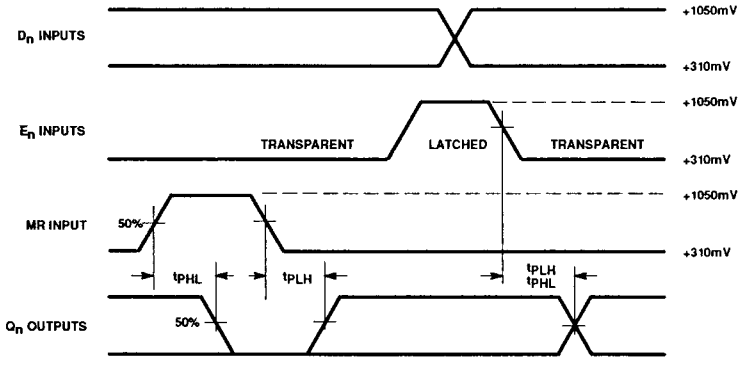
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	3.40 3.40	1.00 1.00	3.40 3.40	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n		1.00 1.00	4.30 4.30	1.00 1.00	4.30 4.30	1.00 1.00	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n	Waveform 2	1.00 1.00	3.90 3.90	1.00 1.00	3.90 3.90	1.00 1.00	3.90 3.90	ns ns
t_{TLH} t_{THL}	Transition time Q_n	Waveform 1	0.90 0.90	3.50 3.50	1.00 1.00	3.50 3.50	0.90 0.90	3.50 3.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	2.5		2.5		2.5		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.5		0.5		0.5		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

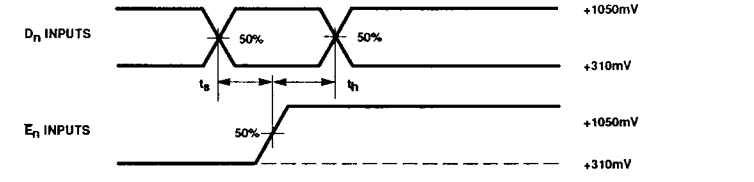
AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset Timing



Waveform 3. Data Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

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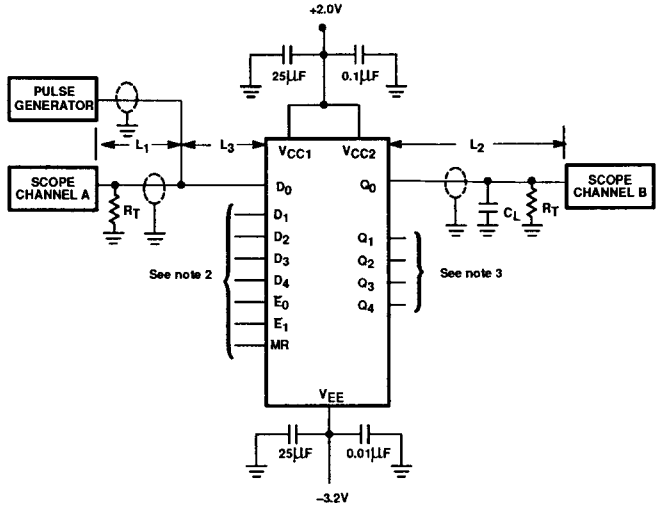
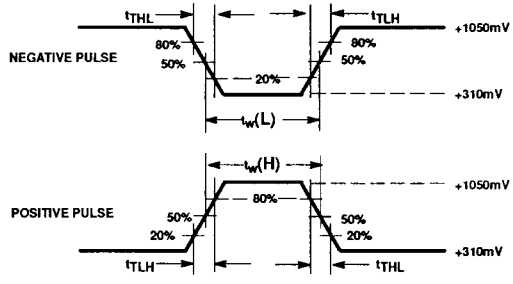
AC TEST CIRCUIT



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	740mV$_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.