

Features

- Low start-up power supply voltage :1.4V(CH5)
- Wide supply voltage range from 2.5V to 7V (CH1~5)
- High speed operation is possible: Maximum 1 MHz
- Supports for up,down, flyback and up/down SEPIC conversion
- Supports for inverting conversion (CH4)
- Synchronized rectification on CH1,CH2
- Selectable P-Ch/N-CH MOSFETdriver
- Built-in On/Off function
- Built-in Short-Circuit Protection.

Applications

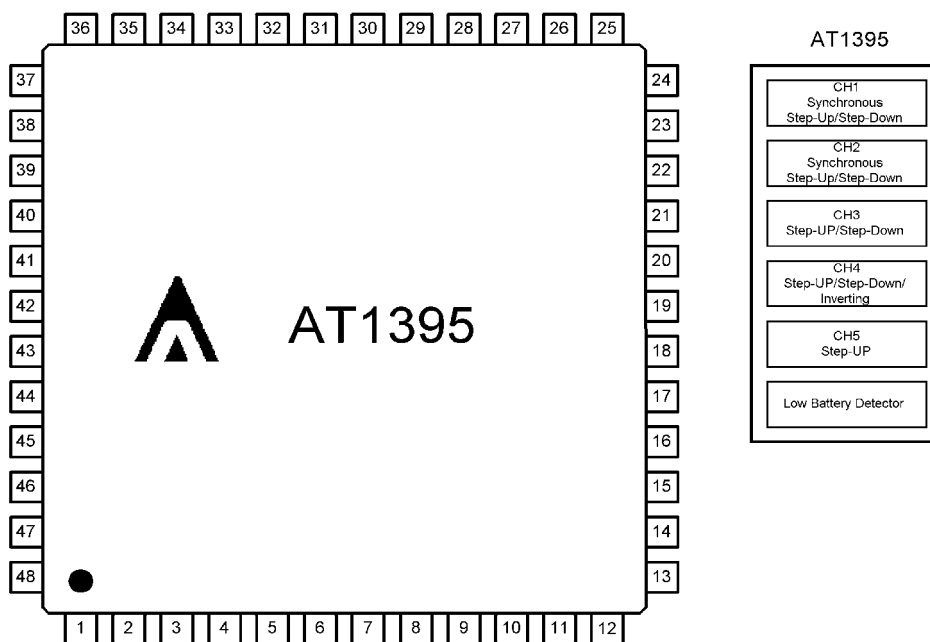
- Digital Cameras
- CCD Imaging Devices
- Camcorders

General Description

The AT1395 is a 5-channel PWM DC/DC control IC for low voltage applications with a soft start function and short circuit detection function. This IC is ideal for up conversion, down conversion, inverting conversion (CH4 only) and up/down conversion (using a step-up/step-down SEPIC or Zeta system with free input and output settings). 5 channels can be built in the LQFP48 package, each channel be controlled, and soft-start.

The AT1395 include one comparator to generate low-battery warning outputs. It also contains two high efficiency topology by using synchronous rectification PWM (It can be disable by floating OUT1_2,OUT2_2.)

Pin Assignment



Ordering Information

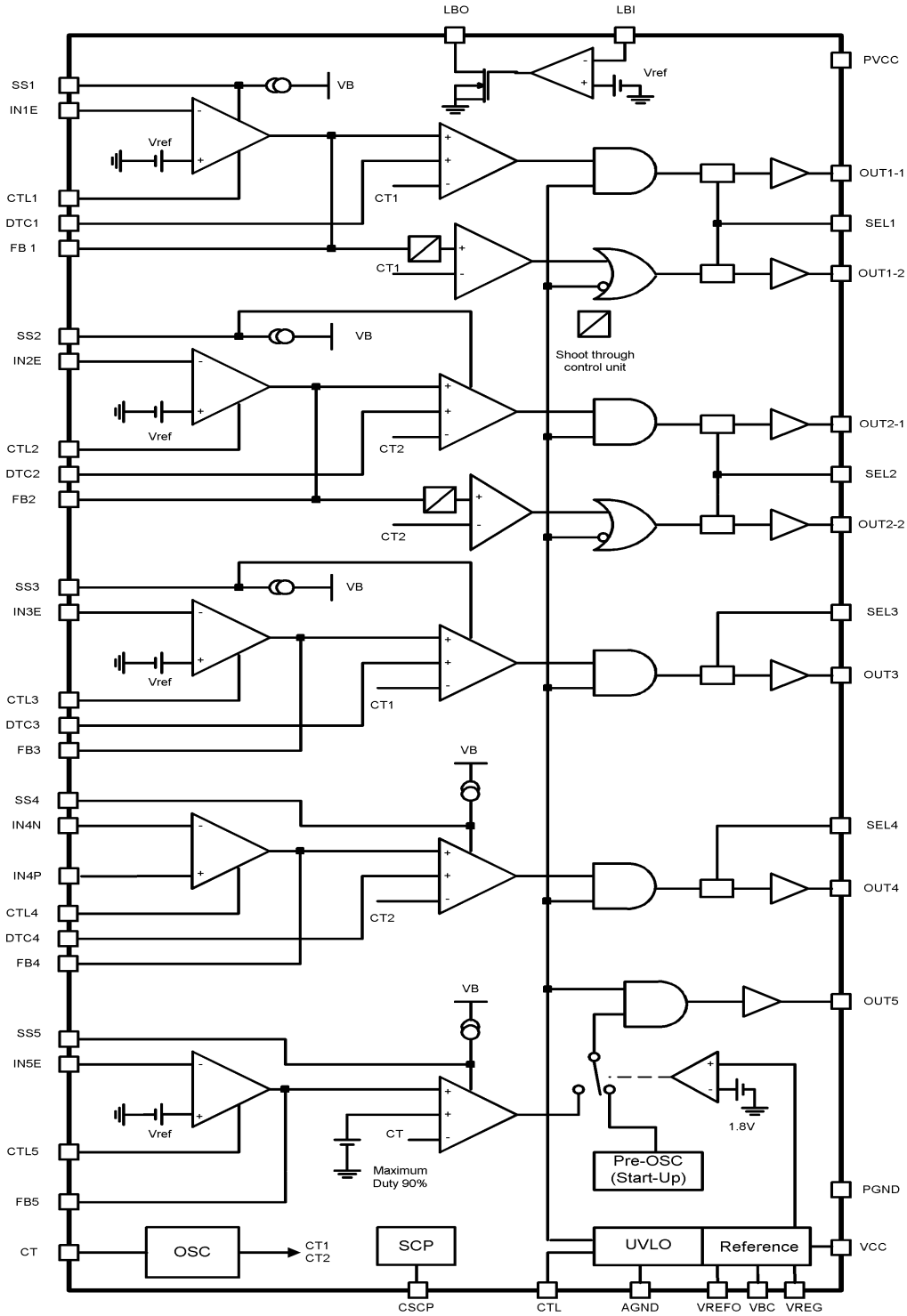
Part number	Package	Marking
AT1395F	LQFP48	AT1395F

Aimtron reserves the right without notice to change this circuitry and specifications.

Pin Description

Pin No.	Pin name	I/O	Function
1	SS5	I	CH5 Soft Start Setting Capacitor
2	FB5	I	CH5 Error Amplifier Output
3	IN5E	I	CH5 Error Amplifier Inverted Input
4	SEL4	I	CH4 Output Driver P-ch/N-ch Control
5	DTC4	I	CH4 Dead Time Control
6	SS4	I	CH4 Soft Start Setting Capacitor
7	FB4	I	CH4 Error Amplifier Output
8	IN4N	I	CH4 Error Amplifier Negative Input
9	IN4P	I	CH4 Error Amplifier Positive Input
10	SEL3	I	CH3 Output Driver P-ch/N-ch Control
11	DTC3	I	CH3 Dead Time Control
12	SS3	I	CH3 Soft Start Setting Capacitor
13	FB3	I	CH3 Error Amplifier Output
14	IN3E	I	CH3 Error Amplifier Inverted Input
15	CTL5	I	CH5 ON/OFF Control Input
16	CTL4	I	CH4 ON/OFF Control Input
17	CTL3	I	CH3 ON/OFF Control Input
18	VREG	O	2.2V Regulator Output
19	VREFO	-	Reference bypass Input
20	AGND	P	Power Ground
21	VCC	P	Power Supply
22	VBC	-	Bias bypass Input
23	CT	-	Oscillation Frequency Setting Capacitor
24	CTL	I	Power Control Input
25	CSCP	-	Timer Latch Short-Circuit Detection Capacitor Input
26	CTL2	I	CH2 ON/OFF Control Input
27	CTL1	I	CH1 ON/OFF Control Input
28	IN2E	I	CH2 Error Amplifier Inverted Input
29	FB2	I	CH2 Error Amplifier Output
30	SS2	I	CH2 Soft Start Setting Capacitor
31	DTC2	I	CH2 Dead Time Control
32	SEL2	I	CH2 Output Driver P-ch/N-ch Control
33	IN1E	I	CH1 Error Amplifier Inverted Input
34	FB1	I	CH1 Error Amplifier Output
35	SS1	I	CH1 Soft Start Setting Capacitor
36	DTC1	I	CH1 Dead Time Control
37	SEL1	I	CH1 Output Driver P-ch/N-ch Control
38	LBI	I	Low Battery Detector Input
39	LBO	O	Low Battery Indicator
40	OUT1_1	O	CH1 Main Side Output
41	OUT1_2	O	CH1 Synchronous Rectifier Side Output
42	OUT2_1	O	CH2 Main Side Output
43	OUT2_2	O	CH2 Synchronous Rectifier Side Output
44	PVCC	P	Drive Output Block Power Supply
45	PGND	P	Drive Output Block Ground
46	OUT3	O	CH3 Output
47	OUT4	O	CH4 Output
48	OUT5	O	CH5 Output

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V _{CC}	--	--	7	V
Output current	I _O	Output pin	--	20	mA
Output peak current	I _O	Output pin, Duty ≤ 5%	--	200	mA
Power dissipation	P _D	T _a ≤ 25°C (LQFP-48P)	--	860	mW
Operation temperature	T _{opr}	--	-30	85	°C
Storage temperature	T _{stg}	--	-55	125	°C

*Semiconductor devices can be permanently damaged by application of stress in excess of absolute ratings. Do not exceed these ratings.

Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
			Startup power supply voltage	V _{CC1}	CH5	
Power supply voltage	V _{CC2}	CH1 to CH4	2.5	3.3	6.5	V
Regulator voltage output current	I _{OR}	VREG pin	-10	--	0	mA
Input voltage	V _{IN}	IN1E to IN5E pins	0	--	V _{CC} -1.8	V
Control input voltage	V _{CTL}	CTL pin	0	--	7	V
Output current	I _O	OUT pin (CH1 to CH4)	--	2	15	mA
		OUT pin (CH5)	1	2	15	mA
Oscillator	f _{OSC}	--	100	500	1000	kHz
Timing capacitor	C _T	--	47	100	560	pF
Soft start capacitor	C _S	CH1 to CH4	--	0.1	1.0	μF
	C _{SS6}	CH5	--	0.1	1.0	μF
Short detection capacitor	C _{CSCP}	--	--	0.1	1.0	μF
VREG pin capacitor	C _{VREG}	--	0.082	0.1	--	μF
Operating ambient temperature	T _A	--	-30	25	85	°C

Electrical Characteristics

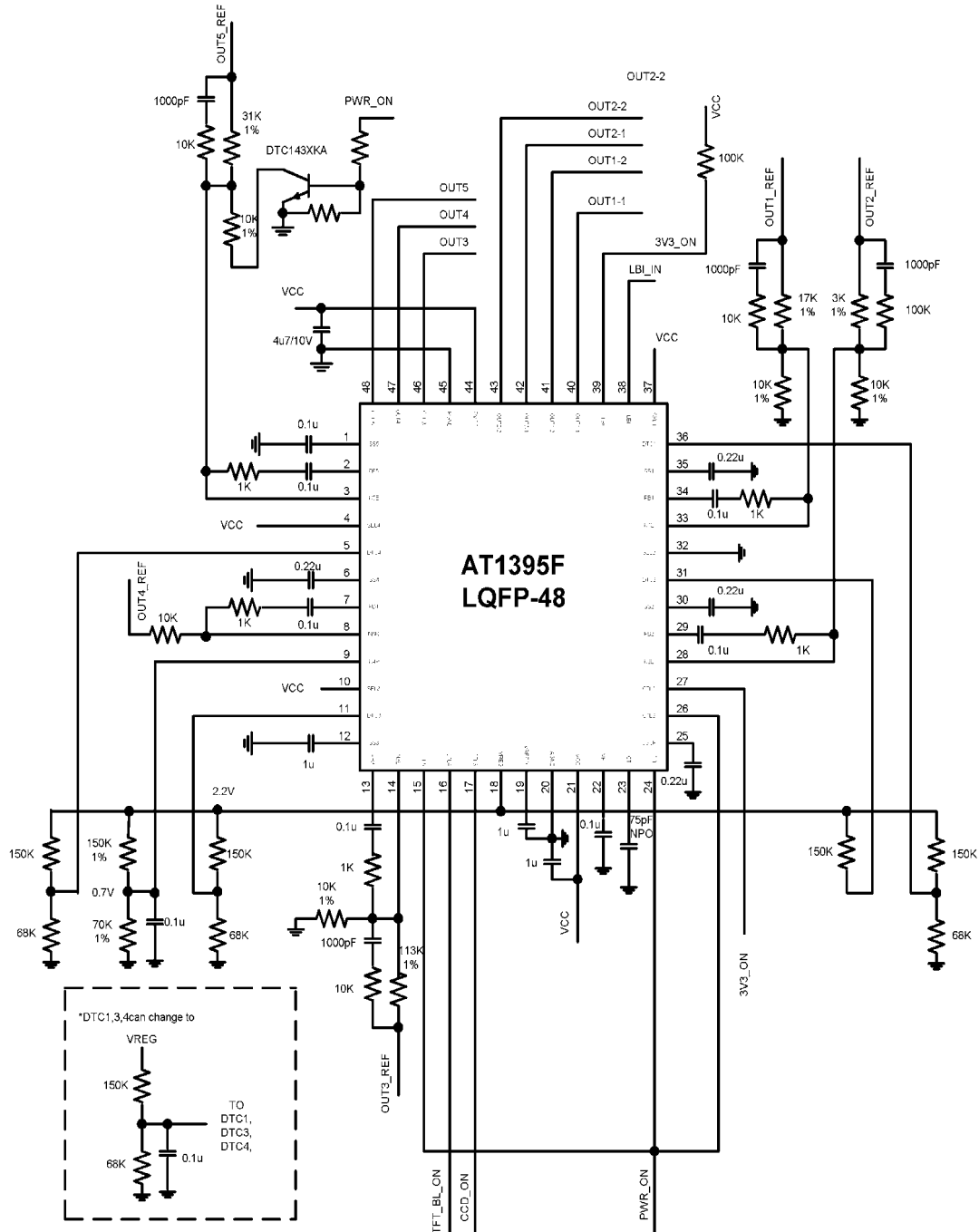
(T_A=25°C, VCC=PVCC=5V)

Parameter	Symbol	Condition	Measure result			Unit
			Min.	Typ.	Max.	
Reference voltage block [REF]						
Regulator voltage	V _{REG}		2.15	2.2	2.25	V
Output voltage temperature stability	$\frac{\Delta V_{REG}}{V_{REG}}$	T _A = -30°C to 85°C	-	0.5	-	%
Input stability	Line	VCC=2.5V to 7V	-10	-	10	mV
Load stability	Load	VREG=0mA to -1mA	-10	-	10	mV
Under voltage lockout block [U.V.L.O]						
Threshold voltage(CH1~CH4)	V _{TH}		2.0	2.2	2.4	V
Hysteresis width(CH1~CH4)	V _H		0.05	0.1	0.3	V
Reset voltage(CH1~CH4)	V _{RST}		-	-	2.5	V
CH5 Pre-OSC change to Main-OSC threshold	V _{TH}		-	1.8	-	V
Pre-OSC frequency(CH6)	f _{Pre-OSC}		320	400	450	KHz
Soft start block [CS]						
Charge current	I _{CS}		-3.0	-2.5	-2.0	μA
Short circuit detection block [SCP]						
Threshold voltage	V _{TH}		0.65	0.70	0.75	V
Input standby voltage	V _{STB}		-	50	100	mV
Input latch voltage	V _I		-	50	100	mV
Input source current	I _{CSCP}		-1.4	-1.0	-0.6	μA
Triangular wave oscillator block [OSC]						
Oscillator frequency	f _{OSC}	CT=75pF	450	500	550	KHz
Frequency stability for voltage	$\frac{\Delta f}{fdv}$	VCC=2.5V to 7V	-	1	10	%
Frequency stability for temperature	$\frac{\Delta f}{fdt}$	T _A =-30°C to 85°C	-	1	20	%
CH5 Maximum Duty	DUTY		80	90	-	%
Error amplifier block [Error Amp](CH1~CH5)						
Threshold voltage	V _{REF}	FB=1.22V	1.20	1.22	1.24	V

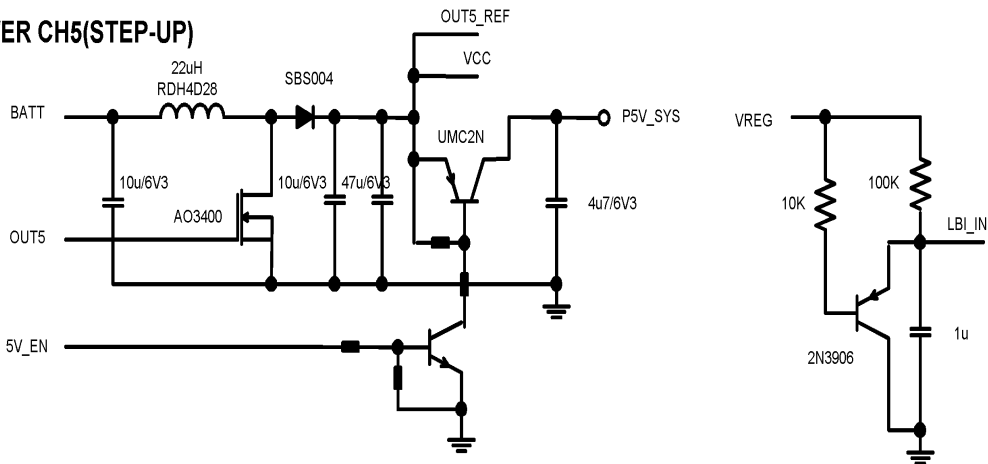
V _T temperature stability	$\Delta V_T/V_T$	T _A = -30°C to 85°C	-	0.5	-	%
Input bias current	I _B	IN=0V	-320	-80	-	nA
Voltage gain	A _V	DC	-	100	-	dB
Frequency bandwidth	BW	A _V =0dB	-	10	-	MHz
Output voltage	V _{OH}		1.3	1.5	-	V
	V _{OL}		-	20	200	mV
Output source current	I _{SOURCE}	FB=0.5V	-	-2.0	-1.0	mA
Output sink current	I _{SINK}	FB=0.5V	70	120	-	μA
Short detect comparator [SCP Comp]						
Threshold voltage	V _{TH}	CH1 to CH4	0.9	1.0	1.1	V
Threshold voltage	V _{TH}	CH5	0.8	0.9	1.0	V
Input bias current	I _B	IN=0V	-320	-80	-	nA
PWM Comp. [PWM Comp]						
Threshold voltage(CH1~6)	V _{T0}	Duty = 0 %	0.25	0.3	-	V
	V _{Tmax}	Duty = 100 %	-	0.80	0.85	V
Input current	I _{DTC}	DTC=0.5V	-1.0	-0.3	-	μA
Output block (CH1 to CH4) [Pin 40,42,46,47]						
Output source current	I _{SOURCE}	OUT=VCC/2	-	-130	-80	mA
Output sink current	I _{SINK}	OUT=VCC/2	65	100	-	mA
Output ON resistor	R _{OH}	OUT = -15mA	-	18	30	Ω
	R _{OL}	OUT = 15mA	-	16	25	Ω
Output block (CH1,2) [Pin 41,43]						
Output source current	I _{SOURCE}	OUT=VCC/2	-	-130	-80	mA
Output sink current	I _{SINK}	OUT=VCC/2	65	100	-	mA
Output ON resistor	R _{OH}	OUT = -15mA	-	18	30	Ω
	R _{OL}	OUT = 15mA	-	16	25	Ω
Output block (CH5) [Pin 48]						
Output source current	I _{SOURCE}	Duty=90%, OUT=VCC/2	-	-260	-160	mA
Output sink current	I _{SINK}	Duty ≤ 5%, OUT=VCC/2	150	260	-	mA
Output ON resistor	R _{OH}	OUT = -15mA	-	9	15	Ω
	R _{OL}	OUT = 15mA	-	9	15	Ω
Control block [CTL]						
CTL input voltage	V _{IH}	Active mode	1.3	-	7	V
	V _{IL}	Standby mode	0	-	0.8	V

CTL1 to CTL5 input voltage	V_{IH}	Active mode	1.3	-	7	V
	V_{IL}	Standby mode	0	-	0.8	V
Input current	I_{CTL}	CTL = 5V	-	5	20	μA
SEL block [CTL]						
SEL1 to SEL4 input voltage	V_{IH}	N-CH Drive	VCC/2	-	7	V
	V_{IL}	P-CH Drive	0	-	0.8	V
Low battery detect block [LBI, LBO]						
LBI detect threshold			1.20	1.22	1.24	V
Detect Hysteresis			-50		+50	mV
LBO output voltage low		Isink=1mA	-	-	0.4	V
LBO output high leakage		VLBO=5V	-	0.01	1	μA
General						
Standby current	I_{css}	CTL=CTL1=CTL2=CTL3=CTL4=CTL5=0V	-	1	10	μA
	$I_{css(o)}$	CTL=0V, CTL1=CTL2=CTL3=CTL4=CTL5="H"	-	200	250	μA
Power supply current	I_{cc}	CTL=CTL1=CTL2=CTL3=CTL4=CTL5="H"	-	3	7	mA

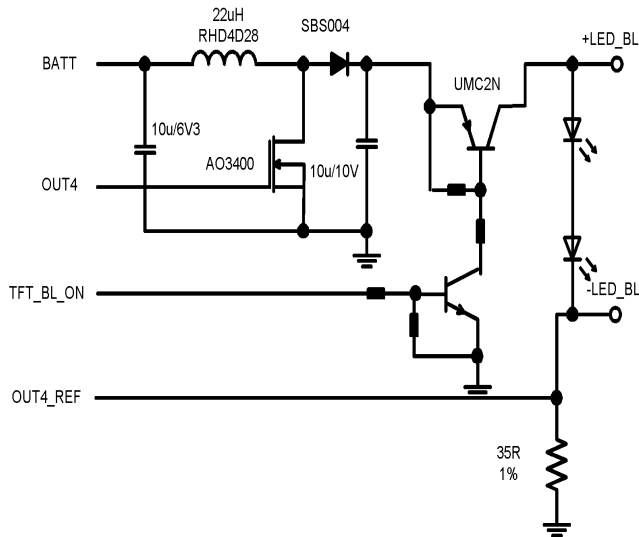
Application Circuit



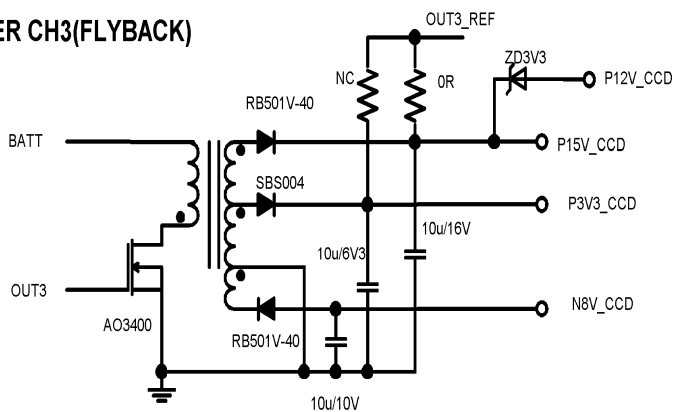
POWER CH5(STEP-UP)



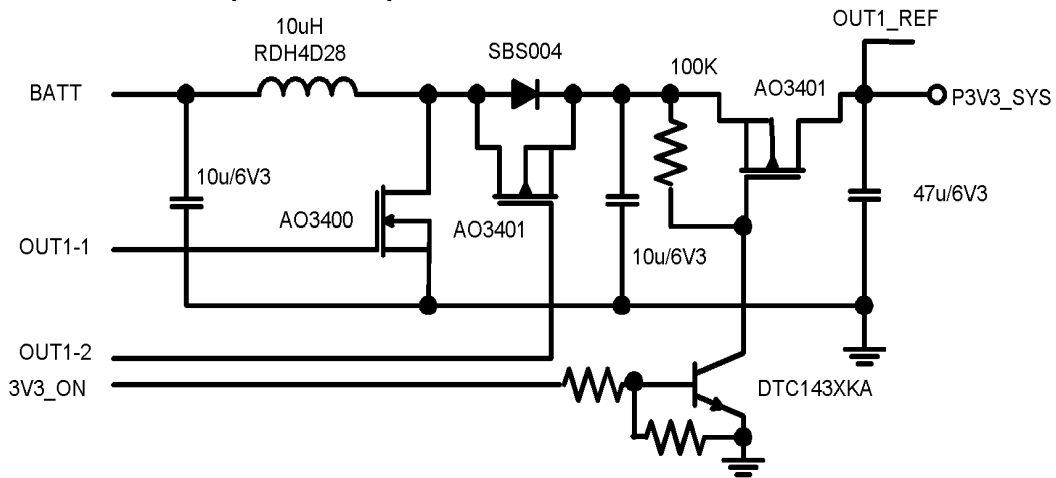
POWER CH4(STEP-UP)



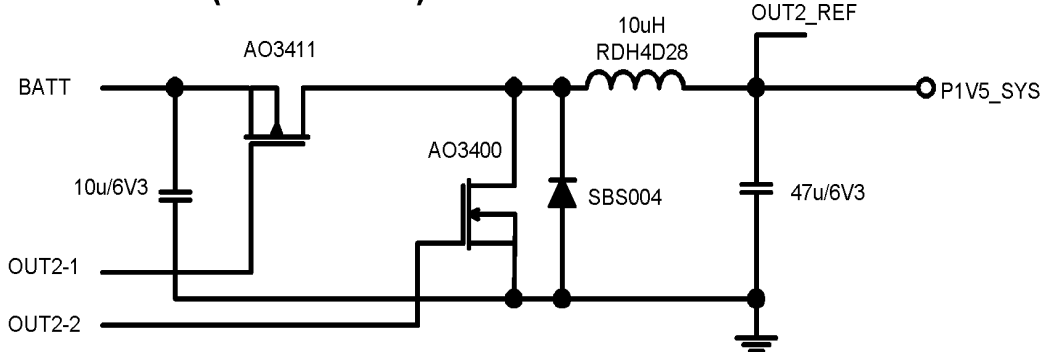
POWER CH3 (FLYBACK)



POWER CH1(STEP-UP)



POWER CH2(STEP-Down)



Function Description

1. Power Converter Functions

* Reference voltage block

The reference voltage circuit generates a temperature independence voltage (typical=2.2V) from the power source, which is used as reference voltage for the IC's internal circuitry and supply load current above 10mA to external device.

* Triangular oscillator block

The triangular wave oscillator is generated by timing capacitor(CT) to incorporate each other. The waveforms CT (amplitude of 0.3V to 0.8V), CT1 (amplitude 0.3V to 0.8V in phase with CT) and CT2 (amplitude 0.3V to 0.8V in inverse phase with CT) are input to the PWM comparator.

* Error amplifier block

The error amplifier outputs controlling error signal to PWM comparator from sensing DC/DC converter output voltage. In addition, an arbitrary loop gain can be set by connecting feedback resistor and capacitor from the output pin to inverted input pin of the error amplifier, in order to make a stable system.

* CH4 Inverting amplifier block

The inverting amplifier detects the DC/DC converter output voltage (negative) and outputs a control signal to the error amplifier.

* PWM comparator block

The PWM comparator is a voltage-to-pulse width converter for controlling the duty cycle of DC/DC converter.

Channels 1, 2 main sides, channel 3, 4, and 5: The comparator keeps the output transistor turn on while the error amplifier output voltage and DTC voltage still higher than the triangular wave voltage.

Channels 1, 2 synchronous rectification sides : The comparator keeps the output transistor turn on while the error amplifier output voltage still lower than the triangular wave voltage.

* Output block

The output block is the totem pole configuration, which could drive external MOSFET or transistor. It can be drive the external N-MOSFET by force the SEL to High, and it can be drive the external P-MOSFET by force the SEL to LOW.

2. Channel Control Function

The channels are turned on and turned off depending on the voltage levels at the CTL, CTL12, CTL3, CTL4, CTL5, and CTL6. Described as follow.

CTL	L	H				
CTL1	X	H	Z	Z	Z	Z
CTL2	X	Z	H	Z	Z	Z
CTL3	X	Z	Z	H	Z	Z
CTL4	X	Z	Z	Z	H	Z
CTL5	X	Z	Z	Z	Z	H
CH1	OFF	ON	OFF	OFF	OFF	OFF
CH2		OFF	ON	OFF	OFF	OFF
CH3		OFF	OFF	ON	OFF	OFF
CH4		OFF	OFF	OFF	ON	OFF
CH5		OFF	OFF	OFF	OFF	ON

X : Don't care Z: Low or Floating

3. Protective Functions

* Short circuit protection and timer latch

The short circuit detection comparator in each channel detects the output voltage level of power converter. When the output voltage falls below the short detection level, there is a constant current bias charging the external capacitor C_{CSCP} which connected to the CSCP pin until the capacitor voltage level reaches about 0.7V then disable the IC. It could reset the actuated protection by restart the power source or pull CTL from low to high.

* Under-voltage lockout protection

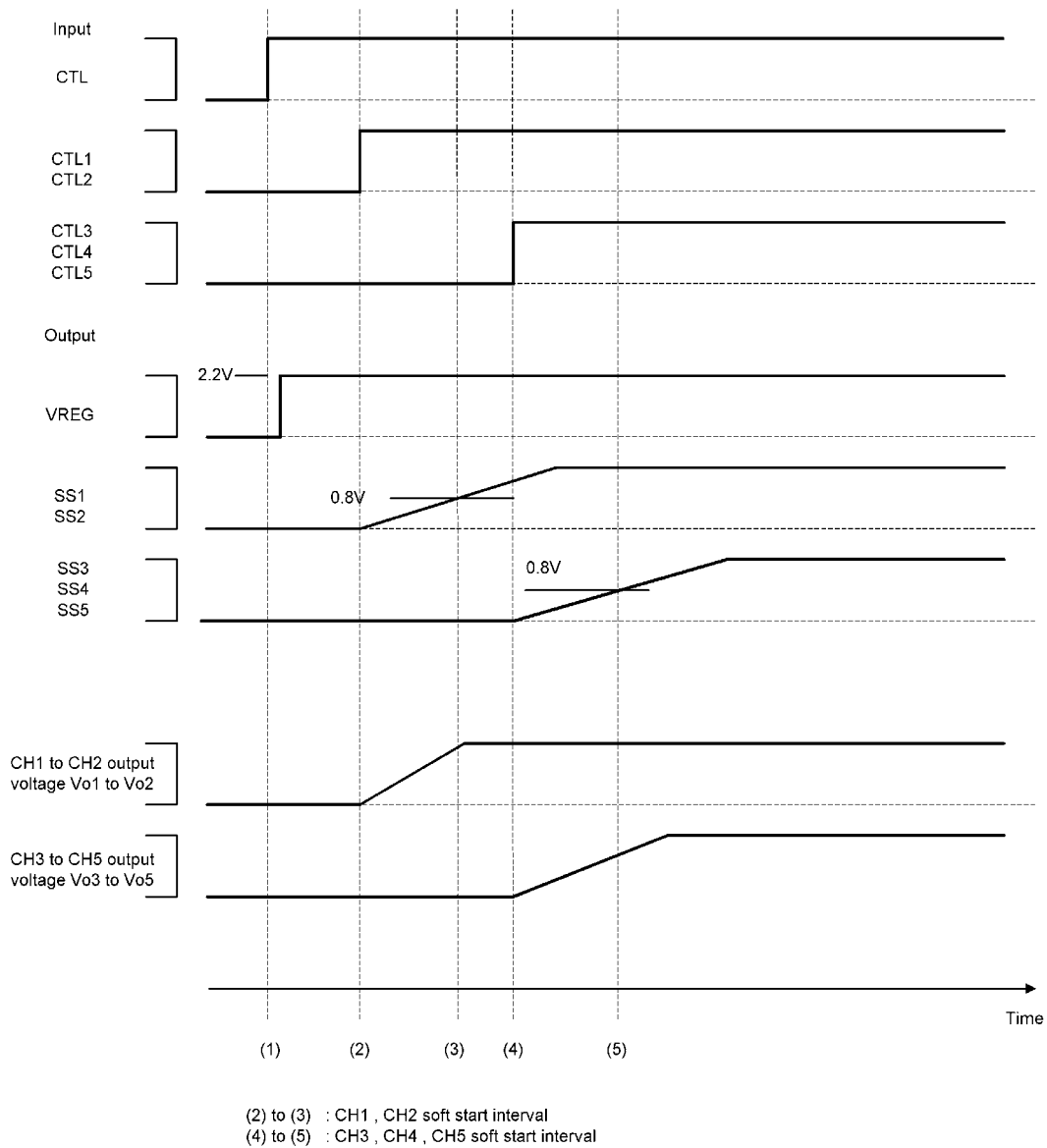
The under-voltage lockout protection is to disable the IC while the supply voltage transient or momentary decrease, which may cause the IC to malfunction. To prevent such malfunctions, the under-voltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and holding the CSCP pin at the “L” level.

* Battery Low Detect Function

The Battery low comparator open-drain output LBO sinks up to 1mA if the LBI input is below its threshold voltage. Connect LBO to power source with a 100K Ω ~1M Ω pull-up resistor.

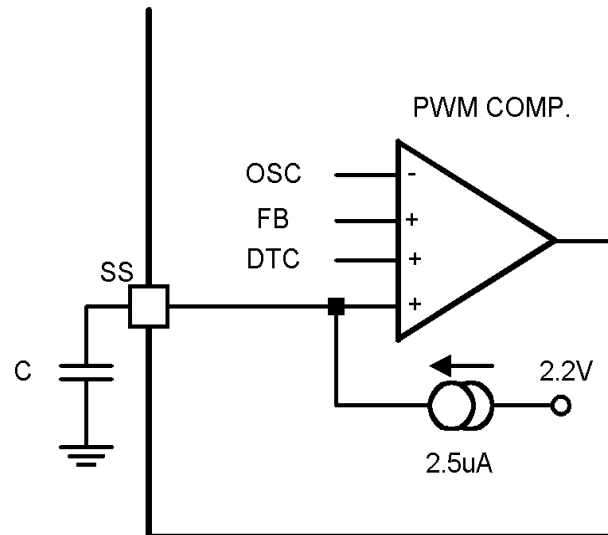
4. Soft Start Operation

* After CTL ON, driving the CTL1, CTL2, CTL3, CTL4 and CTL5 to high level.
 The driving scheme is described as follow diagram.



* Soft start setting (CH1~5)

Consider the input voltage and load current to design the capacitor connected to the SS pin.



It can calculate the CH1~5 soft start time $T_s(s)$.

$$C \times \frac{\Delta V}{\Delta t} = I$$

$$T_s(s) = 0.2 \times C(\mu F)$$

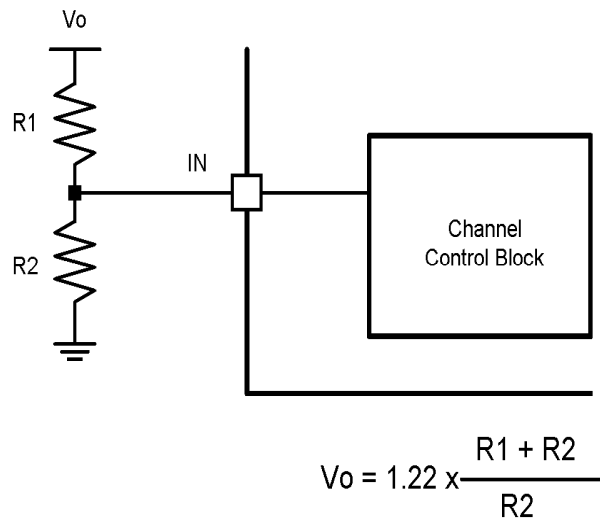
Note : It could be disabled soft start function by floating SS pin.

Determine the triangular Oscillator Frequency

The triangular oscillator frequency is determined by the timing capacitor (C_T). It is difficult to incorporate these non-linear characteristics into the equation. This difference is caused by characteristics, such as changes in the maximum voltage amplitude of the sawtooth waveform with the C_T value and the circuit delay causing the maximum amplitude to become large in the case of a high oscillating frequency even for the same capacitor. In practical use, therefore, the user should read the C_T values from the characteristic curve or should determine an approximate target value by using the equation.

Design the DC/DC Output Voltage

*CH1~5



Setting Time Period When Short Circuit Protection

The CSCP comparator detects each channel output voltage while the power converter work at normal condition. At the same time, the voltage level of CSCP pin is held at low level. If the output load of these converters rapidly malfunction or short, causing the output voltage to drop, the CSCP comparator detects that to enable short circuit protection. The time period when short circuit protection show as follow equation.

Short detection time ($T_{PE}(s)$)

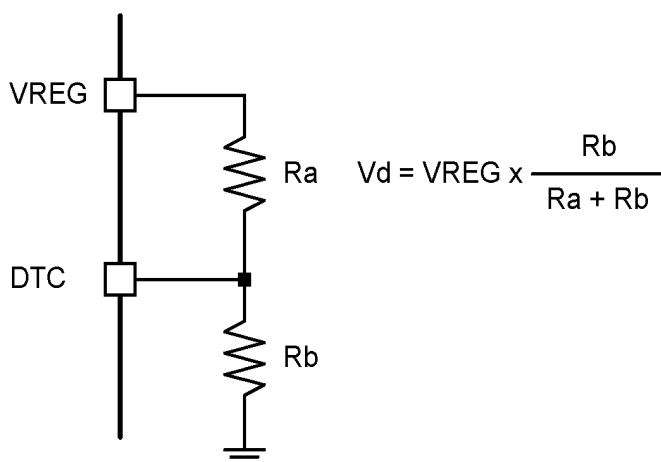
$$T_{PE}(s) = 0.7 * C_{CSCP} (\mu F)$$

Note : It could be disabled short circuit protection function by connecting CSCP pin into the ground.

Setting the Dead Time Control Level

When using Boost, SEPIC, Zeta or flyback DC/DC converter, it must prevent that output transistor works at full-ON state (ON duty = 100%). To prevent this situation, set the maximum duty of these channels. The dead time control circuit is implemented as below. When the voltage at the DTC pin is higher than the triangular wave voltage (CT, CT1, CT2), the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude = 0.5V and triangular wave minimum voltage = 0.3V.

$$Duty_{MAX.} = \left(\frac{Vd - 0.3}{0.5} \right) \times 100\%$$

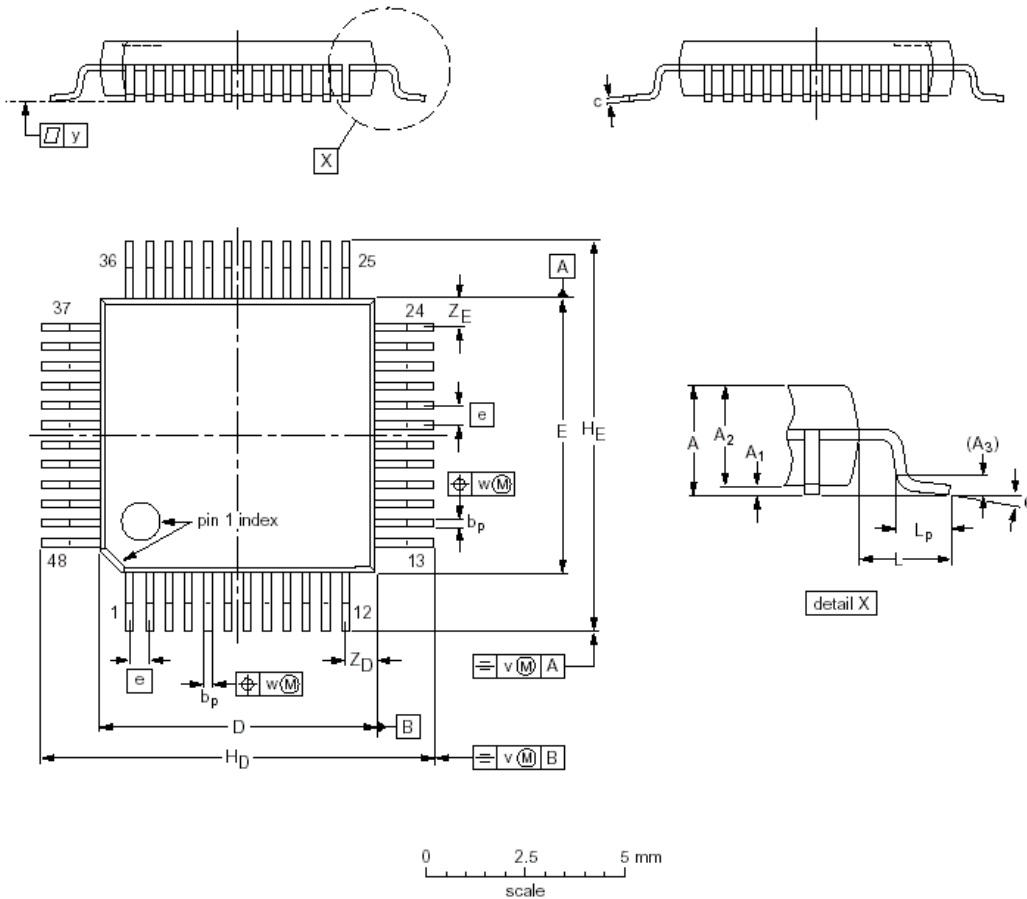


Note 1 : The circuit is suitable at CH1 to CH6.

Note 2 : Shorting DTC and VREG to disable dead time control function.

Package Outline

LQFP48



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°