



CYPRESS

CYW2336

# Dual Serial Input PLL with 2.0- and 1.1-GHz Prescalers

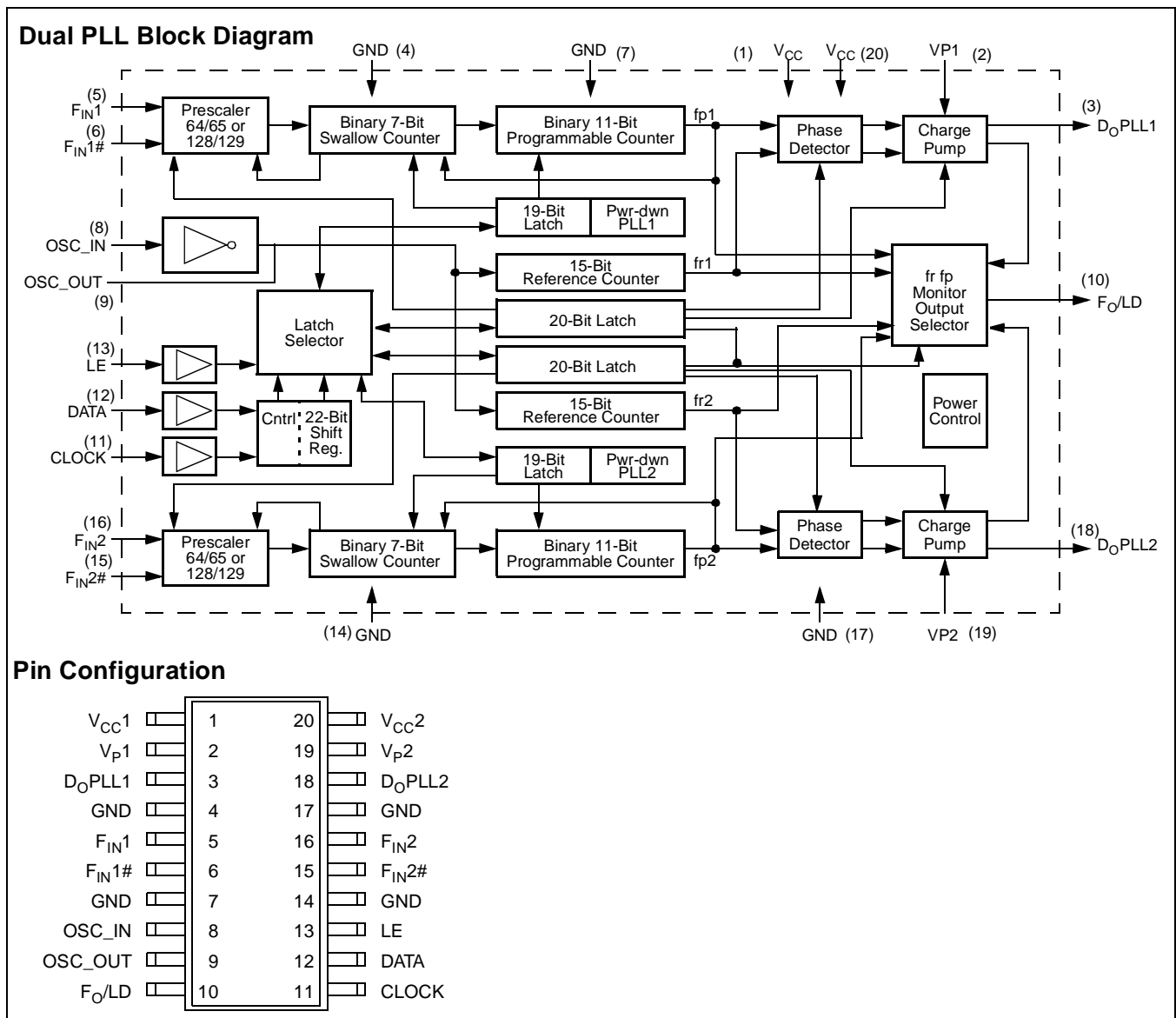
## Features

- Operating voltage 2.7V to 5.5V
- Operating frequency to 2.0 GHz on PLL1 and 1.1 GHz on PLL2 with prescaler ratios of 64/65 and 128/129
- Lock detect feature
- Power-down mode  $I_{CC} < 1 \mu A$  typical at 3.0V
- Serial data input accepts data clock rates as low as 1 kHz
- Low power/voltage operation with low current standby mode
- On-chip reference oscillator

- Available in a 20-pin TSSOP (Thin Shrink Small Outline Package)

## Applications

The Cypress CYW2336 is a dual serial input PLL frequency synthesizer designed for high performance dual conversion TV, VCR, and Set-top tuner sections, as well as downstream receivers for cable modems. The CYW2336 is also well suited for high-volume, low-cost wireless communications applications. One 2.0-GHz and 1.1-GHz prescaler, each with pulse swallow capability are included. The device operates from 2.7V and dissipates only 33 mW.



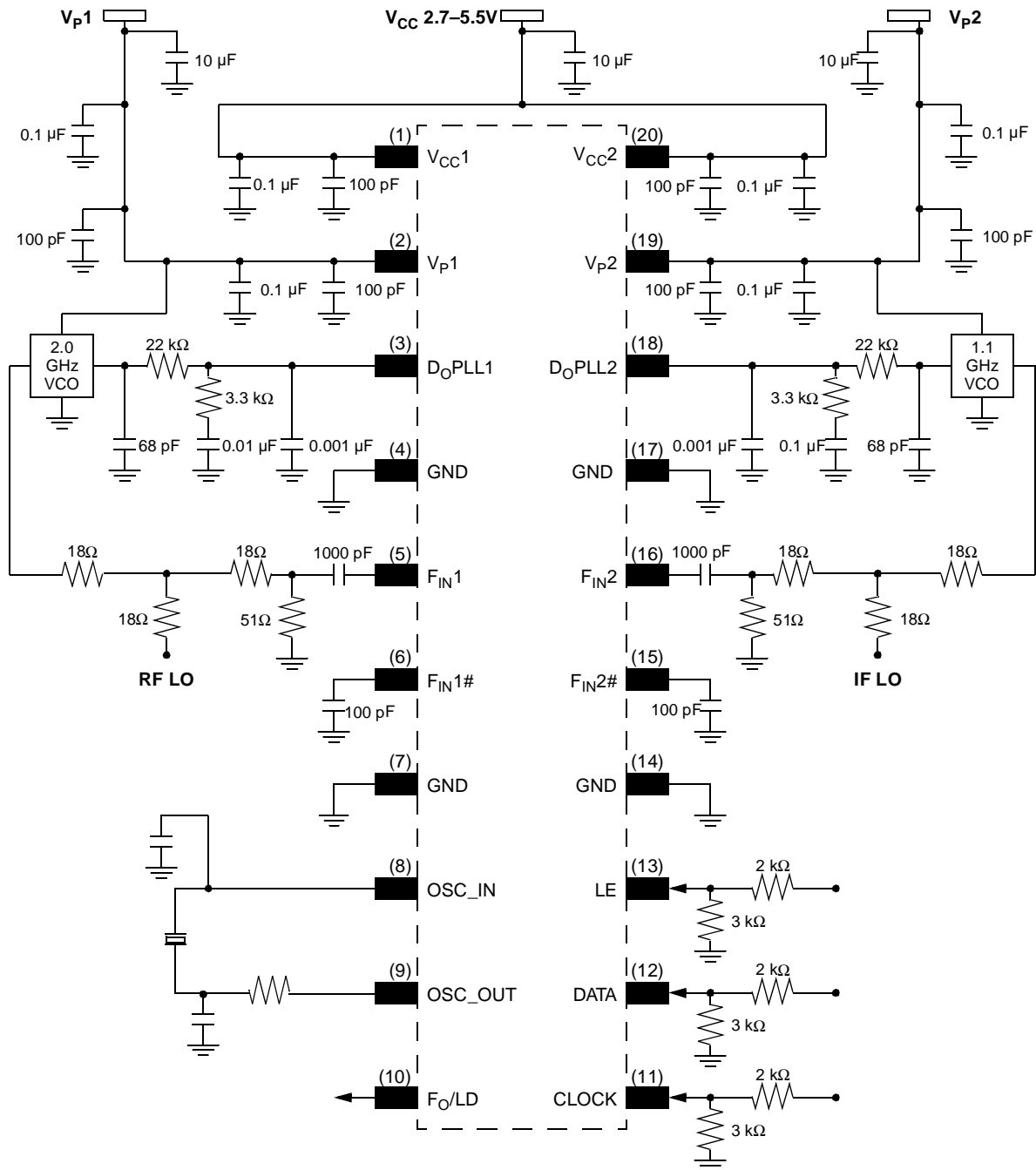


Figure 1. Application Diagram Example - CYW2336 2.0-/1.1-GHz Hi/Hi Dual PLL

**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
V <sub>CC1</sub>	1	P	<b>Power Supply Connection for PLL1 and PLL2:</b> When power is removed from both the V <sub>CC1</sub> and V <sub>CC2</sub> pins, all latched data is lost.
V <sub>P1</sub>	2	P	<b>PLL1 Charge Pump Rail Voltage:</b> This voltage accommodates VCO circuits with tuning voltages higher than the V <sub>CC</sub> of PLL1.
D <sub>OPLL1</sub>	3	O	<b>PLL1 Charge Pump Output:</b> The phase detector gain is $I_p/2\pi$ . Sense polarity can be reversed by setting the FC bit in software (via the Shift Register).
GND	4	G	<b>Analog and Digital Ground Connection:</b> This pin must be grounded.
F <sub>IN1</sub>	5	I	<b>Input to PLL1 Prescaler:</b> Maximum frequency 2.0 GHz.
F <sub>IN1#</sub>	6	I	<b>Complementary Input to PLL1 Prescaler:</b> A bypass capacitor should be placed as close as possible to this pin and must be connected directly to the ground plane.
GND	7	G	<b>Analog and Digital Ground Connection:</b> This pin must be grounded.
OSC_IN	8	I	<b>Oscillator Input:</b> This input has a V <sub>CC</sub> /2 threshold and CMOS logic level sensitivity.
OSC_OUT	9	O	<b>Oscillator Output</b>
F <sub>O</sub> /LD	10	O	<b>Lock Detect Pin:</b> This output is HIGH when the loop is locked. It is multiplexed to the output of the programmable counters or reference dividers in the test program mode. (Refer to Table 3 for configuration.)
CLOCK	11	I	<b>Data Clock Input:</b> On the rising edge, one bit of data is loaded into the Shift Register.
DATA	12	I	<b>Serial Data Input</b>
LE	13	I	<b>Load Enable:</b> On the rising edge of this signal, the data stored in the Shift Register is latched into the counters and configuration controls, PLL1 or PLL2 depending on the control bit states.
GND	14	G	<b>Analog and Digital Ground Connection:</b> This pin must be grounded.
F <sub>IN2#</sub>	15	I	<b>Complementary Input to PLL2 Prescaler:</b> A bypass capacitor should be placed as close as possible to this pin and must be connected directly to the ground plane.
F <sub>IN2</sub>	16	I	<b>Input to PLL2 Prescaler:</b> Maximum frequency 1.1 GHz.
GND	17	G	<b>Analog and Digital Ground Connections:</b> This pin must be grounded.
D <sub>OPLL2</sub>	18	O	<b>PLL2 Charge Pump Output:</b> The phase detector gain is $I_p/2\pi$ . Sense polarity can be reversed by setting the FC bit in software (via the Shift Register).
V <sub>P2</sub>	19	P	<b>PLL2 Charge Pump Rail Voltage:</b> This voltage accommodates VCO circuits with tuning voltages higher than the V <sub>CC</sub> of PLL2.
V <sub>CC2</sub>	20	P	<b>Power Supply Connections for PLL1 and PLL2:</b> When power is removed from both the V <sub>CC1</sub> and V <sub>CC2</sub> pins, all latched data is lost.

### Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating

only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{CC}$ or $V_P$	Power Supply Voltage	-0.5 to +6.5	V
$V_{OUT}$	Output Voltage	-0.5 to $V_{CC}+0.5$	V
$I_{OUT}$	Output Current	$\pm 15$	mA
$T_L$	Lead Temperature	+260	°C
$T_{STG}$	Storage Temperature	-55 to +150	°C

### Handling Precautions

Devices should be transported and stored in antistatic containers.

These devices are static sensitive. Ensure that equipment and personnel contacting the devices are properly grounded.

Cover workbenches with grounded conductive mats.

Always turn off power before adding or removing devices from system.

Protect leads with a conductive sheet when handling or transporting PC boards with devices.

If devices are removed from the moisture protective bags for more than 36 hours, they should be baked at 85°C in a moisture free environment for 24 hours prior to assembly in less than 24 hours.

### Recommended Operating Conditions

Parameter	Description	Test Condition	Rating	Unit
$V_{CC1}$ , $V_{CC2}$	Power Supply Voltage		2.7 to 5.5	V
$V_P$	Charge Pump Voltage		$V_{CC}$ to +5.5	V
$T_A$	Operating Temperature	Ambient air at 0 CFM flow	-40 to +85	°C

**Electrical Characteristics:**  $V_{CC} = V_P = 5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Unless otherwise specified

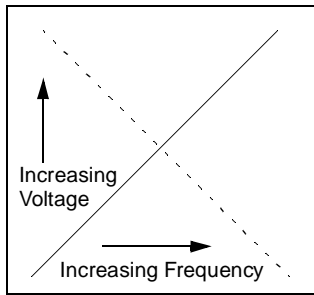
Parameter	Description	Test Condition	Pin	Min.	Typ.	Max.	Unit
$I_{CC}$	Power Supply Current PLL1 + PLL2		$V_{CC1}$ , $V_{CC2}$		12		mA
$I_{PD}$	Power-down Current	Power-down, $V_{CC} = 3.0V$	$V_{CC1}$ , $V_{CC2}$		1	25	$\mu A$
$F_{IN1}$	Operating Frequency	PLL1	$F_{IN1}$	100		2000	MHz
$F_{IN2}$		PLL2	$F_{IN2}$	100		1100	MHz
$F_{OSC}$	Oscillator Input Frequency	with OSC_OUT loaded	OSC_IN	2		25	MHz
		with OSC_OUT unloaded		2		40	MHz
$F_{\phi}$	Maximum Phase Detector Frequency			10			MHz
$V_{IN}$	Input Sensitivity	$V_{CC} = 3.0V$	$F_{IN1}$ and $F_{IN2}$	-15		4	dBm
		$V_{CC} = 5.0V$		-10		4	dBm
$V_{OSC}$	Oscillator Input Sensitivity		OSC_IN	0.5			$V_{P-P}$
$I_{IH}, I_{IL}$	Oscillator Input Current			-100		100	$\mu A$
$V_{IH}$	High Level Input Voltage		DATA, CLOCK, LE	$V_{CC} * 0.8$			V
$V_{IL}$	Low Level Input Voltage					$V_{CC} * 0.2$	V
$I_{IH}, I_{IL}$	High/Low Level Input Current			-10	0.5	10	$\mu A$
$V_{OH}$	High level Output Voltage	$V_I = 1\text{ mA}$	$F_O/LD$	$V_{CC} * 0.8$			V
$V_{OL}$	Low Level Output Voltage					$V_{CC} * 0.2$	V
$ID_{OH(SO)}$	$ID_O$ High, Source Current	$D_O = V_P/2$	$D_{OPLL1}$ $D_{OPLL2}$		-4.4		mA
$ID_{OL(SO)}$	$ID_O$ Low, Source Current				-1.2		mA
$ID_{OH(SI)}$	$ID_O$ High, Sink Current				4.4		mA
$ID_{OL(SI)}$	$ID_O$ Low, Sink Current				1.2		mA
$\Delta ID_O$	$ID_O$ Charge Pump Sink and Source Mismatch	$D_O = V_P/2$ $[ ID_{O(SI)}  -  ID_{O(SO)} ] /$ $[1/2 * \{ ID_{O(SI)}  +  ID_{O(SO)} \}] * 100\%$			3		%
$ID_O$ vs T	Charge Pump Current Variation vs. Temperature	$-40^{\circ}C < T < 85^{\circ}C$ $V_{D_O} = V_P/2^{[1]}$			5		%
$I_{OFF}$	High-Impedance Leakage Current	Loop locked, between reference spikes			$\pm 2.5$		nA

**Notes:**

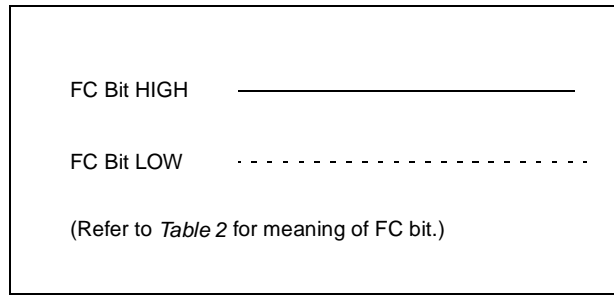
- $ID_O$  vs T; Charge pump current variation vs. temperature.  
 $[|ID_{O(SI)}|_{@T} - |ID_{O(SI)}|_{@25^{\circ}C}] / |ID_{O(SI)}|_{@25^{\circ}C} * 100\%$  and  
 $[|ID_{O(SO)}|_{@T} - |ID_{O(SO)}|_{@25^{\circ}C}] / |ID_{O(SO)}|_{@25^{\circ}C} * 100\%$ .

## Timing Waveforms

Key:

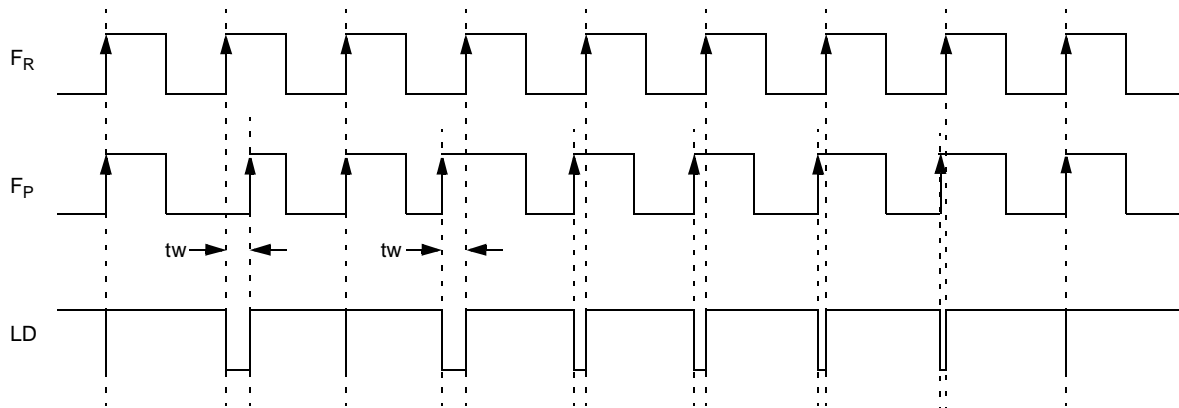


VCO Characteristics

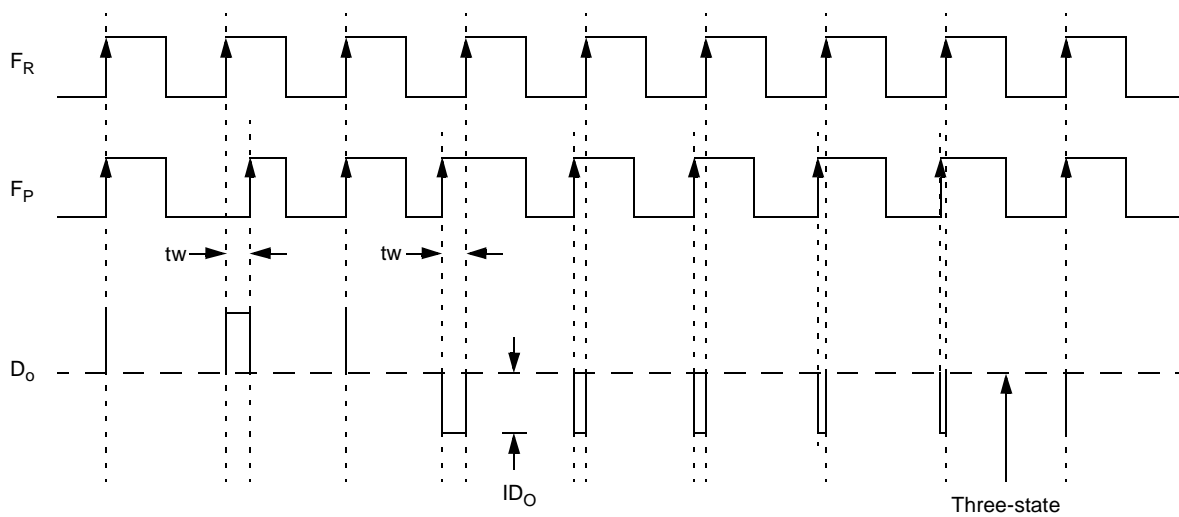


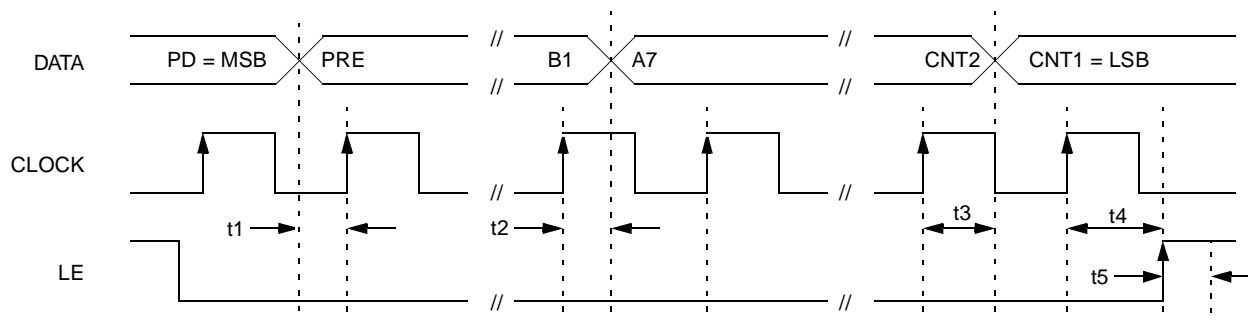
Phase Comparator Sense

### Phase Detector Output Waveform



### D<sub>O</sub> Charge Pump Output Current Waveform



**Timing Waveforms (continued)**
**Serial Data Input Timing Waveform<sup>[2, 3, 4, 5]</sup>**

**Serial Data Input**

Data is input serially using the DATA, CLOCK, and LE pins. Two control bits direct data into the locations given in *Table 1*.

**Table 1. Control Configuration**

CNT1	CNT2	Function
0	0	<b>Program Reference 2:</b> R = 3 to 32767, set PLL2 (low frequency) phase detector polarity, set current in PLL2, set PLL2 three-state, set monitor selector to PLL2.
0	1	<b>Program Reference 1:</b> R = 3 to 32767, set PLL1 (high frequency) phase detector polarity, set current in PLL1, set PLL1 three-state, set monitor selector to PLL1.
1	0	<b>Program Counter for PLL2:</b> A = 0 to 127, B = 3 to 2047, set PLL2 prescaler ratio, set power-down to PLL2.
1	1	<b>Program Counter for PLL1:</b> A = 0 to 127, B = 3 to 2047, set PLL1 prescaler ratio, set power-down to PLL1.

**Notes:**

2.  $t1-t5 = 50 \mu s > t > 0.5 \mu s$
3. CLOCK may remain HIGH after latching in data.
4. DATA is shifted in with the MSB first.
5. For DATA definitions, refer to *Table 2*.

**Table 2. Shift Register Configuration<sup>[6]</sup>**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
<b>Reference Counter and Configuration Bits</b>																					
CNT1	CNT2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	FC	IDO	TS	LD	FO
<b>Programmable Counter bits</b>																					
CNT1	CNT2	A1	A2	A3	A4	A5	A6	A7	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	PRE	PD
<b>Bit(s) Name</b>		<b>Function</b>																			
CNT1, CNT2		<b>Control Bits:</b> Directs programming data to PLL1 (high frequency) or PLL2 (low frequency).																			
R1–R15		<b>Reference Counter Setting Bits:</b> 15 bits, R = 3 to 32767. <sup>[7]</sup>																			
FC		<b>Phase Sense of the Phase Detector:</b> Set to match the VCO polarity, H = + (Positive VCO transfer function).																			
ID <sub>O</sub>		<b>Charge Pump Setting Bit:</b> ID <sub>O</sub> HIGH = 4.4 mA, ID <sub>O</sub> LOW = 1.1 mA.																			
TS		<b>Three-state Bit:</b> Three-states the D <sub>O</sub> output for PLL2 and PLL1 when HIGH.																			
LD		<b>Lock Detect:</b> Directs the lock detect signal source pin 10. Pin 10 is HIGH with narrow low excursions when locked. When not locked, this pin is LOW.																			
F <sub>O</sub>		<b>Frequency Out:</b> This bit can be set to read out reference or programmable divider at the LD pin for test purposes.																			
PRE		<b>Prescaler:</b> Prescaler divide bit, for PLL1 and PLL2 (LOW = 64/65, HIGH = 128/129).																			
PD		<b>Power-down:</b> LOW = power-up, HIGH = power-down. F <sub>IN</sub> is at a high-impedance state, respective B counter is disabled, forces three-state at D <sub>O</sub> outputs and phase comparators are disabled. The reference counter is disabled and the OSC input is high-impedance after both PLLs are powered down. Data can be input and latched in the power-down state.																			
A1–A7		<b>Swallow Counter Divide Ratio:</b> A = 0 to 127.																			
B1–B11		<b>Programmable Counter Divide Ratio:</b> B = 3 to 2047. <sup>[7]</sup>																			

**Table 3. F<sub>O</sub>/LD Pin Truth Table**

FO (Bit 22)		LD (Bit 21)		F <sub>O</sub> /LD Pin Output State
PLL1	PLL2	PLL1	PLL2	
0	0	0	0	Disable
0	0	0	1	PLL2 Lock Detect
0	0	1	0	PLL1 Lock Detect
0	0	1	1	PLL1/PLL2 Lock Detect
0	1	X	0	PLL2 Reference Divider Output
1	0	X	0	PLL1 Reference Divider Output
0	1	X	1	PLL2 Programmable Divider Output
1	0	X	1	PLL1 Programmable Divider Output
1	1	0	1	PLL2 Counter Reset
1	1	1	0	PLL1 Counter Reset
1	1	1	1	PLL1/PLL2 Counter Reset

**Notes:**

6. The MSB is loaded in first.
7. Low count ratios may violate frequency limits of the phase detector.



**Table 4. 7-Bit Swallow Counter (A) Truth Table<sup>[8]</sup>**

Divide Ratio A	A7	A6	A5	A4	A3	A2	A1
<b>PLL1 (High Frequency)</b>							
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
...	...	...	...	...	...	...	...
126	1	1	1	1	1	1	0
127	1	1	1	1	1	1	1
<b>PLL2 (Low Frequency)</b>							
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
...	...	...	...	...	...	...	...
126	1	1	1	1	1	1	0
127	1	1	1	1	1	1	1

**Table 5. 11-Bit Programmable Counter (B) Truth Table<sup>[9]</sup>**

Divide Ratio B	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
...	...	...	...	...	...	...	...	...	...	...	...
2046	1	1	1	1	1	1	1	1	1	1	0
2047	1	1	1	1	1	1	1	1	1	1	1

**Table 6. 15-Bit Programmable Reference Counter (for PLL1 and PLL2) Truth Table<sup>[9]</sup>**

Divide Ratio R	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
32766	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

**Ordering Information<sup>[10]</sup>**

Ordering Code	Package Name	Package Type	TR
CYW2336	ZI	20-pin TSSOP (0.173" wide)	Tape and Reel Option

**Notes:**

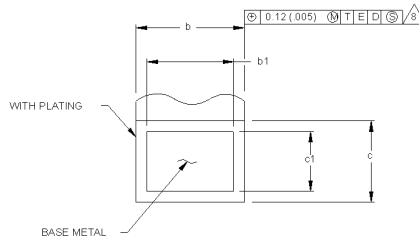
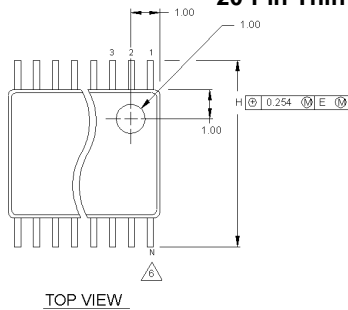
8. B is greater than or equal to A.
9. Divide ratio less than 3 is prohibited. The divide ratio can be calculated using the following equation:  

$$f_{vco} = \{(P * B) + A\} * f_{osc} / R \text{ where } (A \leq B)$$
 f<sub>vco</sub>: Output frequency of the external VCO.  
 f<sub>osc</sub>: The crystal reference oscillator frequency.  
 A: Preset divide ratio of the 7-bit swallow counter (0 to 127).  
 B: Preset ratio of the 11-bit programmable counter (3 to 2047).  
 P: Preset divide ratio of the dual modulus prescaler (64/65 or 128/129).  
 R: Preset ratio of the 15-bit programmable reference counter (3 to 32767).  
 The divide ratio N = (P \* B) + A.

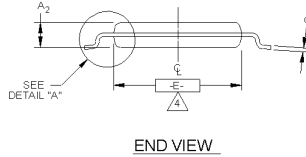
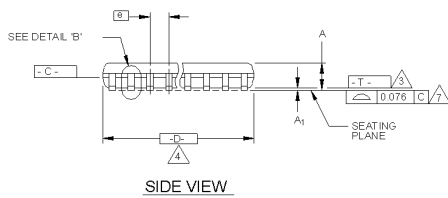
10. Operating temperature range: -40°C to +85°C.

Package Diagram

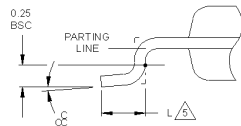
20-Pin Thin Shrink Small Outline Package (TSSOP, 0.173" wide)



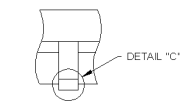
DETAIL "C"  
SCALE: 120/1  
(SEE NOTE 9)



END VIEW



DETAIL "A"  
SCALE: 30/1



DETAIL "B"  
SCALE: 30/1  
DAMBAR PROTRUSION

NOTES:

- DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (0.110±0.005 INCHES)
- DIMENSIONING & TOLERANCES PER ANS I Y 14.5M-1982.
- "T" IS A REFERENCE DATUM.
- "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
- FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS 'B' AND 'C'.
- DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
- CONTROLLING DIMENSION: MILLIMETERS.
- THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A			1.10	AA	2.90	3.00	3.10	8
A <sub>1</sub>	0.05	0.10	0.15	AB	4.90	5.00	5.10	14
A <sub>2</sub>	0.85	0.90	0.95	AC	4.90	5.00	5.10	16
b	0.19	-	0.30	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25	AE	7.70	7.80	7.90	24
c	0.090	-	0.20	AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135					
D	SEE VARIATIONS			4				
E	4.30	4.40	4.50	4				
e	0.65 BSC							
H	6.25	6.40	6.50					
L	0.50	0.60	0.70	5				
N	SEE VARIATIONS			6				
α	0°	4°	8°					

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A			0.433	AA	.114	.118	.122	8
A <sub>1</sub>	.002	.004	.006	AB	.193	.197	.201	14
A <sub>2</sub>	.0335	.0354	.0374	AC	.193	.197	.201	16
b	.0075	-	.0118	AD	.252	.256	.260	20
b1	.0075	.0087	.0098	AE	.303	.307	.311	24
c	.0035	-	.0079	AF	.378	.382	.386	28
c1	.0035	.0050	.0053					
D	SEE VARIATIONS			4				
E	.169	.173	.177	4				
e	.0256 BSC							
H	.246	.252	.256					
L	.020	.024	.028	5				
N	SEE VARIATIONS			6				
α	0°	4°	8°					

\*VARIATION AF IS DESIGNED BUT NOT TOOLED\*