FUJITSU

CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER

MB8850 SERIES

T-49-19-44

TM335-A871: January 1987

CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER

The Fujitsu MB8850 series CMOS single-chip 4-bit microcomputer family is a CMOS version of the conventional MB8840 series. Its architecture and instruction set are almost same as the MB8840 series. By CMOS process, MB8850 series operate with low power dissipation, and further the standby function enable the data retention with lower current.

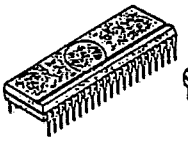
MB8850 series consists of the MB8851, 52, 54, 55, 56, and 58. This series contain max. 2K by 8-bit mask ROM (program memory), max. 128 by 4-bit static RAM (data memory), max. 37 I/O lines (including a serial port), an 8-bit timer/counter, a clock generator, and programmable logic array (PLA).

They are fabricated by the silicon-gate CMOS process, and operate with a single power supply and a 4MHz clock with a prescaler (minimum instruction execution time is 3.0μs). And they are packaged in 42-pin plastic standard/shrink DIP (MB8851), 28-pin plastic standard/shrink DIP (MB8852/54), or 48-pin plastic flat package (MB8855/56/58).

CMOS technology allows the device to operate with low power dissipation (6mA typ. at 1MHz), and further the standby function enables data retention with lower current (100μA max. at V_{CC}=6V).

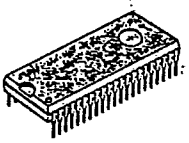
For user's development of the MB8850 series based system, Fujitsu provides the MB8840/50 cross-assembler and host emulator which run on the CP/M-86 and PC-DOS machines, the MB2115 series evaluation board system, and the MB8850U1/U2 and MB8850H piggyback EPROM evaluation devices which have an external 2K x 8-bit EPROM (MBM27C32A). These development tools enable users to minimize their development time and cost.

MB8851M



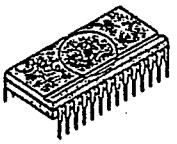
42-PIN PLASTIC STANDARD DIP
(DIP-42P-M01)

MB8851-PSH



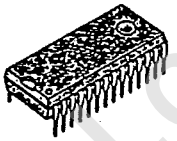
42-PIN PLASTIC SHRINK DIP
(DIP-42P-M02)

MB8852M/54M



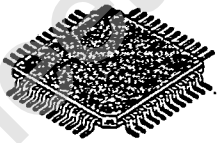
28-PIN PLASTIC STANDARD DIP
(DIP-28P-M02)

MB8852-PSH/54-PSH



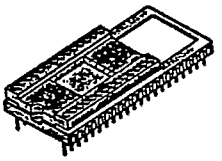
28-PIN PLASTIC SHRINK DIP
(DIP-28P-M03)

MB8855M/56M/58M



48-PIN PLASTIC FLAT PACKAGE
(FPT-48P-M02)

MB8850U1/U2-C



42-PIN CERAMIC MODULE
(MDP-42C-P04)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FEATURES

- CMOS Single-chip 4-bit Microcomputer

- Program Memory:
  - o MB8851/52 (MB8855/56): 2K x 8 bit mask ROM
  - o MB8854 (MB8858) : 1K x 8 bit mask ROM

- Data Memory:
  - o MB8851/52 (MB8854/56): 128 x 4 bit static RAM
  - o MB8854 (MB8858) : 64 x 4 bit static RAM

- I/O Lines:
  -MB8851 (MB8855):
    - o K-Port: 4-bit parallel input-only port
    - o P-Port: 4-bit parallel output-only port
    - o O-Port: 8-bit parallel output-only port
    - o R-Port: Four 4-bit parallel or 16 individual input/output ports
    - o C-Port: Serial I/O, interrupt input, timer/counter input, and timing output
  -MB8852/54 (MB8856/58):
    - o K-Port: 4-bit parallel input-only port
    - o O-Port: 8-bit parallel output-only port
    - o R-Port: Two 4-bit parallel and one 3-bit parallel or 11 individual input/output ports
    - o C-Port: Interrupt input and timer/counter input

- Two Mask Option Output Port Types for O-, P-, and R-Ports:
  - o Standard open-drain
  - o Standard pull-up

- On-chip Mask-programmable PLA (Programmable Logic Array) for Data Conversion at O-Port

- 8-bit Programmable Timer/Counter with Two Clock Modes:
  - o Internal clock (Timer)
  - o External clock (Counter)

- Serial I/O with 4-bit Serial Buffer/Two Clock Modes (MB8851/55):
  - o Internal clock
  - o External clock

- Mask Option Serial Port Output Latch:
  - o With prescaler
  - o Without prescaler

- On-chip Clock Generator:
  - o Crystal/ceramic Resonator or External Clock Drive

- Mask Option Divid-by-two Clock Prescaler for Expanding Clock Range

- Single-level Three Priority Source Maskable Interrupt:
  - o External
  - o Timer/counter overflow
  - o Serial buffer full/empty

- 4 Nesting Levels for Subroutine Call

FEATURES (Continued)

- Instruction Set: Same as MB8840, MB8850F/50B/50H series instruction set
  - o Number of instructions : 70(MB8851/55), 69(MB8852/54/56/58)
  - o Instruction length/cycle: 1 byte/1 cycle or 2 bytes/2 cycles
  - o Execution time : 3 µs min. using 4 MHz clock with prescaler (or 2 MHz clock without prescaler)

- Mask Option Standby Function:
  - o No standby function
  - o Hardware-initiation standby function

- Low Power Dissipation:
  - -Standard/A-version:
    - o 6 mA max. at V_{CC}=5.5V and fc=1 MHz (Active mode)
    - o 100 µA max. at V_{CC}=3.0V and fc=0 MHz (Standby mode)
  - -L-version:
    - o 3 mA max. at V_{CC}=4.0V and fc=0.5MHz (Active mode)
    - o 100 µA max. at V_{CC}=3.0V and fc=0 MHz (Standby mode)

- Single Power Supply Three Supply Voltage Versions:
  - o Standard version (No suffix) : 4.5V to 5.5V (Active mode), 3.5V to 6.0V (Standby mode)
  - o A-version (Suffix A) : 3.5V to 6.0V (Active mode), 3.0V to 6.0V (Standby mode)
  - o L-version (Suffix L) : 2.5V to 4.0V (Active mode), 2.0V to 4.0V (Standby mode)

- Wide Operating Temperature Range:
  - o T_A= -40°C to +85°C (Standard version)
  - o T_A= -30°C to +70°C (A and L versions)

- Silicon-gate CMOS Process

- Five Package Types:
  - -MB8851/A/L:
    - o 42-pin plastic standard DIP: (Suffix M)
    - o 42-pin plastic shrink DIP: (Suffix -PSH)
  - -MB8852/A/L and MB8854/A/L:
    - o 28-pin plastic standard DIP: (Suffix M)
    - o 28-pin plastic shrink DIP: (Suffix -PSH)
  - -MB8855/A/L, MB8856/A/L, MB8857/A/L, and MB8858/A/L:
    - o 48-pin plastic flat package: (Suffix M)

- Powerful Development Support:
  - o Intellec Series III MDS cross-assembler (SM05212-A010)
  - o CP/M-86 and PC-DOS cross-assembler (SM07412-A012/SMXXXXX-XXXX)
  - o CP/M-86 and PC-DOS host emulator software for monitoring evaluation board and symbolic debugging (SM07412-G022/SMXXXXX-XXXX)
  - o MB2115 series evaluation board (-01, -02, -04, and -33A) for software debugging
  - o MB8850U1/U2 CMOS piggyback EPROM evaluation device

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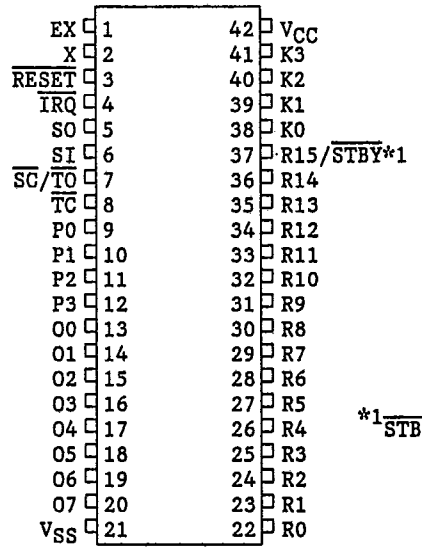
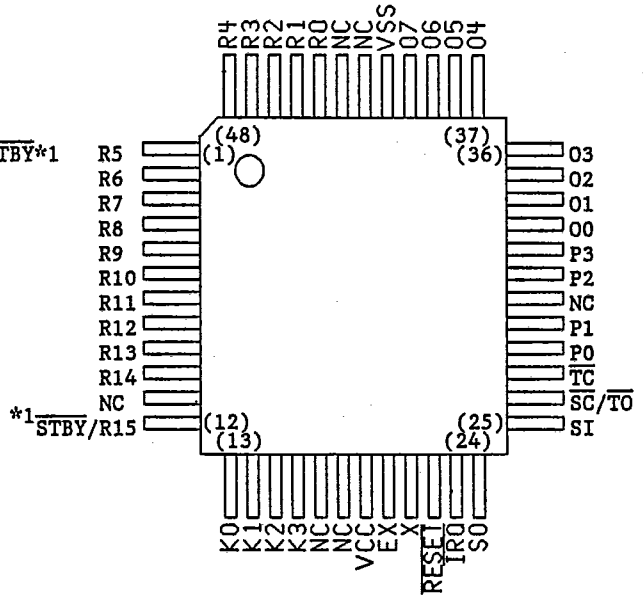
Fig. 1: PIN ASSIGNMENT

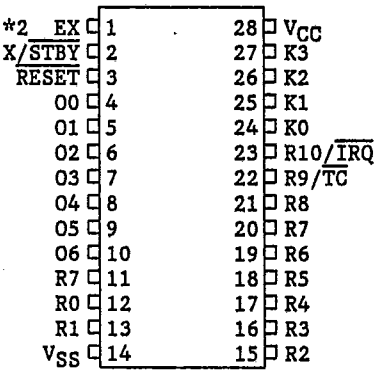
MB8851(Top View)



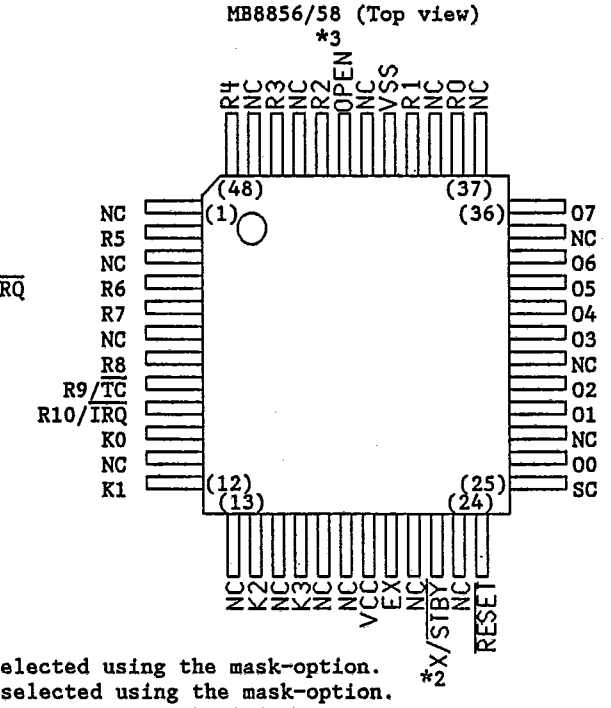
MB8855 (Top view)



MB8852/54(Top View)

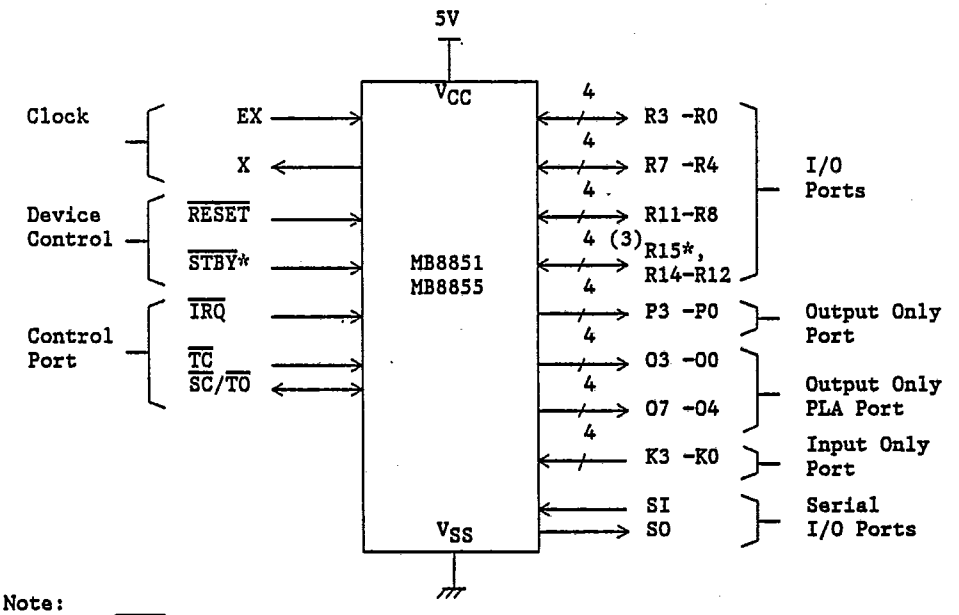


MB8856/58 (Top view)



*1: Either R15 or $\overline{\text{STBY}}$ is selected using the mask-option.
*2: Either of X or $\overline{\text{STBY}}$ is selected using the mask-option.
*3: This pin should not be connected must be left open.

Fig. 2: MB8851/55 LOGIC SYMBOLS



Note:
* Either $\overline{\text{STBY}}$ or R15 is selected depending on mask option of standby function.

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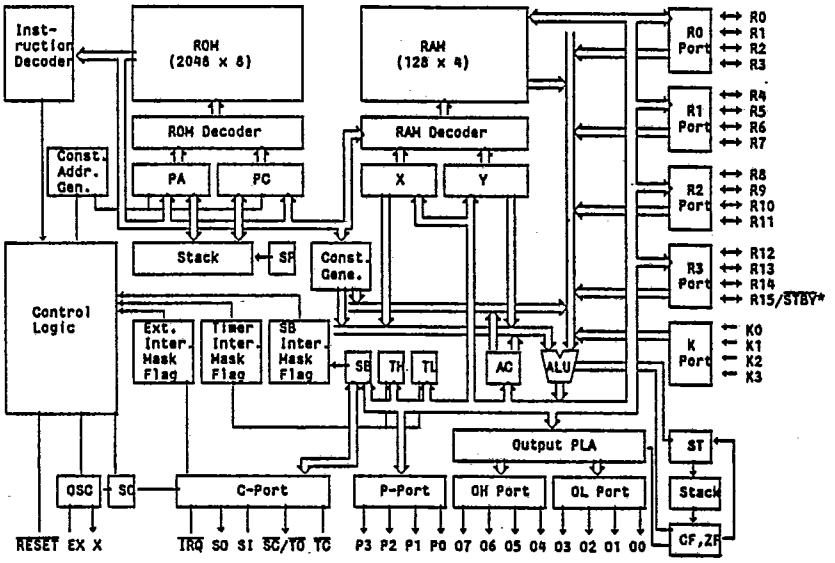
Fig. 3: MB8851/55 BLOCK DIAGRAMS



Note:
* Either R15 or $\overline{\text{STBY}}$ is selected using mask-option.

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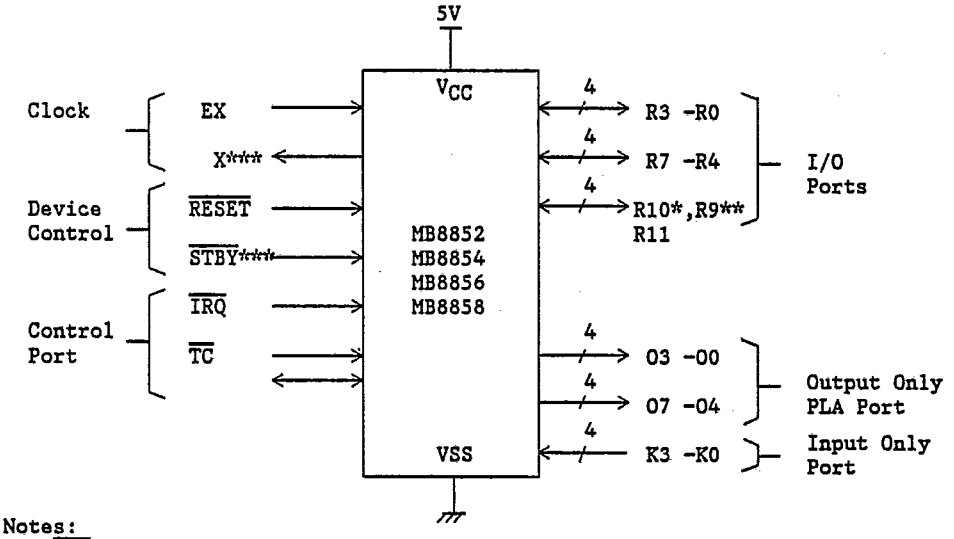
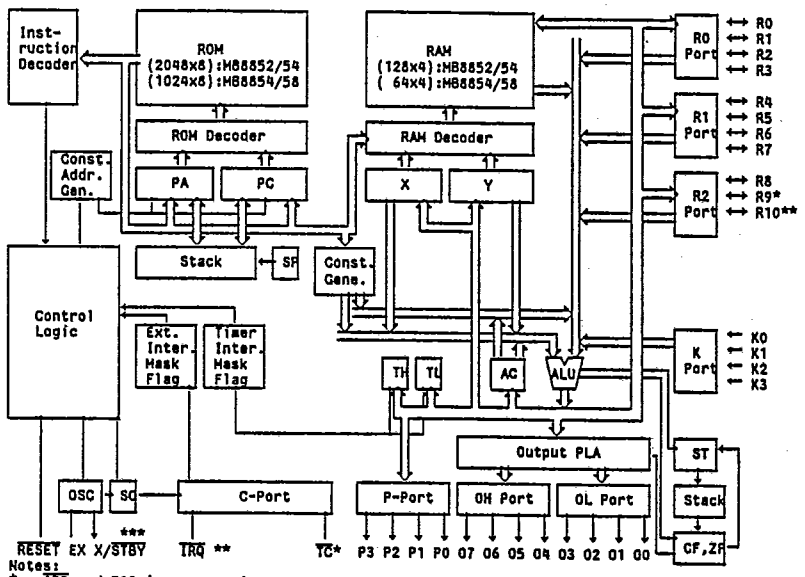
Fig. 4: MB8852/54/56/58 LOGIC SYMBOLS



Notes:
* $\overline{IRQ}$ and R10 is common pin.
** TC and R9 is common pin.
**** Either X or $\overline{STBY}$ is selected depending on mask option of oscillator type and standby function.

Fig. 5: MB8852/54/56/58 BLOCK DIAGRAMS



Notes:
* $\overline{IRQ}$ and R10 is common pin.
** $\overline{TC}$ and R9 is common pin.
*** Either X or $\overline{STBY}$ is selected depending on mask option of oscillator type and standby function.

PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB8850 series.

Table 1: PIN DESCRIPTION

Symbol	Pin No. MB8851 (MB8855)	Pin No. MB8852 (MB8856) MB8854 (MB8858)	Type	Name & Function
• Power Supply				
V_{CC}	42 (19)	28 (19)	-	+5V DC power supply pin.
V_{SS}	21 (41)	14 (41)	-	Ground pin.
• Clock				
EX	1 (20)	1 (20)	I	**Oscillator Input:** Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ceramic resonator is connected between the EX and X pins. When an external oscillator is used, the EX pin receives the exter-nal oscillator signal. This pin is a non-hysteresis input.
X	2 (21)	2 (21)	O	**Oscillator Output:** Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator is connected between the EX and X pins. When an external oscillator is used, the X pin should be left open. In MB8852 (MB8856) and MB8854 (MB8858), this X pin is common to the $\overline{STBY}$ pin. Either of them is selected using mask option. When the crystal/ceramic resonator is implemented, the X pin selected.
• Device Control				
$\overline{RESET}$	3 (22)	3 (24)	I	**Reset:** An external reset input to the internal reset circuit. A low level on the $\overline{RESET}$ pin forcedly stops the MCU's operations, and initializes its internal state. After the $\overline{RESET}$ pin returns high, the MCU restarts execution of program from address #0 (of page #0). The $\overline{RESET}$ pulse must be low for at least two instruction cycles (12 clock periods: 6μs at 4MHz crystal with prescaler) while the oscillator is stably running after power on. An external capacitor (with an internal pull-up resistor) or RC-network, whose time constant should be enough longer than the reset time required, is needed as the external reset circuit. A power-on reset operation requires an external RC-network, whose time constant should be than the supply voltage (V_{CC}) rise time and the oscillator stabilization time.

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Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8851 (MB8855)	Pin No. MB8852 (MB8856) MB8854 (MB8858)	Type	Name & Function
• Device Control (Continued)				
$\overline{RESET}$	3 (22)	3 (24)	I	This pin is a hysteresis input with an internal pullup resistor.
$\overline{STBY}$	37 (12)	2 (22)		**Standby:** A standby initiation/release input to the on-chip standby control circuit control. A low level on the $\overline{STBY}$ pin triggers the standby initiation sequence to force the MCU into the standby mode, and high-level triggers the standby release sequence to release the MCU from the standby mode. The $\overline{STBY}$ initiation pulse and release pulse must be low and high for at least 13 instruction cycle. The pin is inactive during reset. This pin is a hysteresis input with an internal pullup resistor. The $\overline{STBY}$ pin is common to the R 15 pin (MB8851/55) or X pin (MB8852/56 and MB8854/58). Either of them is selectable using mask-option. The $\overline{STBY}$ pin is selected when the standby function is implemented. Note: When the $\overline{STBY}$ pin is selected in the MB852/56 and MB8854/58, only the external clock drive is available.
• C-Port				
$\overline{IRQ}$	4 (23)	23 (9)	I	**Interrupt Request:** A maskable external interrupt input. The falling edge of $\overline{IRQ}$ pulse sets the external interrupt request flag to generate an external interrupt request, only if the external interrupt is enabled in advance by EN instruction. Also, the $\overline{IRQ}$ pin state, which is reflected in the external interrupt input flag (IF) regardless of enabling/disabling the external interrupt, is testable using TSTI instruction. (When $\overline{IRQ}$=L, IF=1; otherwise IF=0.) The $\overline{IRQ}$ pin is common to the R10 pin (MB8852/56 and MB8854/58). Either of them is selectable using software. This pin is a non-hysteresis input with an internal pullup resistor.
$\overline{TC}$	8 (27)	22 (8)	I	**Timer/Counter:** An external count clock input to the on-chip timer/counter. The falling edge of $\overline{TC}$ pulse increments the timer/counter by one bit when the external count clock (counter) mode is enabled by EN instruction. This pin is inactive when the external count clock mode is disabled by DIS instruction or reset.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8851 (MB8855)	Pin No. MB8852 (MB8856) MB8854 (MB8858)	Type	Name & Function
• C-port (Continued)				
$\overline{TC}$	8 (27)	22 (8)	I	This $\overline{TC}$ pin is common to the R9 pin (MB8852/56 and MB8854/58). Either of them is selectable using software. This pin is a non-hysteresis input with an internal pullup resistor.
$\overline{SC}/\overline{TO}$	7 (26)	-	I/O	**Shift Clock/Timing Output:** One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), and synchronous timing output ($\overline{TO}$) is enabled using EN instruction. $\overline{SC}$: 1) Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the serial buffer one bit right (from MSB to LSB). This input is inactive when the external clock mode is disabled by DIS instruction or reset. This pin is a non-hysteresis input. 2) Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock (the on-chip state counter output $\phi 1$: 1/6 of clock generator frequency) shifts the contents of the serial buffer one bit right. In this mode, an internal timing signal, which is generated by the on-chip state counter outputs, $\phi 1$ and $\phi 2$ is output onto the $\overline{SC}$ pin for synchronization. $\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal same as the $\overline{SC}$ output in the internal shift clock mode is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output.
SI	6 (25)	-	I	**Serial Data Input:** Data input to the on-chip serial buffer register. The falling edge of the external or internal shift clock ($\overline{SC}$) shifts the data bit on the SI pin into the MSB of the serial buffer when the serial port is enabled by EN instruction. This pin is inactive when the serial port is disabled by DIS instruction or reset. This pin is a non-hysteresis input with an internal pull-up resistor.

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Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8851 (MB8855)	Pin No. MB8852 (MB8856) MB8854 (MB8858)	Type	Name & Function
• C-Port (Continued)				
SO	5 (24)	-	O	**Serial Data Output:** Data output of the on-chip serial buffer register. An output latch can be provided for the SO pin using mask option. Without the output latch, the LSB data of the serial buffer appears directly to the SO pin. With the output latch implemented, the LSB data is output to the SO pin after it is shifted into the output latch at the falling edge of the external or internal shift clock ($\overline{SC}$). This pin is set high by reset when the output latch is implemented.
• I/O Port				
K3-K0	41-38 (16-13)	27-24 (16,14, 12,10)	I	**K-Port:** A 4-bit parallel non-latched input-only port. K0 is LSB. 4-bit data on K-Port is input into the accumulator by INK instruction. These pins are internally pullup.
P3-P0	12- 9 (32,31, 29,28)	-	O	**P-Port:** A 4-bit parallel latched output-only port. P0 is LSB. 4-bit data in the accumulator is output to P-Port by OUTP instruction. For P-Port pins, one of the standard pull-up and standard open-drain output can be selected using mask option. This port is set high (standard pull-up) or high-Z (standard open-drain) by reset.
O3-O0, O7-O4	16-13, (36-33) 20-17 (40-37)	7- 4 (31,29, 28,26) 11- 8 (36,34, 33,32)	O	**O-Port:** An 8-bit parallel latched output-only port with the on-chip mask-programmable PLA (Programmable Logic Array) for output data conversion. Depending on user's PLA pattern, this port functions as a dual 4-bit parallel output or an 8-bit parallel PLA output. Dual 4-bit parallel output: By OUTO instruction, 4-bit data in the accumulator is output, without conversion, onto the lower nibble (O3-O0) or upper nibble (O7-O4) of O-Port, depending on whether the carry flag (CF) is "0" or "1". 8-bit parallel PLA output: By OUTO instruction, 4-bit data in the accumulator and the carry flag (CF) bit are converted into 8-bit data through the PLA array, and the 8-bit data is output to O-Port. Depending on user's PLA pattern, 32 kinds of 8-bit data conversions are possible. For example, it can be encoded into 8-segment data for LED display.

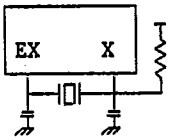
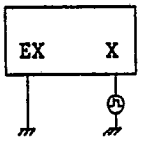
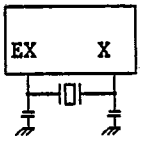
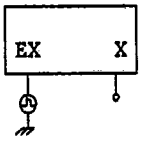
Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8851 (MB8855)	Pin No. MB8852 (MB8856) MB8854 (MB8858)	Type	Name & Function
• I/O Port (Continued)				
O3-O0,	16-13, (36-33)	7- 4 (31,29, 28,26)	O	For O-Port pins, one of the standard pull-up and standard open-drain output can be selected using mask option. This port is set high (standard pull-up) or high-Z (standard current) by reset.
O7-O4	20-17 (40-37)	11- 8 (36,34, 33,32)		
R3 -R0,	25-22, (49-44)	16,15, 13,12 (46,44, 40,38)	I/O	R-Port: This port functions as four 4-bit parallel input (non-latched)/output (latched) ports, or 16 individual input (non-latched)/output (latched) lines, depending on instructions. Parallel I/O: Each 4-bit port is named R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R15-R12), and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of R-Ports #0 to #3 by OUT instruction. 4-bit data on the addressed port is input into the accumulator by IN instruction. (Before IN instruction, the port to be addressed must be set up to "1" state (input) mode).) Individual I/O: Each line from R15 to R0 is indirectly addressed by the Y-register (Bit #). The addressed line is individually set/reset by SETR/RSTR instruction, and especially each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. The addressed line is individually testable by TSTR instruction, and each line of R-Port #2 (R11-R8) is directly testable in paticular by TSTD instruction. (Before the TSTR and TSTD instructions, the line to be addressed must be set up to "1" (input mode).) For R-Port pins, one of the standard pull-up and standard open-drain output can be selected using mask option. This port is set high (standard pull-up) or high-Z (standard open-drain) by reset. MB8851/55: The R15 pin is common to the $\overline{\text{STBY}}$ pin. Either of them can be selected using mask option. The R15 pin is selected when no standby function is implemented. MB8852/56: The R9 pin is common to the $\overline{\text{TC}}$ pin. and MB8854/58 R10 is $\overline{\text{IRQ}}$ pin.
R7 -R4,	29-26, (3-1, 48)	20-17 (5,4, 2,48)		
R11,	33,(7)	-		
R10-R8,	32-30, (6-4)	23-22, (9-7)		
R15-R12	37-34 (12, 10-8)			

Note: Parenthis number is applied to MB8855/56/58.

DIFFERENCES BETWEEN MB8840 SERIES AND MB8850 SERIES

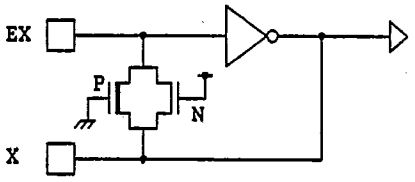
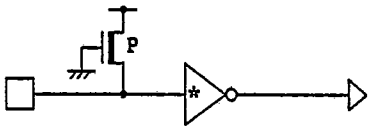
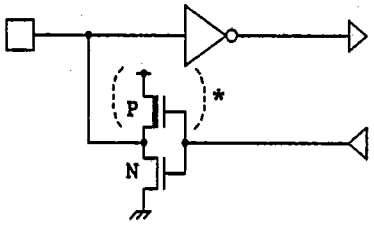
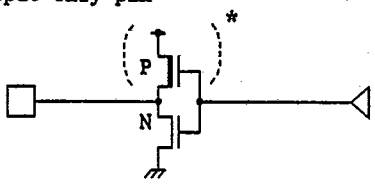
Table 2: DIFFERENCES BETWEEN MB8840 SERIES AND MB8850 SERIES

Item \ Device	MB8840 SERIES	MB8850 SERIES
Process	NMOS	CMOS
Oscillator Type	· Crystal/ceramic oscillator or external clock drive · RC-network oscillator or external clock drive (Mask option)	· Crystal/ceramic oscillator or external clock drive
Method of Oscillation	Crystal/Ceramic Resonator:  External Clock Drive: 	Crystal/Ceramic Resonator:  External Clock Drive: 
Output Port Type (O-, P-, and R-Ports)	· Standard open-drain · Standard pull-up · high-current open-drain · High-current open drain (Mask option)	· Standard open-drain · Standard pull-up (Mask option)
Standby Function	· No standby	· No standby · Hardware-initiation standby (Mask option)
Power Dissipation: -Active -Standby	54mA typ. at V_{CC}=5.5V -	6mA typ. at V_{CC}=5.5V and fc=1MHz (standard version) 100µA max. at V_{CC}=3.0V and fc=0MHz (standard version)
Supply Voltage:	· 4.5V to 5.5V	· Standard Version: 4.5V to 5.5V · A-Version : 3.5V to 6.0V · L-Version : 2.0V to 4.0V
Members	· MB8842M/-PSH, MB8846M · MB8843M/-PSH, MB8847M · MB8844M/-PSH, MB8848M	· MB8851M/-PSH, MB8855M · MB8852M/-PSH, MB8856M · MB8854M/-PSH, MB8858M A- and L-versions are available for each part above.

INPUT/OUTPUT CIRCUITS

All input-only pins are internally pulled up, and all output-only and input/output pins except O-, P-, and R-Ports have push-pull output buffer (standard pull-up). O-, P-, and R-Ports can have push-pull (standard pull-up) or open-drain (standard) buffer using mask option.

Table 3: INPUT/OUTPUT CIRCUITS

Pin	Circuit	Note
EX, X	• Crystal/Ceramic OSC or external clock 	1. Non-hysteresis inverter 2. Feedback resistor: Approx. 2 MΩ typ. (at V_{CC}=5V)
$\overline{RESET}$,* SI, K-Port, $\overline{STBY}$*, $\overline{IRQ}$(MB8851/55)* $\overline{TC}$(MB8851/55)*	• Input only pin 	• Input pull-up resistor (P-ch. Tr.): Approx. 300kΩ typ. (at V_{CC}=5V) * Hysteresis inverter for $\overline{RESET}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{STBY}$
$\overline{SC}$/$\overline{TO}$, R-Port,* $\overline{TC}$(MB8852/54/56/58) $\overline{IRQ}$(MB8852/54/56/58)	• Input/Output pin 	• Output pull-up resistor (P-ch. Tr.): Approx. 5kΩ typ. (at V_{CC}=5V) • Output port options for O-, P-, and R-Ports 1: Standard pull-up: Pull-up resistor (P-ch. Tr.): Approx. 5kΩ typ. (at V_{CC}=5V) *2: Standard open-drain: Without P-ch. pull-up resistor
SO, P-Port,* O-Port *	• Output only pin 	

USER MASK OPTIONS

The MB8850 series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Program Memory	-	User Program	-	1 MB8851/52 (MB8855/56): 2048 x 8 bits 2 MB8854 (MB8858): 1024 x 8 bits
Clock Prescaler	CLK	No	0	f_C=0.5 MHz to 2.0 MHz
		Yes	1	f_C=1.0 MHz to 4.0 MHz
Output PLA Data	SPLA	4-bit parallel output	0	
		8-bit parallel output	1	Customer's output PLA data is needed.
Serial Port Output Latch	SRL	No	0	
		Yes	1	
Output Port Type	PORT	Standard open-drain	0/L	Output port circuit option selected must be the same for all O-, P-, and R-Ports.
		Standard pull-up	1/M	
Standby Function	STBY	No	0	1 MB8851 (MB8855): Pin 5(12) functions as R15. 2 MB8852/54 (MB8856/58) Pin 2(22) functions as X.
		Yes(Hardware initiation	1	1 MB8851 (MB8855): Pin 5(12) functions as $\overline{\text{STBY}}$. 2 MB8852/54 (MB8856/58) Pin 2(22) functions as $\overline{\text{STBY}}$.

NOTES ON OPERATION

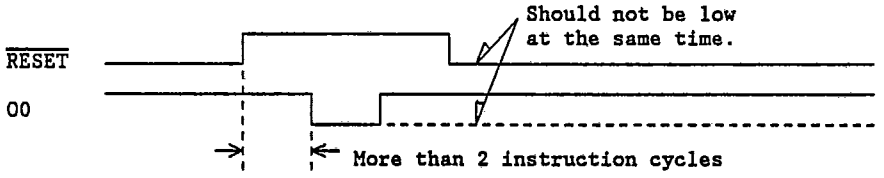
- **Prevention Latch-up**
  Latch-up may occur in CMOS devices when a voltage higher than V_{CC} or lower than V_{SS} is applied to any input or output pin, or when a voltage exceeding the absolute maximum ratings is applied between V_{CC} and V_{SS} pins. If latch-up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

- **Treatment of Unused Pins**
  Unused input pins should be pulled up or down with external resistors they may cause some malfunction. (However, the X pin should be open when an external clock oscillator is used.)

- **Special Function of O0 Pin**
  The O0 pin has another function as a test terminal, in addition to its normal O-Port function. If the O0 pin is forced low while the $\overline{\text{RESET}}$ pin is low, the MCU is placed in the test mode. Therefore, the O0 pin should not be forced low while the $\overline{\text{RESET}}$ pin is low (when all output ports are initialized).

  Especially when the open-drain is selected for the output port option, the O0 pin should be externally pulled up because such open-drain outputs are subject to noise disturbance if left floating.

  At least 2 instruction cycles are required to change O0 pin from high to low after releasing reset ($\overline{\text{RESET}}$: Low → High)



- **$\overline{\text{TO}}$ output in MB8852/56 and MB8854/58**
  The input and output timings are specified with reference to $\overline{\text{TO}}$ (Timing output) output signal in AC characteristics. The MB8851/55 have the $\overline{\text{TO}}$ pin ($\overline{\text{SC}}/\overline{\text{TO}}$), and can output $\overline{\text{TO}}$ signal on that pin by EN instruction. The MB8852/56 and MB8854/58 don't have the $\overline{\text{TO}}$ pin, but can output $\overline{\text{TO}}$ signal on the R8 for reference by a special EN instruction.

- **Drive of R-Port Inputs**
  When the standard pull-up is selected for the output port option, normal CMOS gate devices cannot drive R-Port input. CMOS drive gates are needed. If normal CMOS gates are to be used, the open-drain option should be selected.

- **Standby Current**
  The standby current value specified in DC characteristics is the value when the clock is stopped and all outputs are open, which is different from actual use conditions.

NOTES ON OPERATION (Continues)

- **Supply Voltage**
  Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:
  (1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
  (2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB8850 series instruction set includes 70(69)* instructions, 93% of which are single-byte and single-cycle, and 7% two-byte and two-cycle. The MB8850 series instruction set is exactly the same as the MB8850F/50B/50H/530 series instruction set, and is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

* 70: MB8851, MB8855
69: MB8852, MB8854, MB8856, MB8857

Tables 5 and 6 summarizes the MB8850 series instruction set.

Table 5: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Register-to-Register Transfer	TATH	05	·	·	·	1/1	TH←(AC)
	TATL	06	·	·	·	1/1	TL←(AC)
	TAS	07	·	·	·	1/1	SB←(AC)
	TAY	04	·	·	·	1/1	Y←(AC)
	TSA	17	↕	·	·	1/1	AC←(SB)
	TTHA	15	↕	·	·	1/1	AC←(TH)
	TTLA	16	↕	·	·	1/1	AC←(TL)
	TYA	14	↕	·	·	1/1	AC←(Y)
	XX	1B	↕*1	·	·	1/1	(AC)≠(X)
Register-to-Memory Transfer	L	0D	↕	·	·	1/1	AC←{M(X,Y)}
	LS	2B	↕	·	·	1/1	SB←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	STDC	1A	↕*2	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)-1
	STIC	0A	↕*2	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)+1
	STS	2A	↕	·	·	1/1	M(X,Y)←(SB)
	X	0B	↕*1	·	·	1/1	(AC)≠{M(X,Y)}
	XD D	50-53*	↕*1	·	·	1/1	(AC)≠{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ≠{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included in LI instruction)
	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-5F*	↕	·	·	1/1	X3←0, X2 to X0←imm; imm=0 to 7
	LYI imm	80-8F*	↕	·	·	1/1	Y ←imm; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	70-7F*	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	AND	0F	↕	·	↓Z	1/1	AC←(AC)∩{M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	↕	↕	↓Z	1/1	imm-(Y) ; imm=0 to 15
	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	7F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruction)
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)

Table 5: INSTRUCTION SET SUMMARY (Continued)

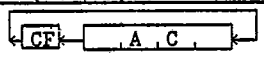
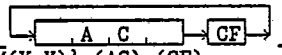
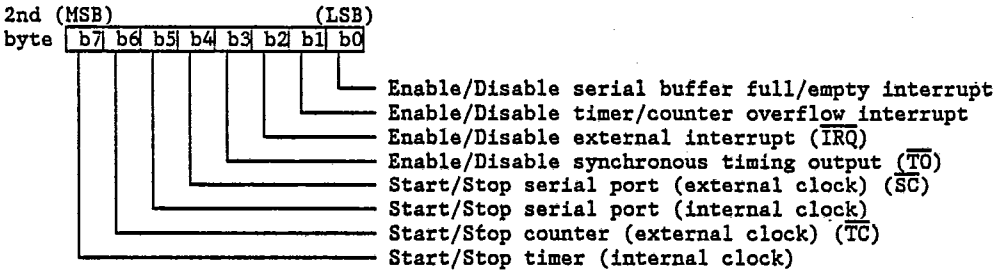
	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Arithmetic & Logical Operation	ICA	71	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruction)
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←(AC)+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipulation	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00-3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00-3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #)
	INK	12	↕	·	·	1/1	AC←(K)
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #)
	OUTO	01	·	·	·	1/1	O←OPLA(AC, CF); OPLA: Output PLA function determined
	OUTP *4	02	·	·	·	1/1	P←(AC) by PLA pattern
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of Port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of Port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000-67FF *	·	·	·	2/2	If ST=1, Subroutine Call for addr; addr=0 to 2047. ST=0, Not Subroutine Call.
	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPA addr	3D00-3DFF *	·	·	·	2/2	Branch always to addr on page #n; addr=(AC) x 4, n=0 to 31
	JPL addr	6800-6FFF *	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 2047. ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return From Interrupt Routine
	RTS	2C	·	·	·	1/1	Return From Subroutine
Flag Manipulation	RSTC	23	·	↓	·	1/1	CF←0
	SETC	21	·	↑	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No Operation

Table 5: INSTRUCTION SET SUMMARY (Continued)

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:



*4: MB8851 and MB8855 only

T-49-19-44

Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
-	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
$\overline{\quad}$ (Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviations	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
D	Direct data memory address (that is part of the instruction code)
$\overline{\text{IF}}$	Interrupt flag
imm	Immediate data
$\overline{\text{IRQ}}$	Interrupt request
K	K-Port (K3 to K0)
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
O	O-Port (O7 to O0)
OPLA	Output programmable logic array
P	P-Port (P3-P0)
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R15-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 15)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SB	Serial buffer register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high nibble
TL	Timer/counter low nibble
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit of X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 6: INSTRUCTION CODE SUMMARY

L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTC	*OUTP	OUT	TAY	TATH	TATL	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTHA	TTLA	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	JPA addr	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr								JPL addr							
7		(ICA)			AI imm											(DCA)
8	LYI imm															
9	(CLA)				LI imm											
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

Notes: : 1-byte/1-cycle instruction : 2-byte/2-cycle instruction

* MB8851 and MB8855 only

2

PRODUCT LINEUP AND DEVELOPMENT TOOLS

The MB8850 series consists of the MB8851/55, MB8852/56, and MB8854/58. The MB8850U1/U2 are available as piggyback EPROM evaluation devices. See Table 7

Table 7: MB8850 SERIES PRODUCT LINEUP & DEVELOPMENT TOOLS

	MB8851M/-PSH (MB8855M)	MB8852M/-PSH (MB8856M)	MB8854M/-PSH (MB8858M)	MB8850U1/U2-XXX-C *
ROM Size	2K x 8 bits (On-chip mask ROM	2K x 8 bits (On-chip mask ROM	1K x 8 bits (On-chip mask ROM	4K x 8 bits (Piggyback EPROM
RAM Size (Directly addressed locations)	128 x 4 bits (0-7)	128 x 4 bits (0-7)	64 x 4 bits (0-7)	128 x 4 bits (0-7)
I/O Port:	Total 37 lines	Total 25 lines	Total 25 lines	Total 37 lines
-Input only port	4	4	4	4
-Output only port	12	8	8	12
-I/O port	16	11	11	16
-Control port:	Total 5 lines	Total 2 lines	Total 2 lines	Total 5 lines
SI	Yes	No	No	Yes
SO	Yes	No	No	Yes
$\overline{SC}/\overline{TO}$	Yes	No	No	Yes
$\overline{IRQ}$	Yes	Yes	Yes	Yes
$\overline{RESET}$	Yes	Yes	Yes	Yes
Output Port Type of O-, P-, R-Port	· Standard pull-up · Standard open-drain (Mask option)	· Standard pull-up · Standard open-drain (Mask option)	· Standard pull-up · Standard open-drain (Mask option)	· Standard pull-up (411/412/413) · Standard open-drain (401/402/413) (Mask Option)
Output PLA Pattern	33 patterns · Dual 4-Bit parallel output · 8-bit PLA output (32 patterns)	33 patterns · Dual 4-Bit parallel output · 8-bit PLA output (32 patterns)	33 patterns · Dual 4-Bit parallel output · 8-bit PLA output (32 patterns)	· #001(401/411) · #002(402/411) · #003(403/411) (Mask option)
Stack Depth (Nesting level)	4 levels	4 levels	4 levels	4 levels
Timer/Counter:	Yes	Yes	Yes	Yes
-Buffer size	8 bits	8 bits	8 bits	8 bits
-Clock source	Internal/ External	Internal/ External	Internal/ External	Internal/ External
Serial I/O:	Yes	No	No	Yes
-Buffer size	4 bits	4 bits	4 bits	4 bits
-Clock source	Internal/ External	-	-	Internal/ External
-Output latch	Yes/No (Mask option)	-	-	Yes(U1)/No(U2) (Mask option)
Clock Generator:	Yes	Yes	Yes	Yes
-Oscillator type	· Crystal/ External	· Crystal/ External	· Crystal/ External	· Crystal/ RC-network/ External
-Clock frequency (With prescaler)	0.5MHz-2MHz (1MHz-4MHz)	0.5MHz-2MHz (1MHz-4MHz)	0.5MHz-2MHz (1MHz-4MHz)	0.5MHz-2MHz (1MHz-4MHz)

Table 7: MB8850 SERIES PRODUCT LINEUP & DEVELOPMENT TOOLS (Continued)

	MB8851M/-PSH (MB8855M)	MB8852M/-PSH (MB8856M)	MB8854M/-PSH (MB8858M)	MB8850U1/U2-XXXE-C*
Clock Prescaler (Divid-by-two)	Yes/No (Mask option)	Yes/No (Mask option)	Yes/No (Mask option)	Yes/No (Selected by external pin)
Interrupt Functions:	Yes	Yes	Yes	Yes
-Nesting level	Single level	Single level	Single level	Single level
-Interrupt sources	3 sources	3 sources	3 sources	3 sources
Standby Function:	· Yes/No (Mask option)	· Yes/No (Mask option)	· Yes/No (Mask option)	· Yes/No (Selectable by external pin)
-Initiation method	· Hardware	· Hardware	· Hardware	· Hardware
-Oscillator state during standby	· Idle	· Idle	· Idle	· Idle
-Output state during standby	· Hold	· Hold	· Hold	· Hold
-Standby off reset function	· No	· No	· No	· No
Instruction Set:				
-Number	70	69	69	70
-Length/cycle	1/1 or 2/2	1/1 or 2/2	1/1 or 2/2	1/1 or 2/2
Min. Instruction Execution Time	3µs at 2MHz (Without prescaler)	3µs at 2MHz (Without prescaler)	3µs at 2MHz (Without prescaler)	3µs at 2MHz (Without prescaler)
Power Supply	Single	Single	Single	Single +5V
Operating Temp. Range:				
-Standard Version	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
-A-, L-Version	-30°C to +70°C	-30°C to +70°C	-30°C to +70°C	-
Process	CMOS	CMOS	CMOS	CMOS
Package	· DIP-42P · SH-DIP-42P (· QFP-48P)	· DIP-28P · SH-DIP-28P (· QFP-48P)	· DIP-28P · SH-DIP-28P (· QFP-48P)	· MDIP-42P
Development tool:				
-Hardware	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-04 : EPROM writer (Common) MB2115-33A : DUE board			
-Software	SM05212-A010: Intellec series III MDS cross-assembler SM07412-A012: CP/M-86 cross-assembler SM0XXXX-AXXX: PC-DOS cross-assembler SM07412-G022: CP/M-86 host emulator SM0XXXX-GXXX: PC-DOS host emulator			

Notes:

* Suffix specifies OPLA pattern and output port type option, as follows:

Suffix	OPLA Pattern	Output Port Type
401E	#001	Standard pull-up
402E	#002	Standard pull-up
403E	#003	Standard pull-up
411E	#001	Standard open-drain
412E	#002	Standard open-drain
413E	#003	Standard open-drain

OUTPUT PLA (OPLA) PATTERN

OPLA #001 (Dual 4-bit parallel output)

CF	Accumulator AC3	AC2	AC1	AC0	O-Port Output 07	06	05	04	03	02	01	00	HEX	Note
0	0	0	0	0	X	X	X	X	0	0	0	0	F0	4-BIT PARALLEL OUTPUT
0	0	0	0	1	X	X	X	X	0	0	0	1	F1	
0	0	0	1	0	X	X	X	X	0	0	1	0	F2	
0	0	0	1	1	X	X	X	X	0	0	1	1	F3	
0	0	1	0	0	X	X	X	X	0	1	0	0	F4	
0	0	1	0	1	X	X	X	X	0	1	0	1	F5	
0	0	1	1	0	X	X	X	X	0	1	1	0	F6	
0	0	1	1	1	X	X	X	X	0	1	1	1	F7	
0	1	0	0	0	X	X	X	X	1	0	0	0	F8	
0	1	0	0	1	X	X	X	X	1	0	0	1	F9	
0	1	0	1	0	X	X	X	X	1	0	1	0	FA	
0	1	0	1	1	X	X	X	X	1	0	1	1	FB	
0	1	1	0	0	X	X	X	X	1	1	0	0	FC	
0	1	1	0	1	X	X	X	X	1	1	0	1	FD	
0	1	1	1	0	X	X	X	X	1	1	1	0	FE	
0	1	1	1	1	X	X	X	X	1	1	1	1	FF	
1	0	0	0	0	0	0	0	0	X	X	X	X	0F	4-BIT PARALLEL OUTPUT
1	0	0	0	1	0	0	0	1	X	X	X	X	1F	
1	0	0	1	0	0	0	1	0	X	X	X	X	2F	
1	0	0	1	1	0	0	1	1	X	X	X	X	3F	
1	0	1	0	0	0	1	0	0	X	X	X	X	4F	
1	0	1	0	1	0	1	0	1	X	X	X	X	5F	
1	0	1	1	0	0	1	1	0	X	X	X	X	6F	
1	0	1	1	1	0	1	1	1	X	X	X	X	7F	
1	1	0	0	0	1	0	0	0	X	X	X	X	8F	
1	1	0	0	1	1	0	0	1	X	X	X	X	9F	
1	1	0	1	0	1	0	1	0	X	X	X	X	AF	
1	1	0	1	1	1	0	1	1	X	X	X	X	BF	
1	1	1	0	0	1	1	0	0	X	X	X	X	CF	
1	1	1	0	1	1	1	0	1	X	X	X	X	DF	
1	1	1	1	0	1	1	1	0	X	X	X	X	EF	
1	1	1	1	1	1	1	1	1	X	X	X	X	FF	

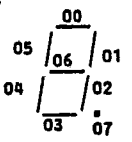
OPLA #002 (8-bit parallel for 8-segment LED/ dual 4-bit parallel output)

CF	Accumulator AC3	AC2	AC1	AC0	O-Port Output 07	06	05	04	03	02	01	00	HEX	Note
0	0	0	0	0	1	1	0	0	0	0	0	0	C0	8-SEGMENT DISPLAY
0	0	0	0	1	1	1	1	1	1	0	0	1	F9	
0	0	0	1	0	1	0	1	0	0	1	0	0	A4	
0	0	0	1	1	1	0	1	1	0	0	0	0	B0	
0	0	1	0	0	1	0	0	1	1	0	0	1	99	
0	0	1	0	1	1	0	0	1	0	1	0	0	92	
0	0	1	1	0	1	0	0	0	0	0	1	0	82	
0	0	1	1	1	1	1	1	1	1	0	0	0	F8	
0	1	0	0	0	1	0	0	0	0	0	0	0	80	
0	1	0	0	1	1	0	0	1	0	0	0	0	90	
0	1	0	1	0	1	0	0	0	1	0	0	0	88	
0	1	0	1	1	1	0	0	0	0	0	1	1	83	
0	1	1	0	0	1	1	0	0	0	1	1	0	C6	
0	1	1	0	1	1	0	1	0	0	0	0	1	A1	
0	1	1	1	0	1	0	0	0	0	1	1	0	86	
0	1	1	1	1	1	0	0	0	1	1	1	0	8E	
1	0	0	0	0	0	0	0	0	0	0	0	0	00	PARALLEL OUTPUT
1	0	0	0	1	0	0	0	1	0	0	0	1	11	
1	0	0	1	0	0	0	1	0	0	0	1	0	22	
1	0	0	1	1	0	0	1	1	0	0	1	1	33	
1	0	1	0	0	0	1	0	0	0	1	0	0	44	
1	0	1	0	1	0	1	0	1	0	1	0	1	55	
1	0	1	1	0	0	1	1	0	0	1	1	0	66	
1	0	1	1	1	0	1	1	1	0	1	1	1	77	
1	1	0	0	0	1	0	0	0	1	0	0	0	88	
1	1	0	0	1	1	0	0	1	1	0	0	1	99	
1	1	0	1	0	1	0	1	0	1	0	1	0	AA	
1	1	0	1	1	1	0	1	1	1	0	1	1	BB	
1	1	1	0	0	1	1	0	0	1	1	0	0	CC	
1	1	1	0	1	1	1	0	1	1	1	0	1	DD	
1	1	1	1	0	1	1	1	0	1	1	1	0	EE	
1	1	1	1	1	1	1	1	1	1	1	1	1	FF	Blank

OPLA #003 (8-bit parallel output for 8-segment LED)

CF	Accumulator AC3	AC2	AC1	AC0	O-Port Output 07	06	05	04	03	02	01	00	HEX	Note
0	0	0	0	0	1	1	0	0	0	0	0	0	C0	8-SEGMENT DISPLAY
0	0	0	0	1	1	1	1	1	1	0	0	1	F9	
0	0	0	1	0	1	0	1	0	0	1	0	0	A4	
0	0	0	1	1	1	0	1	1	0	0	0	0	B0	
0	0	1	0	0	1	0	0	1	1	0	0	1	99	
0	0	1	0	1	1	0	0	1	0	0	1	0	92	
0	0	1	1	0	1	0	0	0	0	0	1	0	82	
0	0	1	1	1	1	1	1	1	1	0	0	0	F8	
0	1	0	0	0	1	0	0	0	0	0	0	0	80	
0	1	0	0	1	1	0	0	1	0	0	0	0	90	
0	1	0	1	0	1	1	0	0	0	1	1	1	C7	
0	1	0	1	1	1	0	0	0	1	0	0	1	89	
0	1	1	0	0	1	0	0	0	1	1	0	0	8C	
0	1	1	0	1	1	0	0	0	1	0	0	0	88	
0	1	1	1	0	1	0	1	1	1	1	1	1	BF	
0	1	1	1	1	1	1	1	1	1	1	1	1	FF	Blank
1	0	0	0	0	0	1	0	0	0	0	0	0	40	8-SEGMENT DISPLAY
1	0	0	0	1	0	1	1	1	1	0	0	1	79	
1	0	0	1	0	0	0	1	0	0	1	0	0	24	
1	0	0	1	1	0	0	1	1	0	0	0	0	30	
1	0	1	0	0	0	0	0	1	1	0	0	1	19	
1	0	1	0	1	0	0	0	1	0	0	1	0	12	
1	0	1	1	0	0	0	0	0	0	0	1	0	02	
1	0	1	1	1	0	1	1	1	1	0	0	0	78	
1	1	0	0	0	0	0	0	0	0	0	0	0	00	
1	1	0	0	1	0	0	0	1	0	0	0	0	10	
1	1	0	1	0	1	0	1	0	0	1	1	1	A7	
1	1	0	1	1	1	0	1	1	0	0	1	1	B3	
1	1	1	0	0	1	0	0	1	1	1	0	1	9D	
1	1	1	0	1	1	0	0	1	0	1	1	0	96	
1	1	1	1	0	1	0	0	0	0	1	1	1	87	
1	1	1	1	1	0	1	1	1	1	1	1	1	7F	

Notes:



0 : Low (Light: Active low)
1 : High
X : Undefined. Data latched previously by OUTO instruction remains as it is.

STAMDARD VERSION ELECTRICAL CHARACTERISTICS

- ABSOLUTE MAXIMUM RATINGS(MB8851/52/54)†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-40		+85	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

- RECOMMENDED OPERATING CONDITIONS(MB8851/52/54)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Active operation range
		3.5		6.0	V	Standby operation range
	V_{SS}		0		V	
Input High Voltage	V_{IH}	0.8·V_{CC}		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.2·V_{CC}	V	
Operating Ambient Temperature	T_A	-40		+85	°C	

- **DC CHARACTERISTICS (MB8851/52/54)**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	O-, P-, R-Ports (Standard pull-up), $\overline{SC}/\overline{TO}$, SO	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
			V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	O-, P-, R-Ports (All output options), $\overline{SC}/\overline{TO}$, SO	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.2mA			0.6	V
Input Leakage Current	I_{IL}	R-Port(Standard pull-up), $\overline{SC}/\overline{TO}$, $\overline{TC}$(MB8852/54/56/58) $\overline{IRQ}$(MB8852/54/56/58)	V_{CC}=5.5V V_{IL}=0.4V		-1.2	-3.2	mA
		$\overline{EX}$, K-Port, SI, $\overline{RESET}$, $\overline{STBY}$, $\overline{TC}$(MB8851/55) $\overline{IRQ}$(MB8851/55)	V_{CC}=5.5V V_{IL}=0.4V		-20	-60	μA
Open-Drain Output Leakage Current	I_{LEAK}	O-, P-, R-Ports (Standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V Output in high-Z		0.1	40	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.), 5.5V(Max.) fc=1MHz(Active), All outputs open		2	6	mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=3.5V to 6.0V fc=0(Standby), All outputs open		10	100	μA
Input Capacitance	C_{IN}	All pins except V_{CC} and V_{SS}	fc=1MHz		10	20	pF

- **AC CHARACTERISTICS**

CLOCK TIMING(MB8851/52/54)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_c	EX, X	Crystal/ceramic OSC or external clock drive: Fig. 6 and 7	0.5	2	MHz	Without prescaler
				1	4		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Fig. 6 and 7	0.5	2.0	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open): Fig. 6 and 7	225		ns	Without prescaler
				100			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open): Fig. 6 and 7	5	100	ns	

Fig. 6: CLOCK TIMING

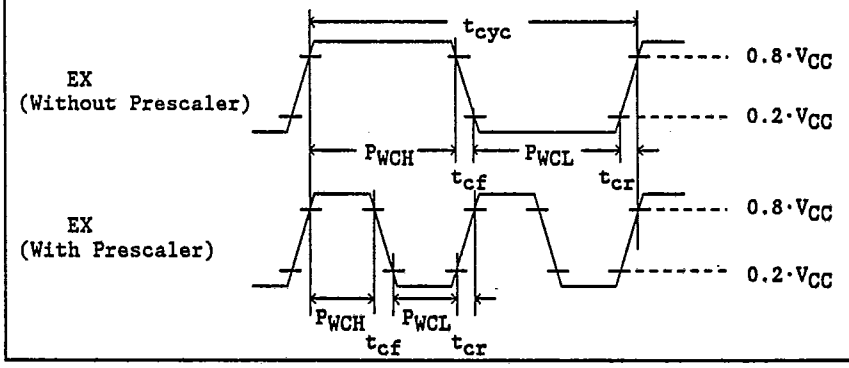
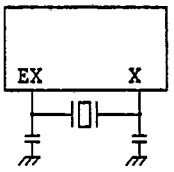


Fig. 7: CLOCK CIRCUIT CONFIGURATIONS

(1) Crystal/Ceramic Oscillator



(2) External Clock Drive

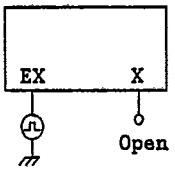
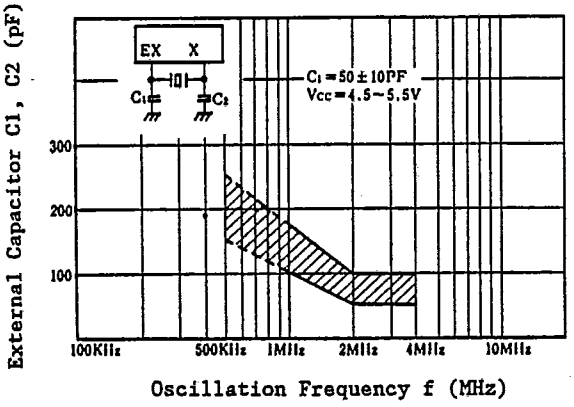


Fig. 8: CRYSTAL OSCILLATOR CHARACTERISTICS (EXAMPLE)
for MB8851/52/54)



Notes:

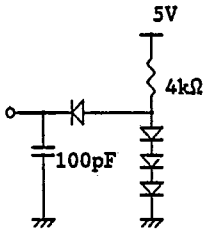
1) The cross-hatched portion is an area where the on-chip oscillator has stable characteristics and short stabilization time when a average crystal resonator is used. This chart gives an target value of the external capacitor to realize a desired frequency. When an exact frequency is needed, capacitor value should be determined, adjusting to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend a high-frequency crystal resonator with on-chip 1/2 prescaler.

OUTPUT TIMING(MB8851/52/54)
(Recommended operating conditions unless otherwise noted.)

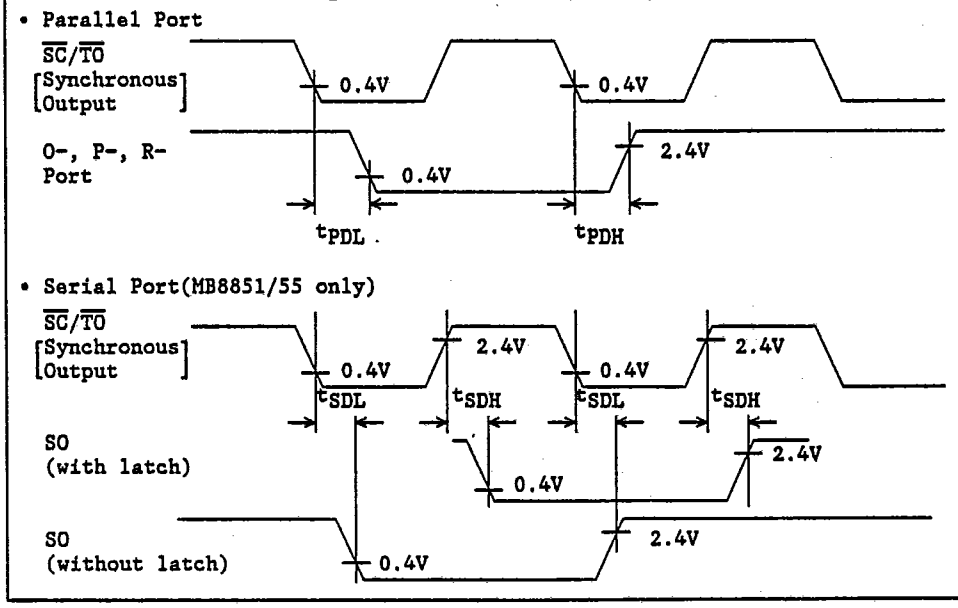
Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
O-, P-, R-Port Delay Time	t_{PDH}	O-, P-, R-Port	Fig. 9		1000	ns
	t_{PDL}				350	
Serial Port Delay Time (MB8851/55)	t_{SDH}	SO	Fig. 9		1000	ns
	t_{SDL}				350	

Notes:
1. A 5kΩ pull-up is required when open-drain output is used.
2. All the output loading values are 100pF + 1TTL. See figure below.



2

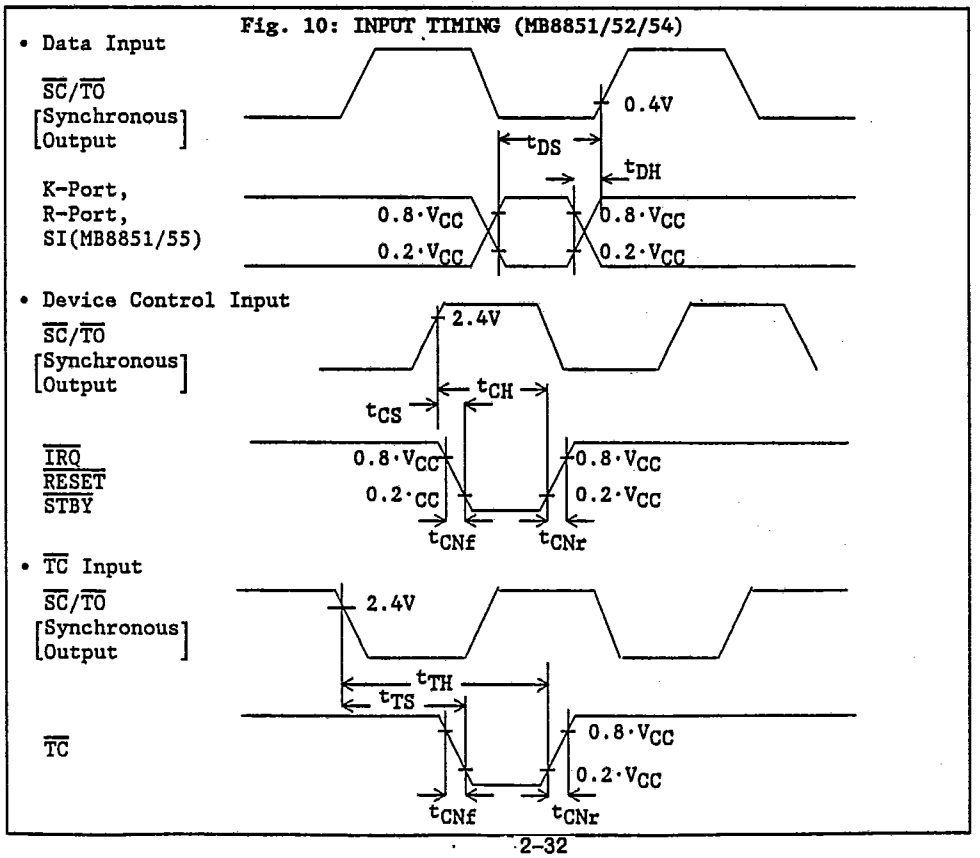
Fig. 9: OUTPUT TIMING(MB8851/52/54)



INPUT TIMING(MB8851/52/54)
(Recommended operating conditions unless otherwise noted.) T-49-19-44

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	K-Port, R-Port, SI(MB8851/55)	Fig. 10	$t_{cyc}+1000$		ns
Input Data Hold Time	t_{DH}				$t_{cyc}-50$	
Device Control Setup Time	t_{CS}	$\overline{RESET}$, $\overline{STBY}$	Fig. 10		$2t_{cyc}-200$	ns
		$\overline{IRQ}$			$t_{cyc}-200$	
Device Control Hold Time	t_{CH}	$\overline{RESET}$, $\overline{STBY}$	Fig. 10	$2t_{cyc}+50$		ns
		$\overline{IRQ}$		$t_{cyc}+50$		
Timing Input Setup Time	t_{TS}	$\overline{TC}$	Fig. 10		$2t_{cyc}-200$	ns
Timing Input Hold Time	t_{TH}	$\overline{TC}$	Fig. 10	$2t_{cyc}+50$		ns
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	$\overline{STBY}$, $\overline{IRQ}$, $\overline{RESET}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$ (MB8851/55)	Fig. 10	Should be less than 200ns		

Fig. 10: INPUT TIMING (MB8851/52/54)



A-VERSION ELECTRICAL CHARACTERISTICS

- ABSOLUTE MAXIMUM RATINGS(MB8851A/52A/54A)†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-30		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

- RECOMMENDED OPERATING CONDITIONS(MB8851A/52A/54A)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	3.5		6.0	V	Active operation range
		3.0		6.0	V	Standby operation range
	V_{SS}		0		V	
Input High Voltage	V_{IH}	0.8·V_{CC}		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.2·V_{CC}	V	
Operating Ambient Temperature	T_A	-30		+70	°C	

- **DC CHARACTERISTICS (MB8851A/52A/54A)**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	O-, P-, R-Ports (Standard pull-up), SC/TO, SO	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
			V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	O-, P-, R-Ports (All output options), SC/TO, SO	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.2mA			0.6	V
Input Leakage Current	I_{IL}	R-Port(Standard pull-up), SC/TO, TC(MB8852A/54A/56A/58A) IRQ(MB8852A/54A/56A/58A)	V_{CC}=5.5V V_{IL}=0.4V		-1.2	-3.2	mA
		EX, K-Port, SI, RESET, STBY, TC(MB8851A/55A) IRQ(MB8851A/55A)	V_{CC}=5.5V V_{IL}=0.4V		-20	-60	μA
Open-Drain Output Leakage Current	I_{LEAK}	O-, P-, R-Ports (Standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V Output in high-Z		0.1	40	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.), 5.5V(Max.) fc=1MHz(Active), All outputs open		2	6	mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=3.5V to 6.0V fc=0(Standby), All outputs open		10	100	μA
Input Capacitance	C_{IN}	All pins except V_{CC} and V_{SS}	fc=1MHz		10	20	pF

- **AC CHARACTERISTICS**

CLOCK TIMING(MB8851A/52A/54A)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_c	EX, X	Crystal/ceramic OSC or external clock drive: Fig. 11 and 12	0.5	2	MHz	Without prescaler
				1	4		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Fig. 11 and 12	0.5	2.0	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open): Fig. 11 and 12	225		ns	Without prescaler
				100			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open): Fig. 11 and 12	5	100	ns	

Fig. 11: CLOCK TIMING

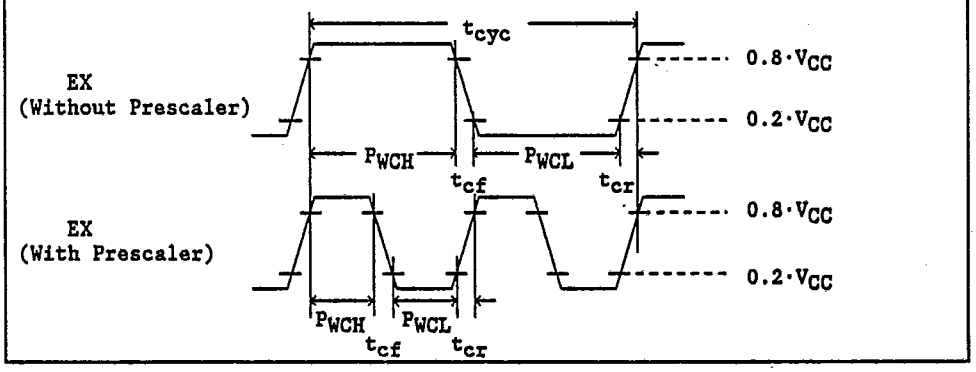
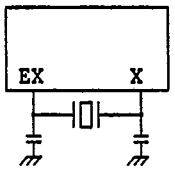


Fig. 12: CLOCK CIRCUIT CONFIGURATIONS

(1) Crystal/Ceramic Oscillator



(2) External Clock Drive

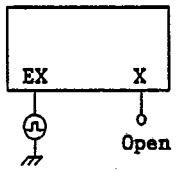
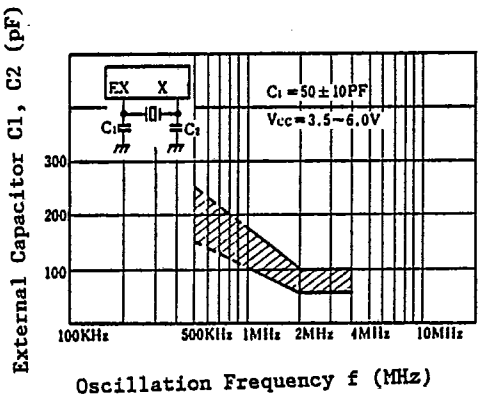


Fig. 13: CRYSTAL OSCILLATOR CHARACTERISTICS (EXAMPLE)
for MB8851A/52A/54A)



Notes:

1) The cross-hatched portion is an area where the on-chip oscillator has stable characteristics and short stabilization time when a average crystal resonator is used. This chart gives an target value of the external capacitor to realize a desired frequency. When an exact frequency is needed, capacitor value should be determined, adjusting to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend a high-frequency crystal resonator with on-chip 1/2 prescaler.

OUTPUT TIMING(MB8851A/52A/54A)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condi-tions	Value		Unit
				Min.	Max.	
O-, P-, R-Port Delay Time	t_{PDH}	O-, P-, R-Port	Fig. 14		1000	ns
	t_{PDL}				350	
Serial Port Delay Time (MB8851A/55A)	t_{SDH}	SO	Fig. 14		1000	ns
	t_{SDL}				350	

Notes:
1. A 5kΩ pull-up is required when open-drain output is used.
2. All the output loading values are 100pF + 1TTL. See figure below.

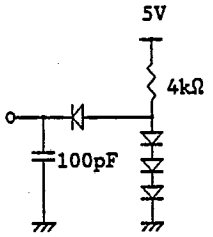


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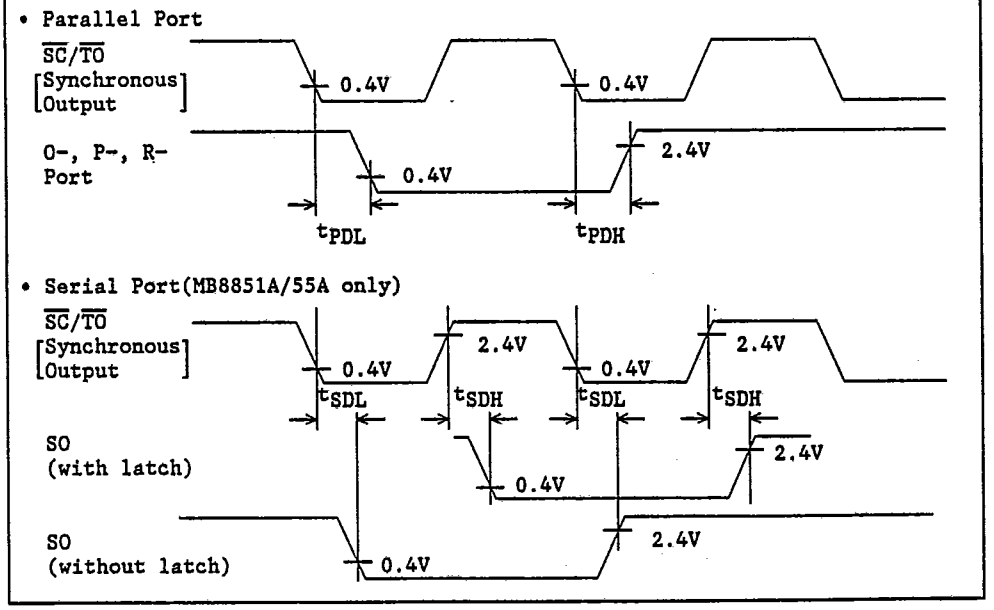
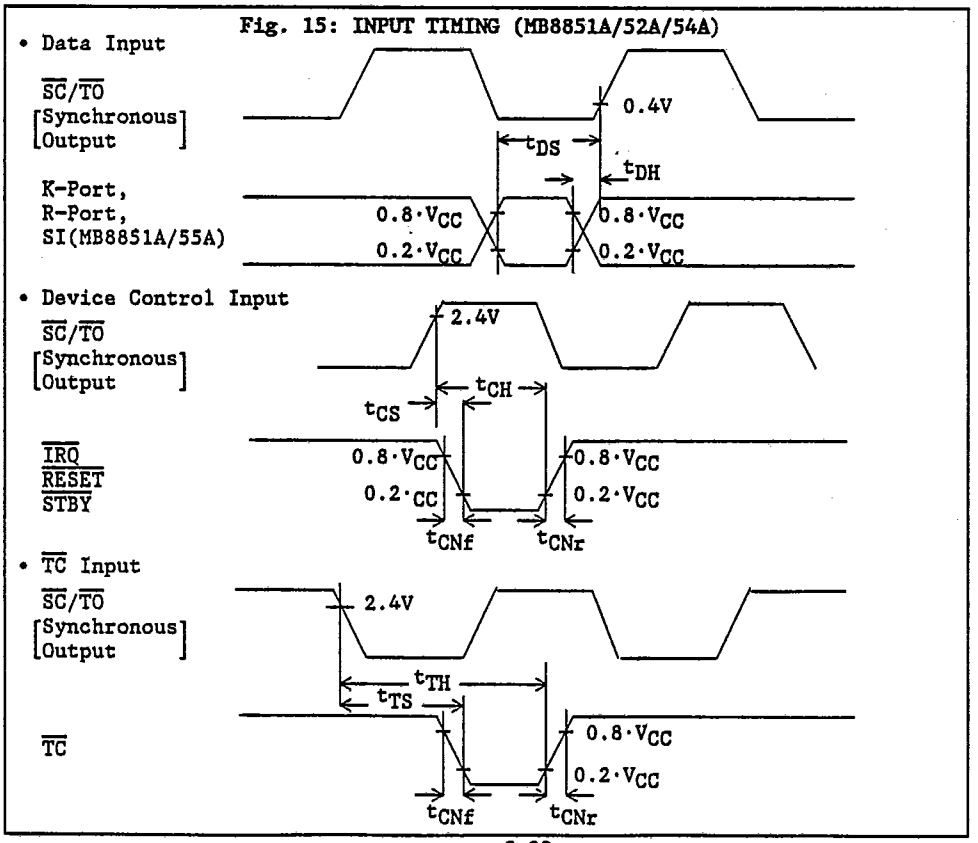
Fig. 14: OUTPUT TIMING(MB8851A/52A/54A)



INPUT TIMING(MB8851A/52A/54A)
(Recommended operating conditions unless otherwise noted.) T-49-19-44

Parameter	Symbol	Pin/Port	Conditions	Value Min.	Value Max.	Unit
Input Data Setup Time	t_{DS}	K-Port, R-Port, SI(MB8851A/55A)	Fig. 15	t_{cyc}+1000		ns
Input Data Hold Time	t_{DH}				t_{cyc}-50	
Device Control Setup Time	t_{CS}	$\overline{RESET}$, $\overline{STBY}$	Fig. 15		$2t_{cyc}$-200	ns
		$\overline{IRQ}$			t_{cyc}-200	
Device Control Hold Time	t_{CH}	$\overline{RESET}$, $\overline{STBY}$	Fig. 15	$2t_{cyc}$+50		ns
		$\overline{IRQ}$		t_{cyc}+50		
Timing Input Setup Time	t_{TS}	$\overline{TC}$	Fig. 15		$2t_{cyc}$-200	ns
Timing Input Hold Time	t_{TH}	$\overline{TC}$	Fig. 15	$2t_{cyc}$+50		ns
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	$\overline{STBY}$, $\overline{IRQ}$, $\overline{RESET}$, $\overline{TC}$, $\overline{SC/TO}$ (MB8851A/55A)	Fig. 15	Should be less than 200ns		

Fig. 15: INPUT TIMING (MB8851A/52A/54A)



L-VERSION ELECTRICAL CHARACTERISTICS

• **ABSOLUTE MAXIMUM RATINGS(MB8851L/52L/54L)†**

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
	V_{SS}		0		V	
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-30		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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• **RECOMMENDED OPERATING CONDITIONS(MB8851L/52L/54L)**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	2.5		4.0	V	Active operation range
		2.0		4.0	V	Standby operation range
	V_{SS}		0		V	
Input High Voltage	V_{IH}	0.8·V_{CC}		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.2·V_{CC}	V	
Operating Ambient Temperature	T_A	-30		+70	°C	

- **DC CHARACTERISTICS (MB8851L/52L/54L)**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	O-, P-, R-Ports (Standard pull-up), $\overline{SC}/\overline{TO}$, SO	V_{CC}=3.0V I_{OH}=-10μA	2.7	2.95		V
Output Low Voltage	V_{OL}	O-, P-, R-Ports (All output options), $\overline{SC}/\overline{TO}$, SO	V_{CC}=3.0V I_{OL}=400μA		0.1	0.3	V
Input Leakage Current	I_{IL}	R-Port(Standard pull-up), $\overline{SC}/\overline{TO}$, $\overline{TC}$(MB8852L/54L/56L/58L) $\overline{IRQ}$(MB8852L/54L/56L/58L)	V_{CC}=4.0V V_{IL}=0.3V		-0.8	-2.4	mA
		$\overline{EX}$, K-Port, SI, $\overline{RESET}$, $\overline{STBY}$, $\overline{TC}$(MB8851L/55L) $\overline{IRQ}$(MB8851L/55L)	V_{CC}=4.0V V_{IL}=0.3V		-15	-40	μA
Open-Drain Output Leakage Current	I_{LEAK}	O-, P-, R-Ports (Standard open-drain)	V_{CC}=4.0V V_{OH}=4.0V Output in high-Z		0.1	40	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=3.0V(Typ.), 4.0V(Max.) fc=500kHz(Active), All outputs open		0.6	3.0	mA
	I_{CCH}	V_{CC}	V_{CC}=3.0V fc=0(Standby), All outputs open		10	100	μA
Input Capacitance	C_{IN}	All pins except V_{CC} and V_{SS}	fc=500kHz		10	20	pF

- **AC CHARACTERISTICS**

CLOCK TIMING(MB8851L/52L/54L)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_c	EX, X	Crystal/ceramic OSC or external drive: Fig. 16 and 17	0.4	0.8	MHz	Without prescaler
				0.8	1.6		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Fig. 16 and 17	1.25	2.5	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open): Fig. 16 and 17	500		ns	Without prescaler
				250			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open): Fig. 16 and 17	5	200	ns	

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Fig. 16: CLOCK TIMING

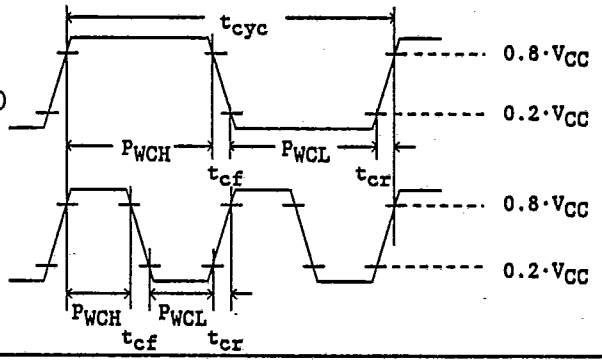
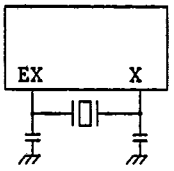


Fig. 17: CLOCK CIRCUIT CONFIGURATIONS

(1) Crystal/Ceramic Oscillator



(2) External Clock Drive

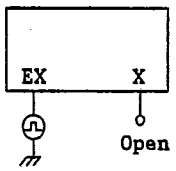
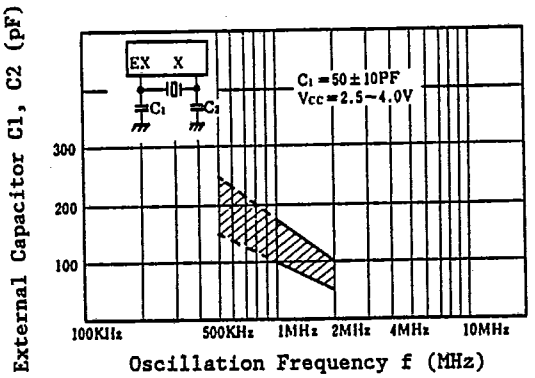


Fig. 18: CRYSTAL OSCILLATOR CHARACTERISTICS (EXAMPLE)
for MB8851L/52L/54L)



Notes:

1) The cross-hatched portion is an area where the on-chip oscillator has stable characteristics and short stabilization time when a average crystal resonator is used. This chart gives an target value of the external capacitor to realize a desired frequency. When an exact frequency is needed, capacitor value should be determined, adjusting to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend a high-frequency crystal resonator with on-chip 1/2 prescaler.

OUTPUT TIMING(MB8851L/52L/54L)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
O-, P-, R-Port Delay Time	t_{PDH}	O-, P-, R-Port	Fig. 19		2000	ns
	t_{PDL}				700	
Serial Port Delay Time (MB8851L/55L)	t_{SDH}	SO	Fig. 19		2000	ns
	t_{SDL}				700	

Notes:
1. A 5kΩ pull-up is required when open-drain output is used.
2. All the output loading values are as figure below.

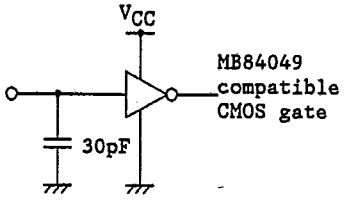


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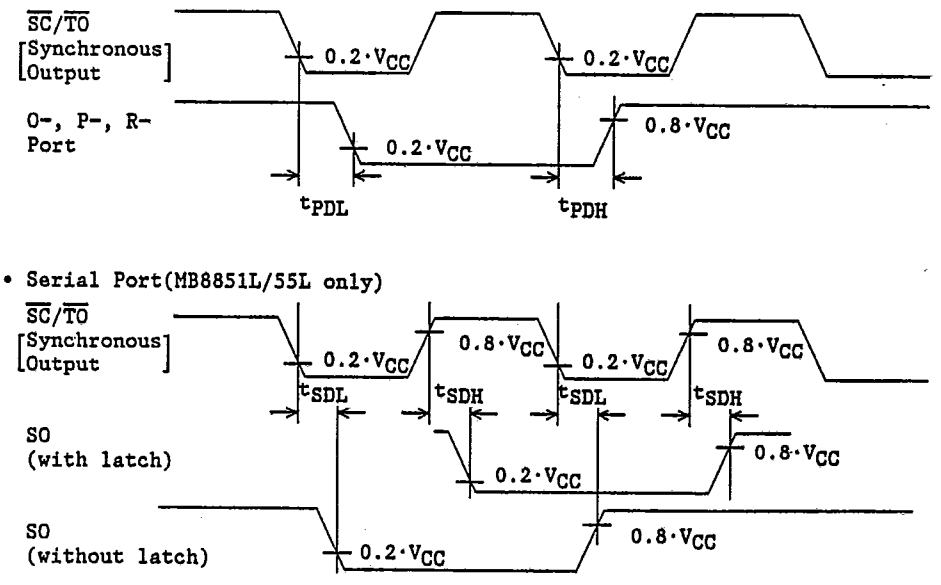
Fig. 19: OUTPUT TIMING(MB8851L/52L/54L)



INPUT TIMING(MB8851L/52L/54L)
(Recommended operating conditions unless otherwise noted.)

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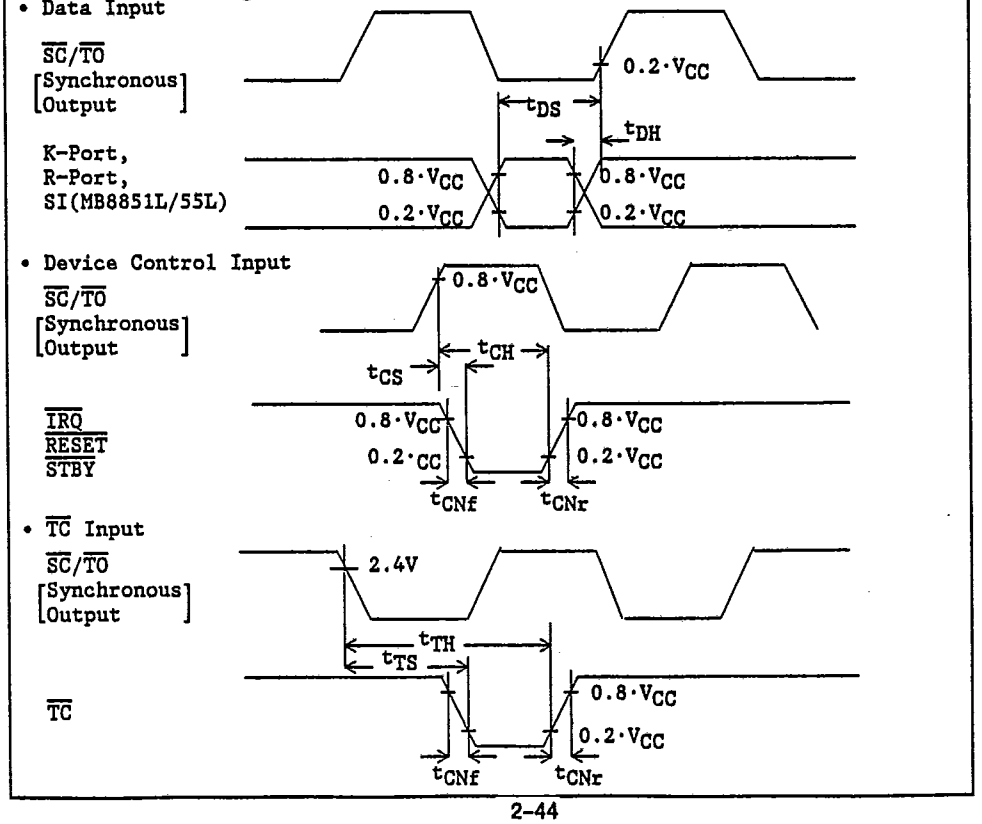
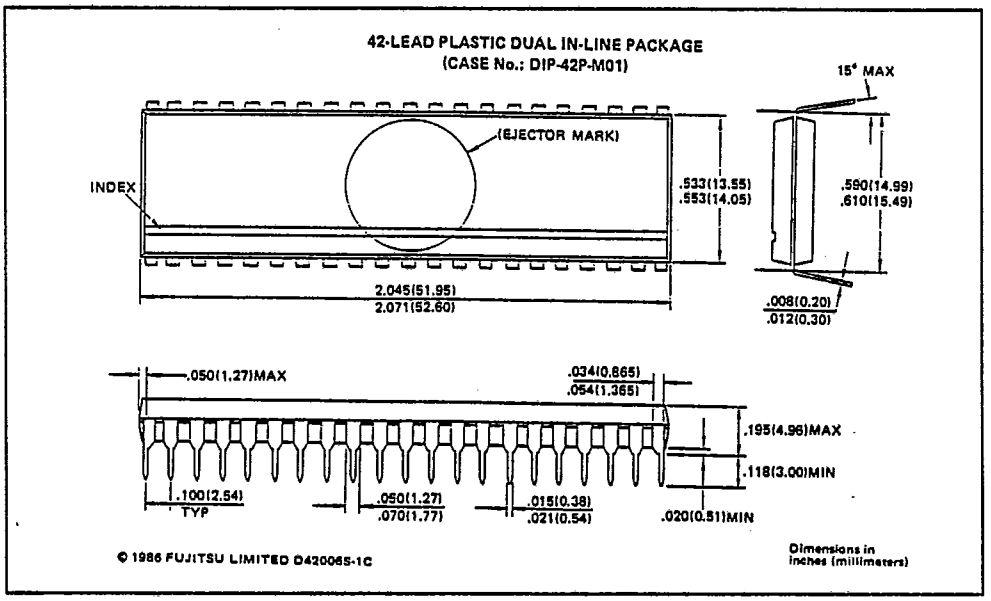
Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	K-Port, R-Port, SI(MB8851L/55L)	Fig. 20	t_{cyc}+2000		ns
Input Data Hold Time	t_{DH}				t_{cyc}-100	
Device Control Setup Time	t_{CS}	$\overline{RESET}$, $\overline{STBY}$	Fig. 20		$2t_{cyc}$-400	ns
		$\overline{IRQ}$			t_{cyc}-400	
Device Control Hold Time	t_{CH}	$\overline{RESET}$, $\overline{STBY}$	Fig. 20	$2t_{cyc}$+100		ns
		$\overline{IRQ}$		t_{cyc}+100		
Timing Input Setup Time	t_{TS}	$\overline{TC}$	Fig. 20		$2t_{cyc}$-400	ns
Timing Input Hold Time	t_{TH}	$\overline{TC}$	Fig. 20	$2t_{cyc}$+100		ns
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	$\overline{STBY}$, $\overline{IRQ}$, $\overline{RESET}$, $\overline{TC}$, $\overline{SC/TO}$ (MB8851L/55L)	Fig. 20	Should be less than 200ns		

Fig. 20: INPUT TIMING (MB8851L/52L/54L)

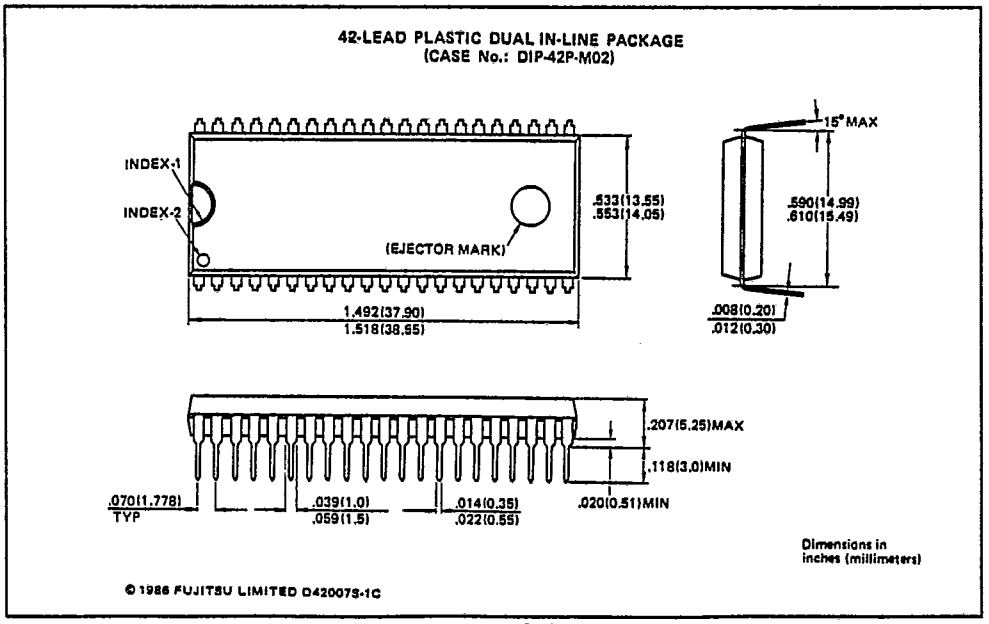


PACKAGE DIMENSIONS

• MB8851M/AM/LM: 42-PIN PLASTIC STANDARD DIP

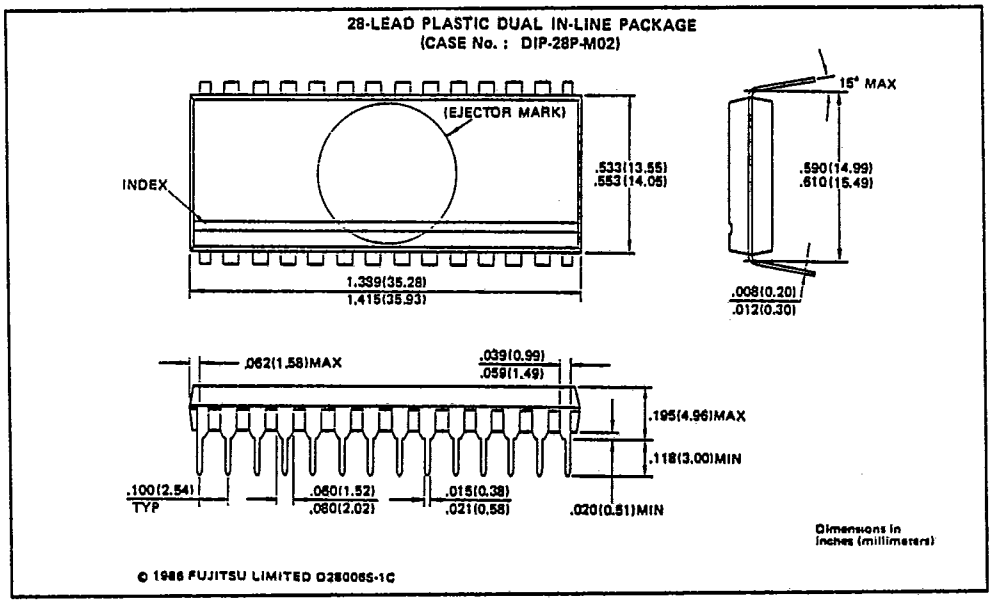


• MB8851-PSH/A-PSH/L-PSH: 42-PIN PLASTIC SHRINK DIP

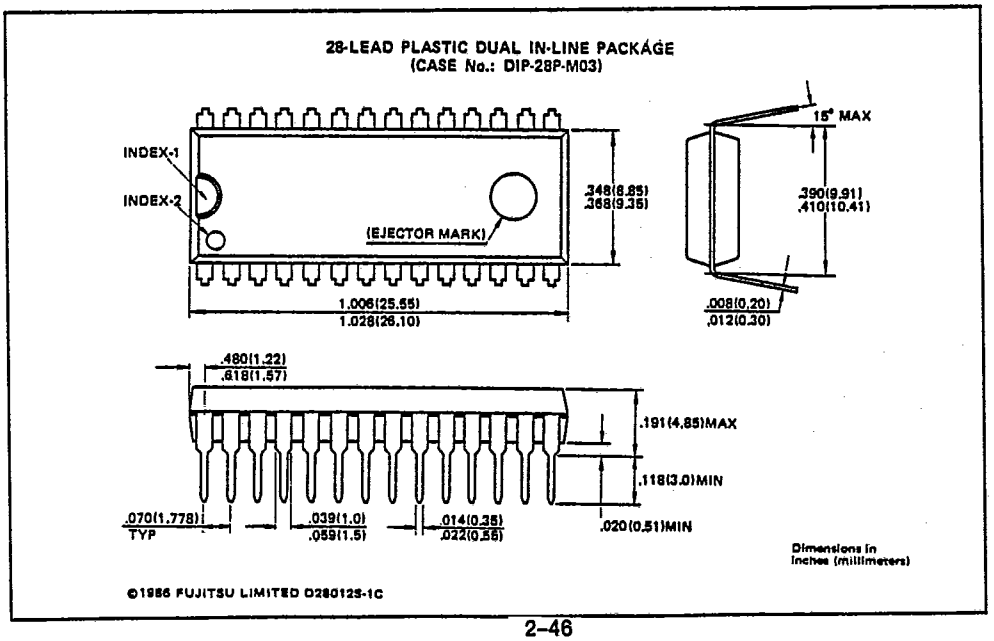


PACKAGE DIMENSIONS

- MB8852M/54M, MB8852AM/54AM, & MB8852LM/54LM: 28-PIN PLASTIC STANDARD DIP

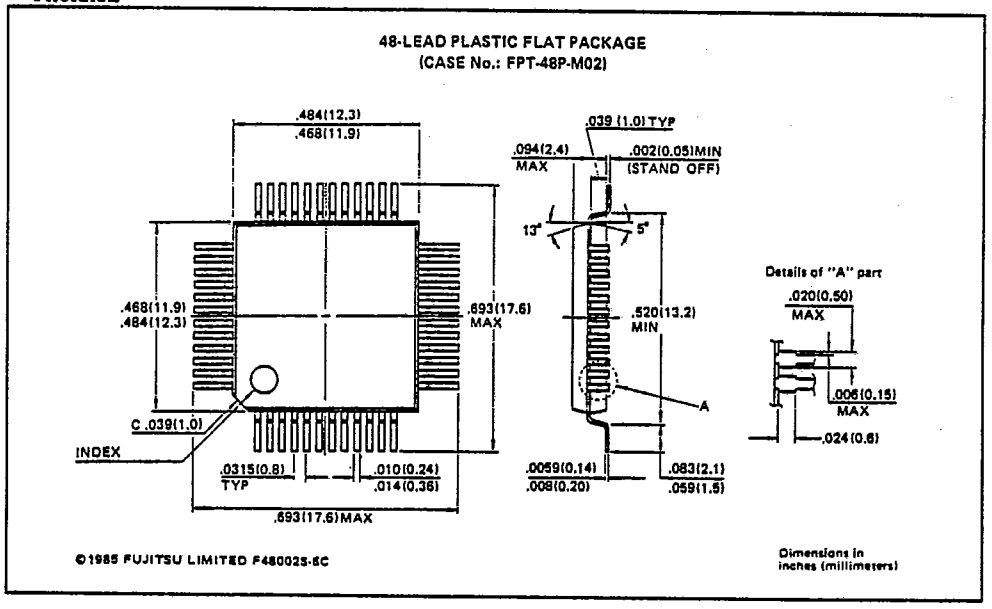


- MB8852-PSH/54-PSH, MB8852A-PSH/54A-PSH, & MB8852L-PSH/54L-PSH: 28-PIN PLASTIC SHRINK DIP

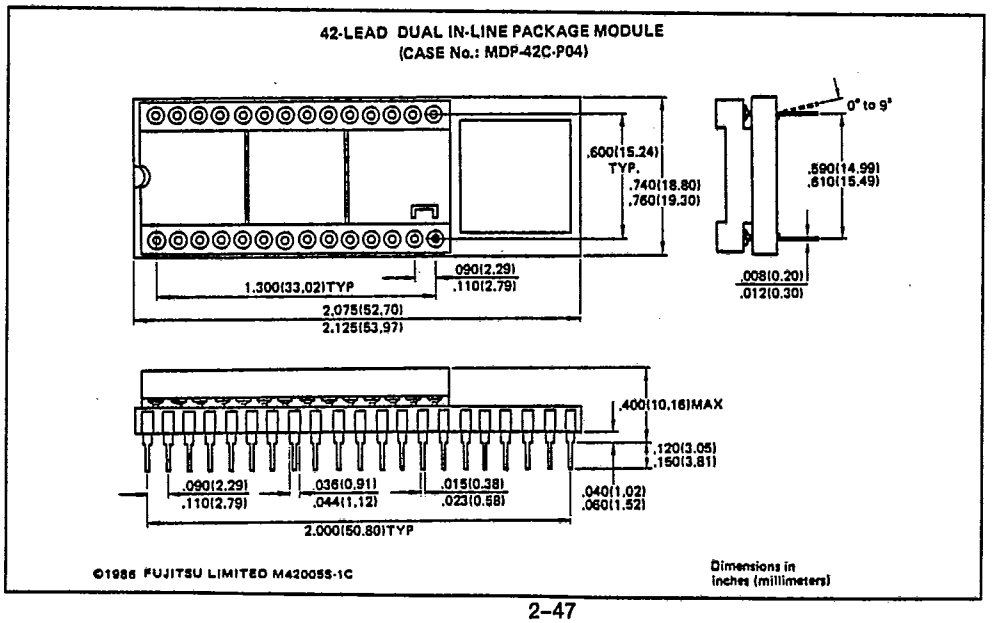


PACKAGE DIMENSIONS(Continues)

- MB8855M/56M/58M, MB8855AM/56AM/58AM, & MB8855LM/56LM/58LM: 48-PIN PLASTIC FLAT PACKAGE



- MB8850U1/U2-C: 42-PIN CERAMIC MODULE



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