MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

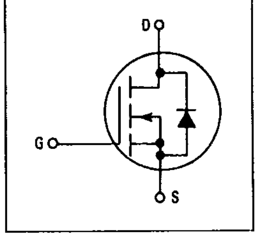
MTM15N05L
MTM15N06L
MTP15N05L
MTP15N06L

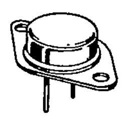
Designer's Data Sheet
Power Field Effect Transistors
N-Channel Enhancement-Mode Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

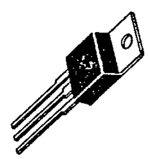
- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
LOGIC LEVEL
15 AMPERES
$r_{DS(on)}$ = 0.15 OHM
50 and 60 VOLTS





MTM15N05L
MTM15N06L
CASE 1-04
TO-204AA



MTP15N05L
MTP15N06L
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM15N05L MTP15N05L	MTM15N06L MTP15N06L	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±15 ±20		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 40		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient MTM15N05L/06L MTP15N05L/06L	$R_{\theta JA}$	30 62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA) MTM/MTP15N05L MTM/MTP15N06L	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)		$V_{GS(th)}$	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3 1.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	900	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 4		—	2800	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	200	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 4		—	2400	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 4	C_{oss}	—	450	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 7.5 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	260	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 15 A, V_{GS} = 5 Vdc) See Figures 6 and 10.	Q_g	14 (typ)	22	nC
Gate-Source Charge		Q_{gs}	7 (typ)	—	
Gate-Drain Charge		Q_{gd}	7 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figures 14 and 15.	V_{SD}	1.8 (typ)	—	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and center of the die.)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad.)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

TYPICAL CHARACTERISTICS

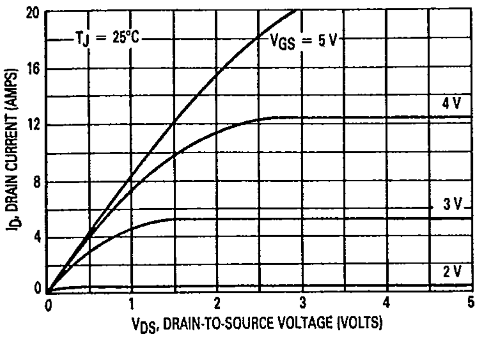


Figure 1. On-Region Characteristics

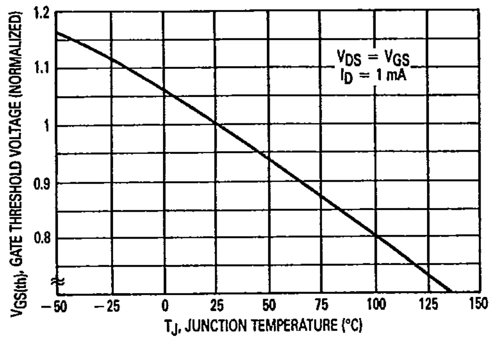


Figure 2. Gate-Threshold Voltage Variation With Temperature

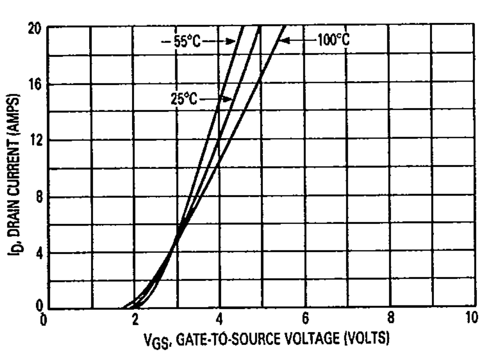


Figure 3. Transfer Characteristics

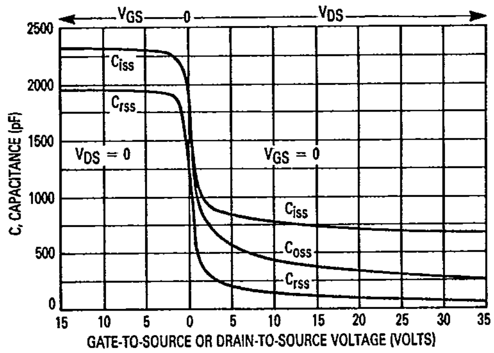


Figure 4. Capacitance Variation

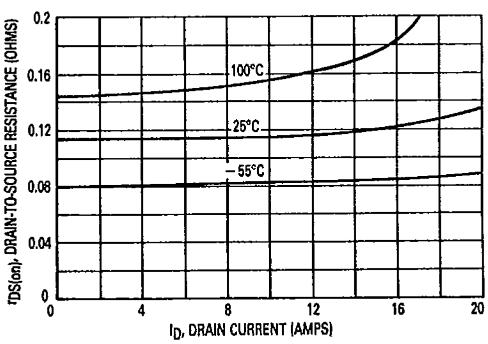


Figure 5. On-Resistance versus Drain Current

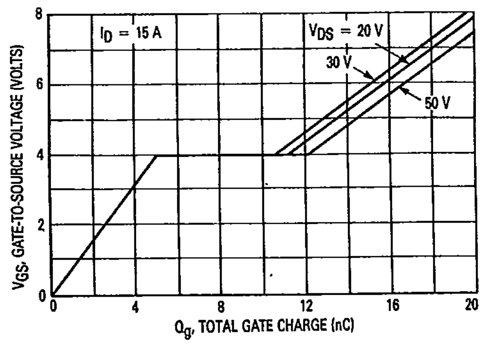


Figure 6. Gate Charge Variation

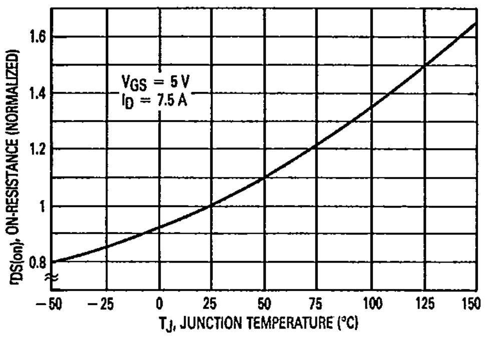


Figure 7. On-Resistance Variation with Temperature

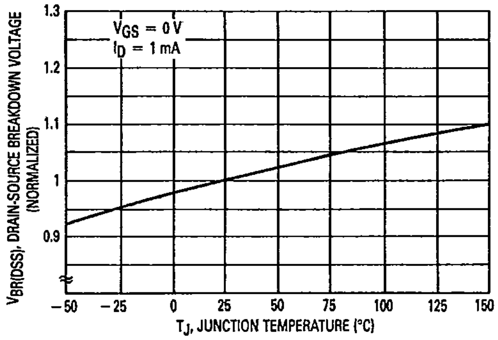


Figure 8. Drain-Source Breakdown Voltage Variation with Temperature

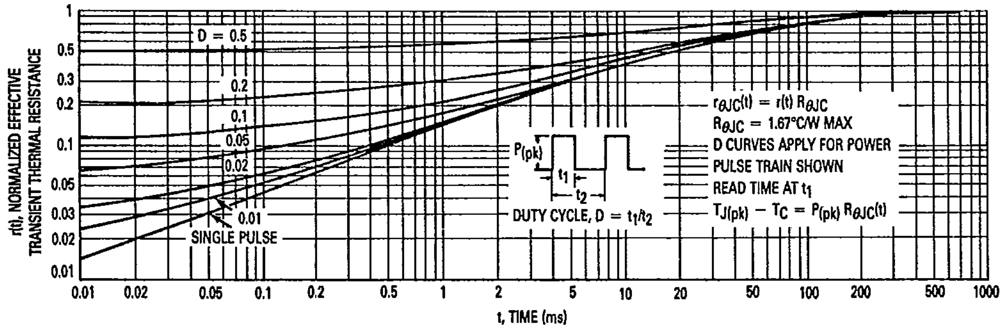
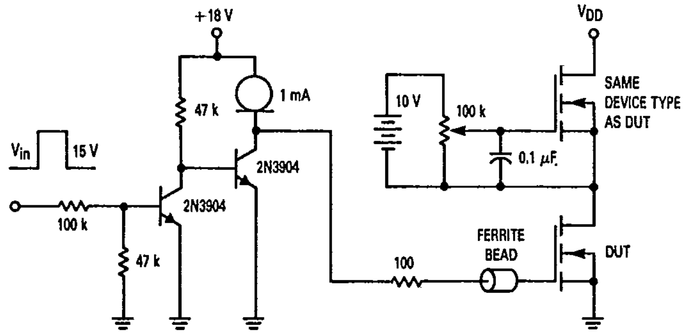


Figure 9. Thermal Response



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

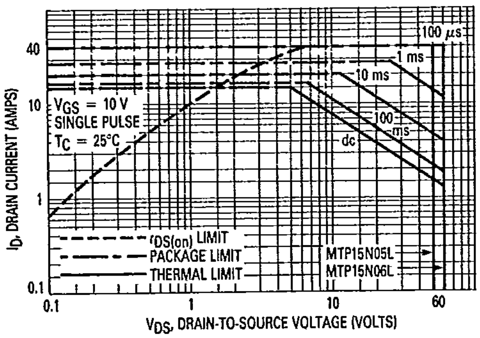


Figure 11. Maximum Rated Forward Biased Safe Operating Area

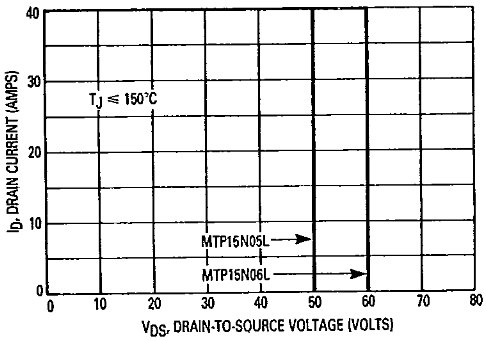
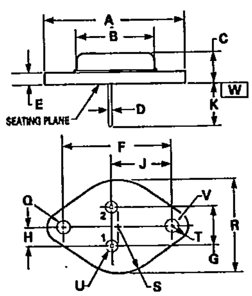


Figure 12. Maximum Rated Switching Safe Operating Area

OUTLINE DIMENSIONS

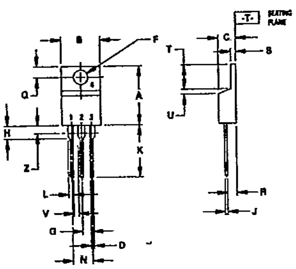


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 3.
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ ϕ 0.25 (0.010) Ⓜ W V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ ϕ 0.30 (0.012) Ⓜ W V Ⓜ Q Ⓜ

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB