RF2175

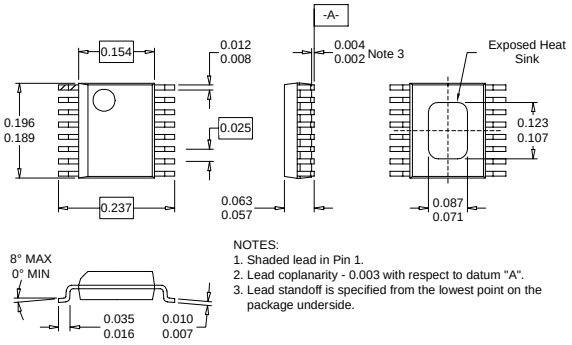
3V 400MHZ LINEAR AMPLIFIER

Typical Applications

- 3V TETRA Cellular Handsets
- 3V CDMA Cellular Handsets
- Portable Battery-Powered Equipment

Product Description

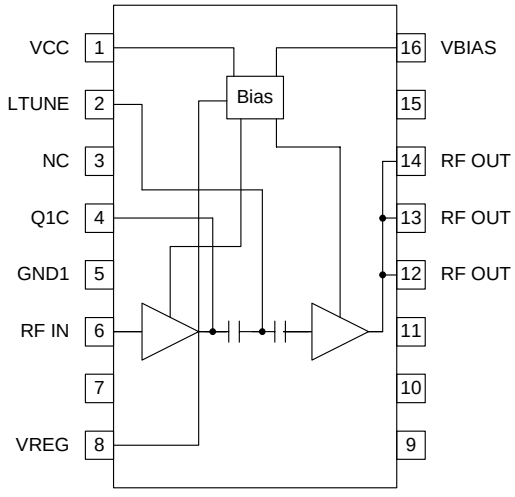
The RF2175 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in TETRA hand-held digital cellular equipment, spread-spectrum systems, and other applications in the 380MHz to 512MHz band. The RF2175 has an analog bias control voltage to maximize efficiency. The device is self-contained with 50Ω input, and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics. The package is a small SSOP-16 plastic with backside ground.



Package Style: SSOP-16 Slug

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 31.8dBm Linear Output Power
- 37.5dB Linear Gain
- 30% Linear Efficiency
- On-Board Power Down Mode
- 380MHz to 512MHz Operation

Ordering Information

RF2175	3V 400MHz Linear Amplifier
RF2175 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF Off)	+8.0	V_{DC}
Supply Voltage (RF Applied)	+4.5	V_{DC}
Mode Voltage (V_{BIAS})	+5.0	V_{DC}
Control Voltage (V_{REG})	+5.0	V_{DC}
Input RF Power (Avg.)	+5	dBm
Output VSWR - Inband	6:1	
Output VSWR - Out of Band	20:1	
Operating Ambient Temperature	-30 to +100	°C
Storage Temperature	-40 to +120	°C
Moisture Sensitivity	JEDEC Level 5 *	

Caution! ESD sensitive device.

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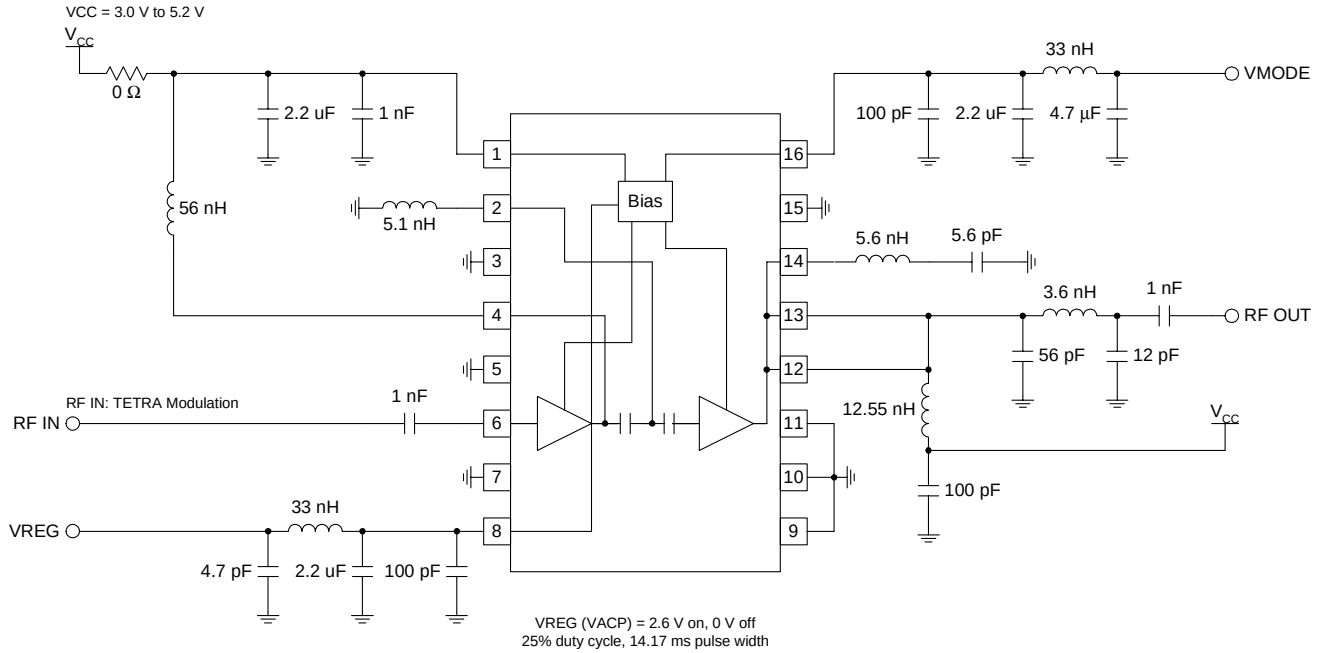
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=410MHz to 420MHz unless otherwise specified, 25% duty cycle. P_{OUT}=31.8dBm
Usable Frequency Range	380		512	MHz	
Typical Frequency Range		410 to 420		MHz	
Linear Gain	35.0	37.5	39.0	dB	
Harmonic			-30	dBc	
P3dB Output Power	34			dBm	
Linear Output Power (TETRA Modulation)	31.8			dBm	
Total Linear Efficiency	25	30		%	
Adjacent Channel Power Rejection	-35			dBc	ACPR@25kHz, TETRA modulation
	-45			dBc	ACPR@50kHz, TETRA modulation
Power Supply					
Power Supply Voltage	3.0	3.6	4.5	V	
Idle Current		230	300	mA	All V_{CC} pins, no RF input.
V_{CC} Current			1650	mA	All V_{CC} pins, P_{OUT}=31.8dBm
V_{REG} Current			13	mA	Pin 8
V_{BIAS} Current			3	mA	Pin 16
Turn On/Off Time			<150	µs	Time for power to rise to 95% of its final value. Measured with 4.7µF and 2.2µF capacitors on both V_{REG} and V_{BIAS} lines.
Total Current (Power Down)			10	µA	V_{REG}=Low
V_{REG} "Low" Voltage		0	0.2	V	
V_{REG} "High" Voltage	2.7	2.8	2.9	V	
V_{BIAS} Control Voltage Range		2.8	2.9	V	

* The RF2175 is considered JEDEC Level 5 for moisture sensitivity with a maximum peak reflow temperature of 220°C. To assure reliable performance, this part must be handled in accordance with JEDEC specifications for a Level 5 part.

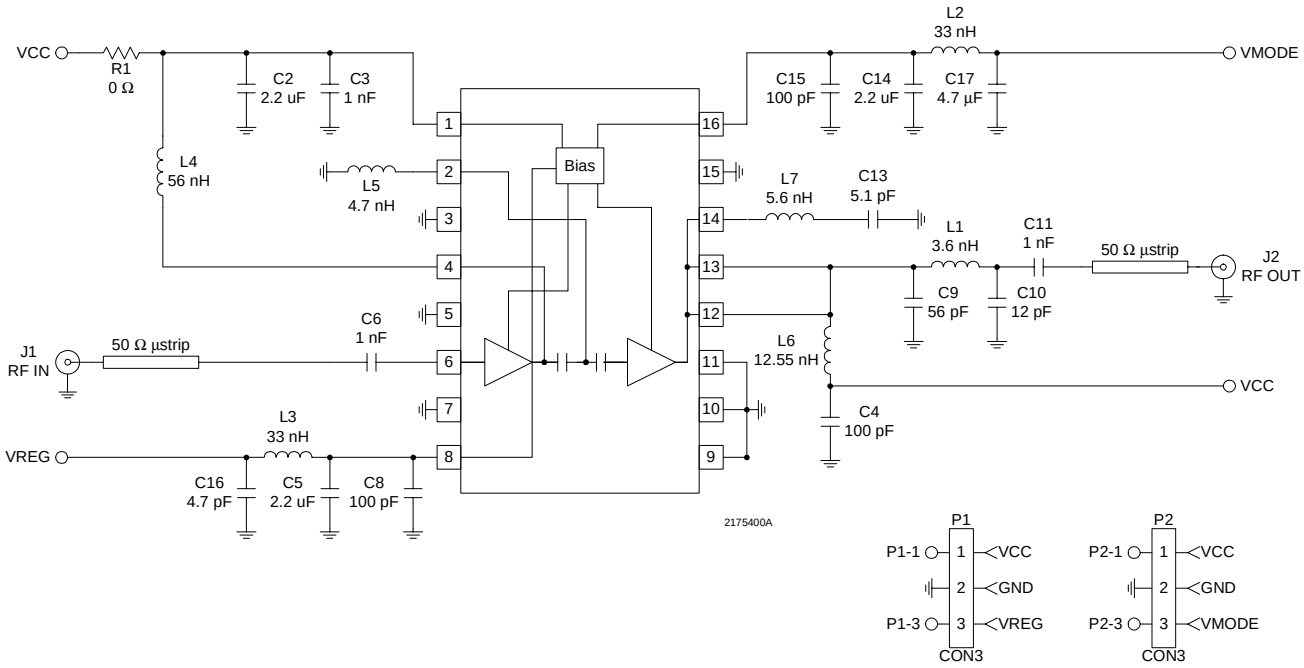
Pin	Function	Description	Interface Schematic
1	VCC	Power supply for input bias circuitry. A 1nF high frequency bypass capacitor is recommended.	
2	L TUNE	Interstage Tuning. A shunt inductor to GND is required to optimize the match.	
3	NC	No connection.	
4	Q1C	Power supply for stage 1. V_{CC} should be fed through a 25nH or greater inductor with a decoupling capacitor on the V_{CC} side.	
5	GND1	Ground for stage 1. For best performance, keep traces physically short and connect immediately to ground plane. This ground should be isolated from the backside ground contact.	
6	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
7	NC	No connection.	
8	VREG	Power Down control. When this pin is “low”, all circuits are shut off. When this pin is 2.8V, all circuits are operating normally. V_{PD} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 100pF high frequency bypass capacitor is recommended.	
9	NC	No connection.	
10	NC	No connection.	
11	NC	No connection.	
12	RF OUT	RF output and power supply for the output stage. The bias for the output stage is provided through this pin and pin 13. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
13	RF OUT	Same as pin 12.	
14	RF OUT	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with a shunt capacitor at $2f_0$ is connected to this pin.	
15	NC	No connection.	
16	VBIAS	The bias pin allows higher efficiency in low power power modes. When operating at full output, VBIAS should be 2.8V.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad, which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic
380MHz



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.028”, Board Material FR-4