TOSHIBA

TC220C/E DRAM Core

0.3µm 3T dRAMASIC

Toshiba's 1 Mbit embedded DRAM core is available for the TC220C and TC220E product families. Each DRAM cell is based on a three transistor structure as shown in Figure 1. This multi-feature DRAM core is easily integrated into a broad range of applications through utilization of different core configurations.

DRAM Core Features

- Power supply: 3.3V ±0.3V
- Memory configurations
  - 128K x 8 bit
  - 64K x 16 bit
  - 32K x 32 bit
  - 16K x 64 bit
- Full address without multiplex
- Separate data input and output
- Read access modes
  - Random access
  - EDO/Hyper page mode
- Refresh scheme
  - $\overline{RAS}$ only refresh
  - CBR ($\overline{CAS}$ before $\overline{RAS}$) refresh
- Performance specification
  - trc random read cycle: 50 ns
  - tpc page mode read cycle: 25 ns
  - Refresh cycle: 256 cycles/ms (@Tj = 85°C)

Embedded DRAM Benefits

Benefits derived from integration of DRAM with logic are:

- Flexibility in utilizing different DRAM core configurations based on the application requirement
- Memory access time lower than discrete packaged devices
- Elimination of a large number of pins and associated packages, effectively reducing circuit board area
- Lower power consumption since systems with fast and wide memory busses will dissipate significantly less power due to lower capacitance on-chip connections
- Lower switching noise on data bus between memory and logic

Target Applications

Applications for 3T dRAMASIC™ include hard disk drive controllers, buffer memory for hubs and switches and printers.
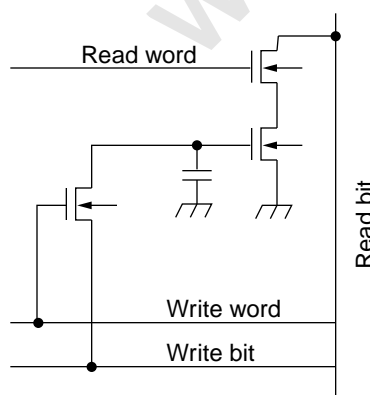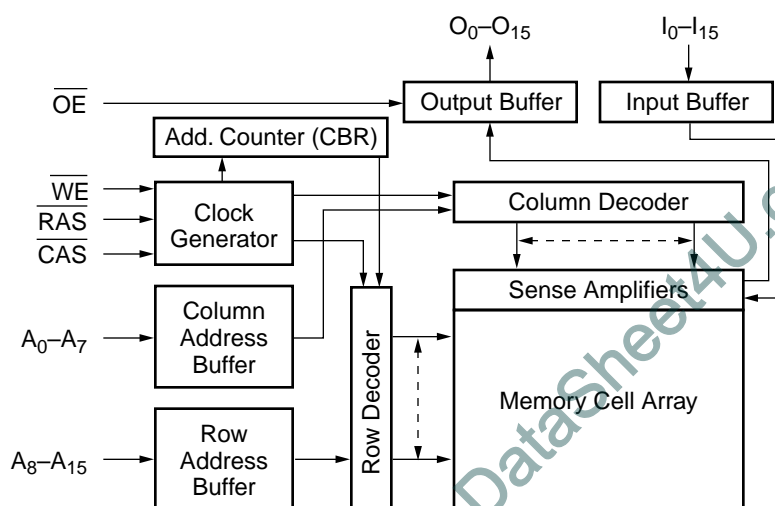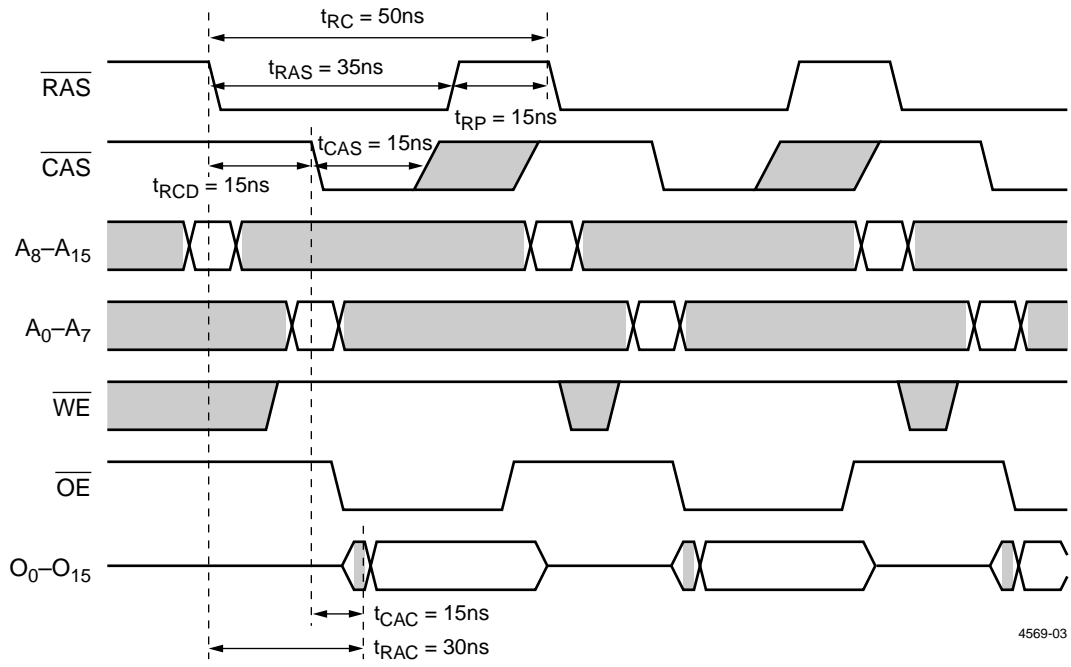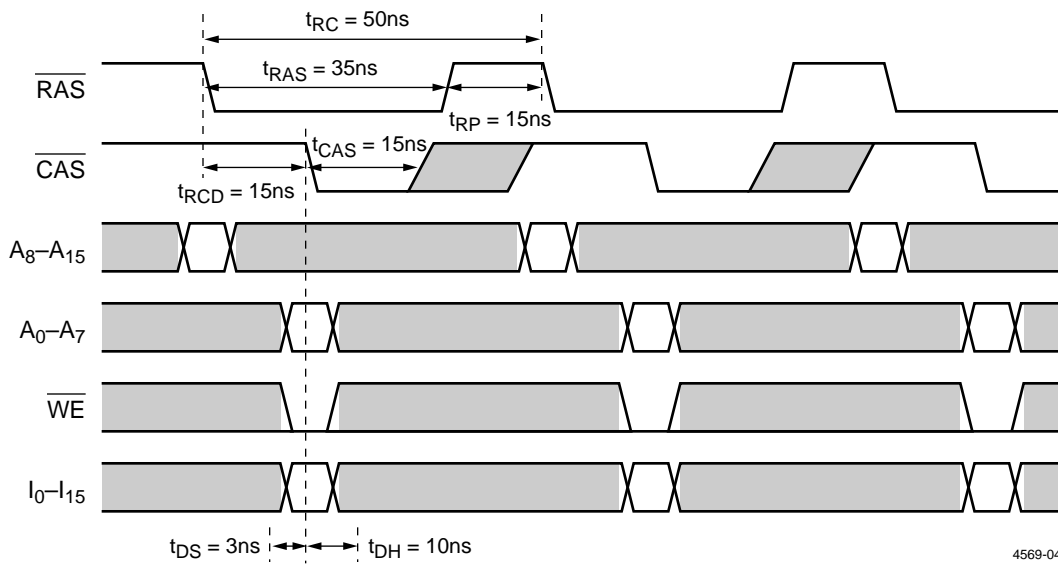

Figure 1. Three-Transistor DRAM Cell

Figure 2. DRAM Core Block Diagram

Timing Diagrams

Figure 3. Random Mode Read Cycle

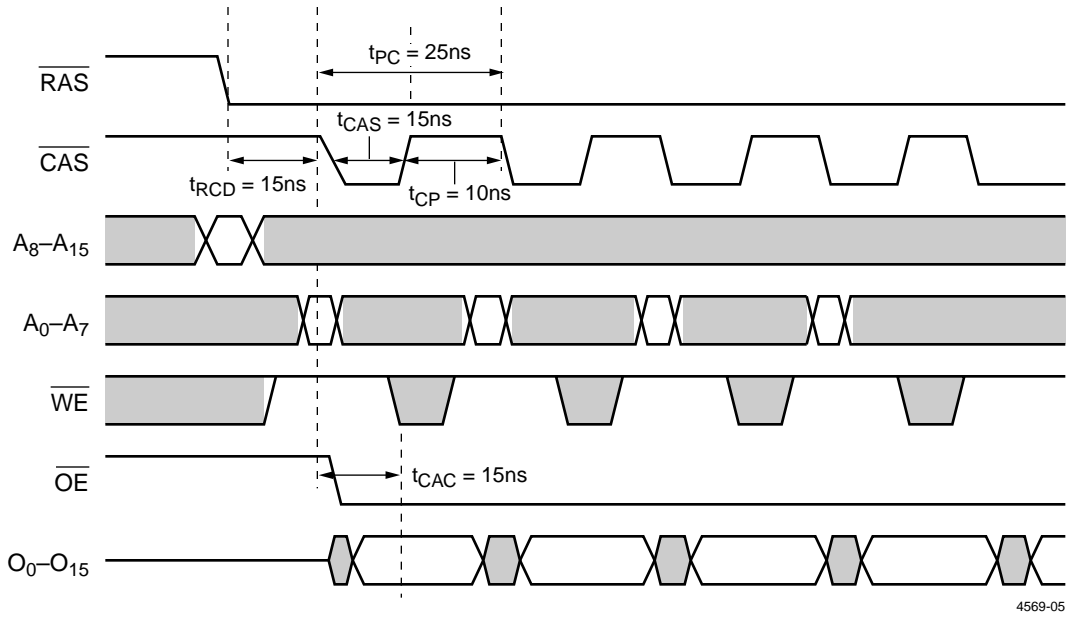
Figure 4. Random Mode Write Cycle
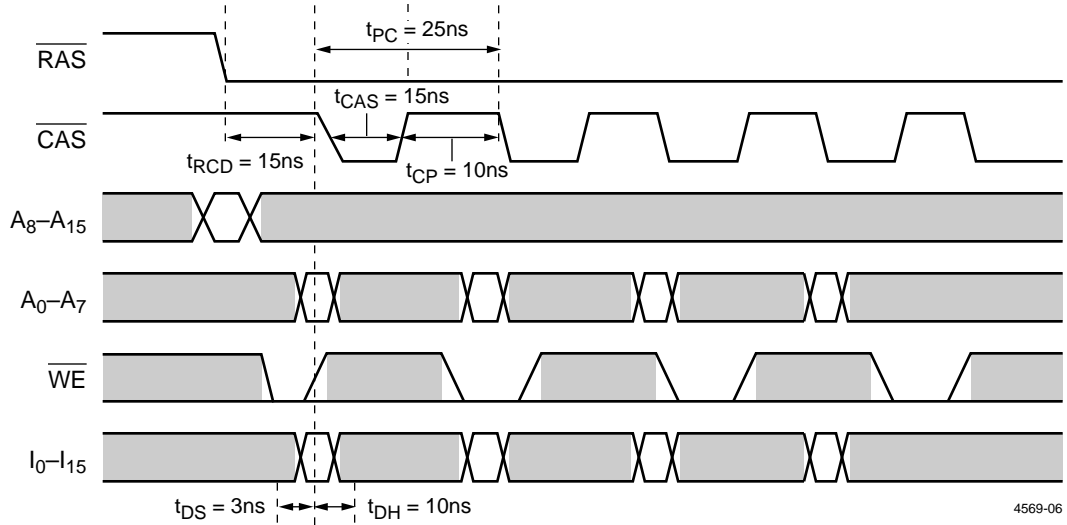
Figure 5. Hyper Page Mode Read Cycle

Figure 6. Hyper Page Mode Write Cycle

Technology Resource Centers

Toshiba ASIC Technology Resource Centers are located throughout the U.S. and provide a high level of technical expertise for support before, during and after the design of a Toshiba ASIC. This includes support issues dealing with EDA environments and design kits, Toshiba design methodologies, Toshiba ASIC technologies and Toshiba ASIC design implementation. Design consultation is also available.

In addition, Toshiba's North America Semiconductor Engineering Development Center in San Jose, CA is staffed by system, technology and EDA design experts to work with partners on advanced System IC applications.

Rigorous production quality control and monitoring coupled with a sophisticated batch tracking system enables Toshiba to meet the requirements of fast ramping, high volume markets.

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