DATA SHEET

74LV423
Dual retriggerable monostable multivibrator with reset

Product specification
1997 Feb 04

IC24 Data Handbook

Philips Semiconductors

PHILIPS

FEATURES

- Optimized for Low Voltage applications: 1.0 to 5.5V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) $<$ 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) $>$ 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulses
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

DESCRIPTION

The 74LV423 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT423.

The 74LV423 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). They are normally connected as shown in Figure 1. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering. Figures 2 and 3 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}. For pulse width when C_{EXT} <10000pF, see Figure 6. When $C_{EXT} >$ 10,000pF, the typical output pulse width is defined as: $t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.), where t_W = pulse width in ns; R_{EXT} = external resistor in KΩ; and C_{EXT} = external capacitor in pF. Schmitt-trigger action in the $n\overline{A}$ and nB inputs makes the circuit highly tolerant of slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$ $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15pF V_{CC} = 3.3V R_{EXT} = 5KΩ C_{EXT} = 0pF	 16 13	 ns ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_{CC} = 3.3V, V_I = GND to V_{CC}[1]	17	pF

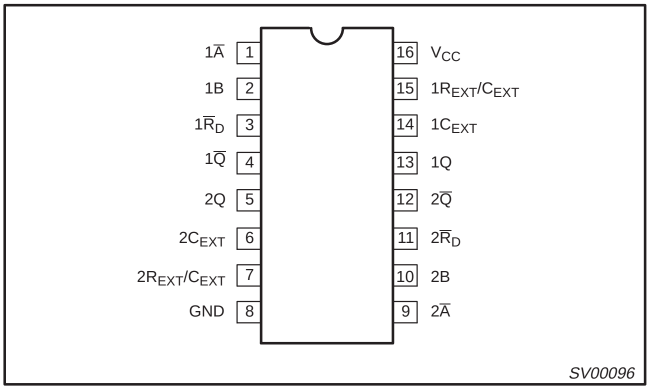
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV423 N	74LV423 N	SOT38-1
16-Pin Plastic SO	–40°C to +125°C	74LV423 D	74LV423 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV423 DB	74LV423 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV423 PW	74LV423PW DH	SOT403-1

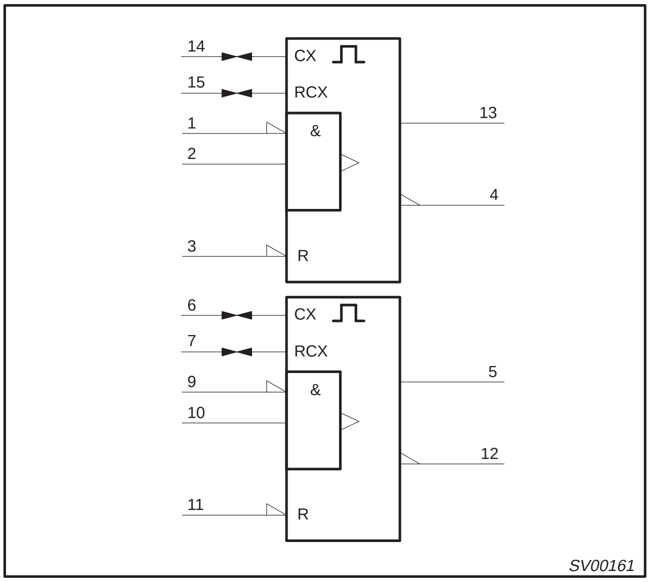
PIN CONFIGURATION



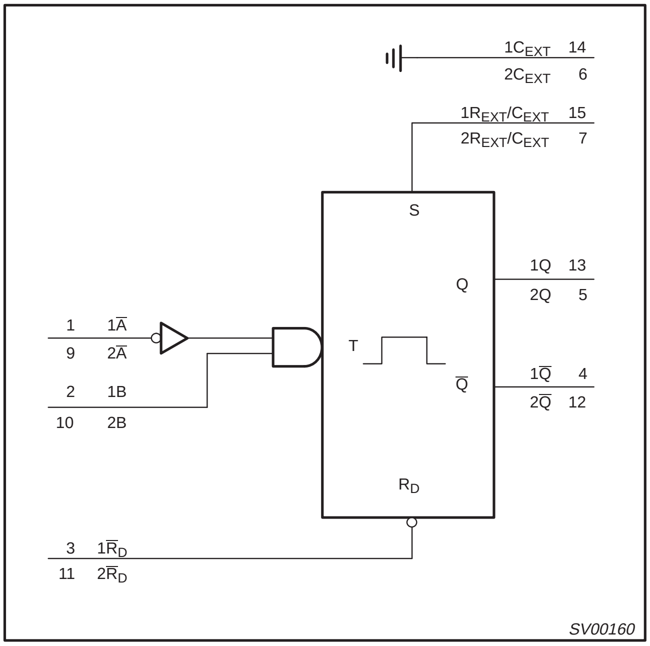
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,9	1A̅, 2A̅	Trigger inputs (negative-edge triggered)
2,10	1B, 2B	Trigger inputs (positive-edge triggered)
3,11	$1\overline{R}_D$, $2\overline{R}_D$	Direct reset LOW
4, 12	1Q̅, 2Q̅	Outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	External resistor/capacitor connection
8	GND	Ground (0V)
13, 5	1Q, 2Q	Outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	External capacitor connection
15	$1R_{EXT}/C_{EXT}$	External resistor/capacitor connection
16	V_{CC}	Positive supply voltage

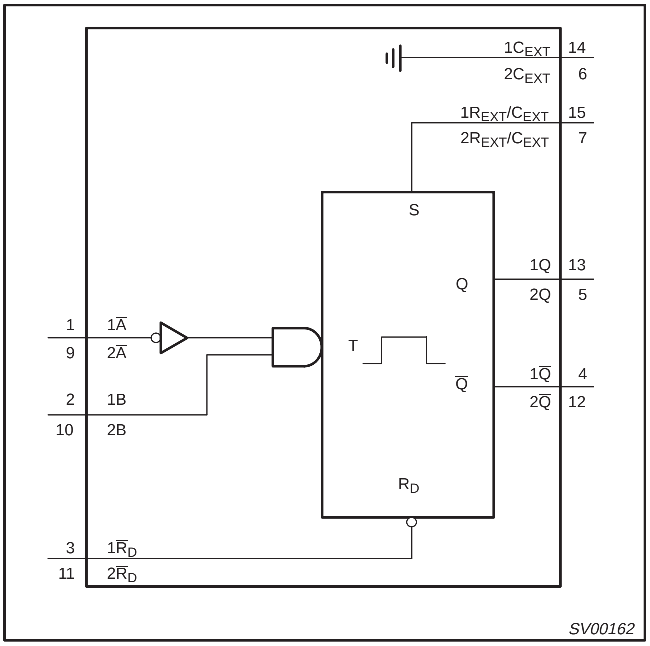
LOGIC SYMBOL (IEEE/IEC)



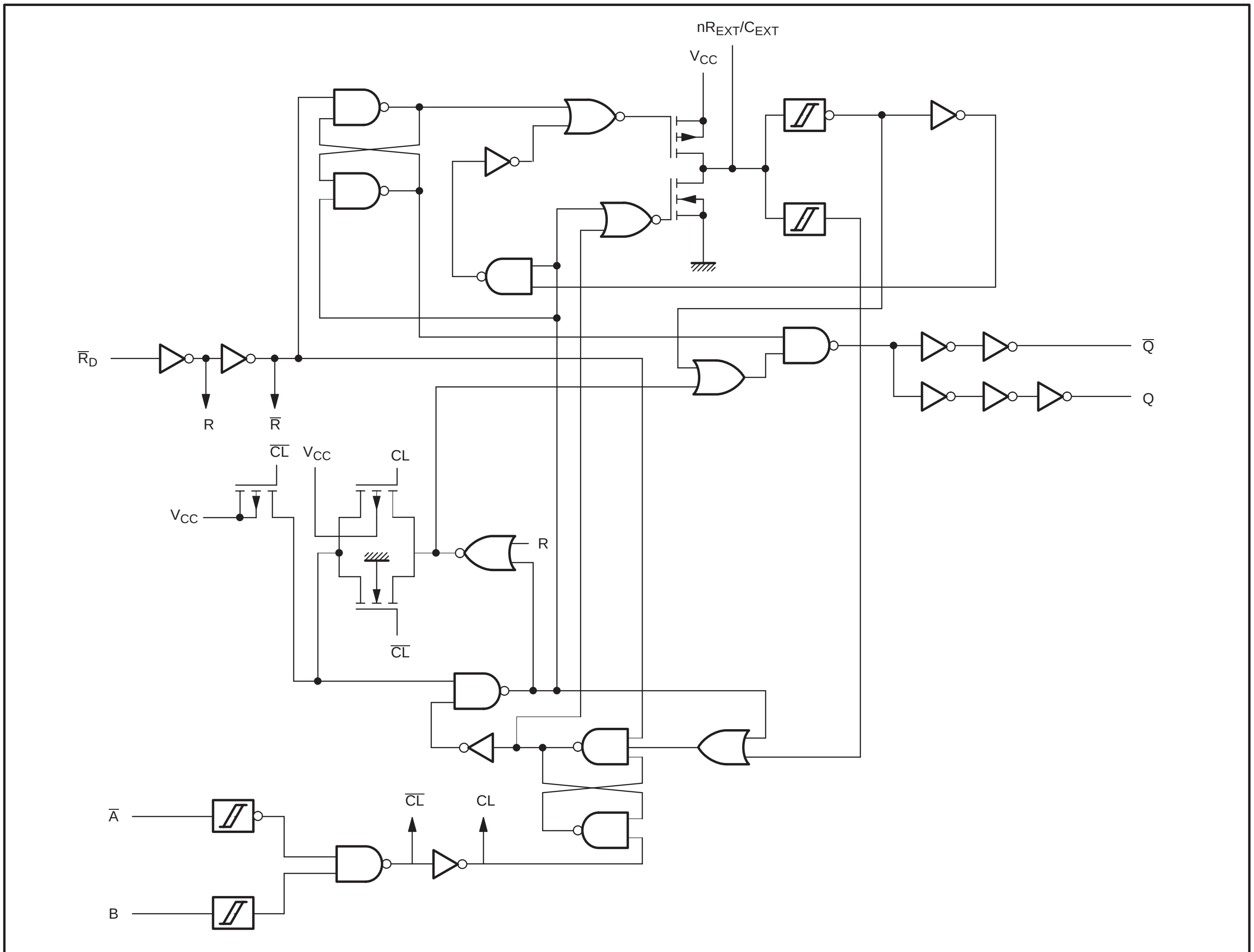
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



It is recommended that Pin 6 ($2C_{EXT}$) and Pin 14 ($1C_{EXT}$) by externally grounded to Pin 8 (GND)

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FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L *	H *
X	X	L	L *	H *
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔

NOTES:

* If the monostable was triggered before this condition was established, the pulse will continue as programmed.

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH transition

↓ = HIGH-to-LOW transition

⊓ = one HIGH level output pulse

⊔ = one LOW level output pulse

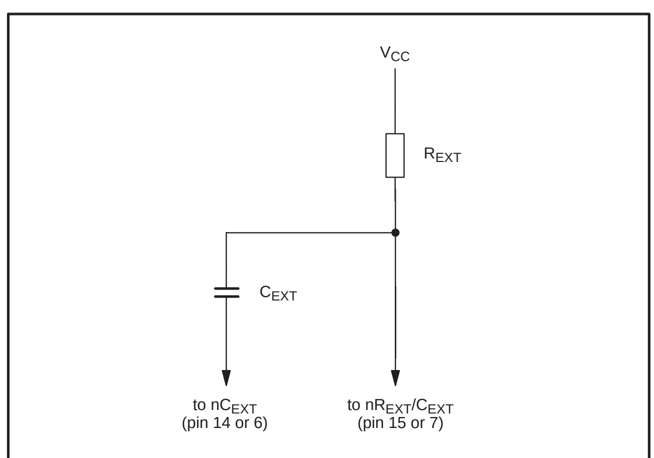


Figure 1. Timing Component Connection

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	 25 35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs – bus driver outputs		 50 70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.2	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			–40°C to +85°C			–40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
	Quiescent supply current; flip-flops	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		80	
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
	Quiescent supply current; LSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			500		1000	
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}	Propagation delay $n\overline{R}_D$, $n\overline{A}$, nB, to $n\overline{Q}$	Figure 4 C_{EXT} = 0pF R_{EXT} = 5kΩ	1.2		150				ns
			2.0		51	95		116	
			2.7		38	70		85	
			3.0 to 3.6		30[2]	56		68	
			4.5 to 5.5		20[3]	38		45	
t_{PLH}	Propagation delay $n\overline{R}_D$, $n\overline{A}$, nB, to $n\overline{Q}$	Figure 4 C_{EXT} = 0pF R_{EXT} = 5kΩ	1.2		150				ns
			2.0		51	95		116	
			2.7		38	70		85	
			3.0 to 3.6		30[2]	56		68	
			4.5 to 5.5		20[3]	38		45	
t_{PHL}	Propagation delay nR_D to nQ (reset)	Figure 4 C_{EXT} = 0pF R_{EXT} = 5kΩ	1.2		120				ns
			2.0		41	77		92	
			2.7		30	56		68	
			3.0 to 3.6		24[2]	45		54	
			4.5 to 5.5		18[3]	34		41	
t_{PLH}	Propagation delay nR_D to nQ (reset)	Figure 4 C_{EXT} = 0pF R_{EXT} = 5kΩ	1.2		120				ns
			2.0		41	77		92	
			2.7		30	56		68	
			3.0 to 3.6		24[2]	45		54	
			4.5 to 5.5		18[3]	34		41	
t_W	Trigger pulse width nA = LOW	Figure 4	2.0	30			40		ns
			2.7	25			30		
			3.0 to 3.6	20			25		
			4.5 to 5.5	15			20		
t_W	Trigger pulse width nB = HIGH	Figure 4	2.0	30			40		ns
			2.7	25			30		
			3.0 to 3.6	20	6[2]		25		
			4.5 to 5.5	15			20		
t_W	Reset pulse width nR_D = LOW	Figure 3	2.0	36					ns
			2.7	30			40		
			3.0 to 3.6	25			30		
			4.5 to 5.5	20			25		
t_W	Output pulse width $n\overline{Q}$ = HIGH nQ = LOW	Figures 2, 3	2.0						µs
			2.7						
			3.0 to 3.6		450[2]				
			4.5 to 5.5						
t_W	Output pulse width $n\overline{Q}$ = HIGH nQ = LOW	Figures 2, 3	2.0						ns
			2.7						
			3.0 to 3.6		75[2]				
			4.5 to 5.5						
t_{rt}	Retrigger time nA, nB	Figure 2	2.0						ns
			2.7						
			3.0 to 3.6		30[2]				
			4.5 to 5.5						

NOTES ON FOLLOWING PAGE

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
R_{EXT}	External timing resistor	Figure 6	1.2	20		1000			kΩ
			2.0	5		1000			
			2.7	5		1000			
			3.0 to 3.6	2		1000			
			4.5 to 5.5	2		1000			
C_{EXT}	External timing capacitor	Figure 6[3]	2.0	No limits					pF
			2.7						
			3.0 to 3.6						
			4.5 to 5.5						

NOTES:

1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.
4. For other R_{EXT} and C_{EXT} combinations see Figure 6.
   if C_{EXT} > 10 nF, the next formula is valid:
   $t_W = K \times R_{EXT} \times C_{EXT}$ (typ.)
   where, t_W = output pulse width in ns;
   R_{EXT} = external resistor in kΩ; C_{EXT} = external capacitor in pF;
   K = constant = 0.45 for V_{CC} = 5.0V and 0.48 for V_{CC} = 2.0V.
   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.
5. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}.
   The output pulse width will only be extended when the time between the active-going edges of the trigger pulses meets the minimum retrigger time.
   If C_{EXT} > 10 pF, the next formula (at V_{CC} = 5.0V) for the set-up time of a retrigger pulse is valid:
   $t_{rt} = 30 + 0.19R \times C^{-9} + 13 \times R^{1.05}$ (typ.)
   where, t_{rt} = retrigger time in ns;
   C_{EXT} = external capacitor in pF;
   R_{EXT} = external resistor in kΩ.
   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.
6. When the device is powered up, initiate the device via a reset pulse, when C_{EXT} < 50pF.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

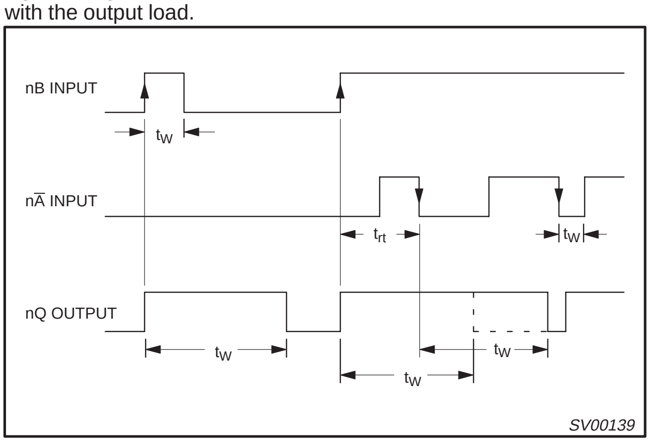


Figure 2. Output pulse control using retrigger pulse; $n\overline{R}_D$ = HIGH.

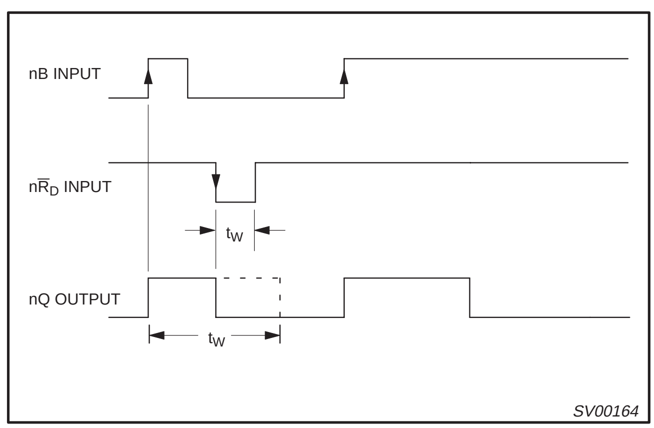


Figure 3. Output pulse control using reset input $n\overline{R}_D$; $n\overline{A}$ = LOW.

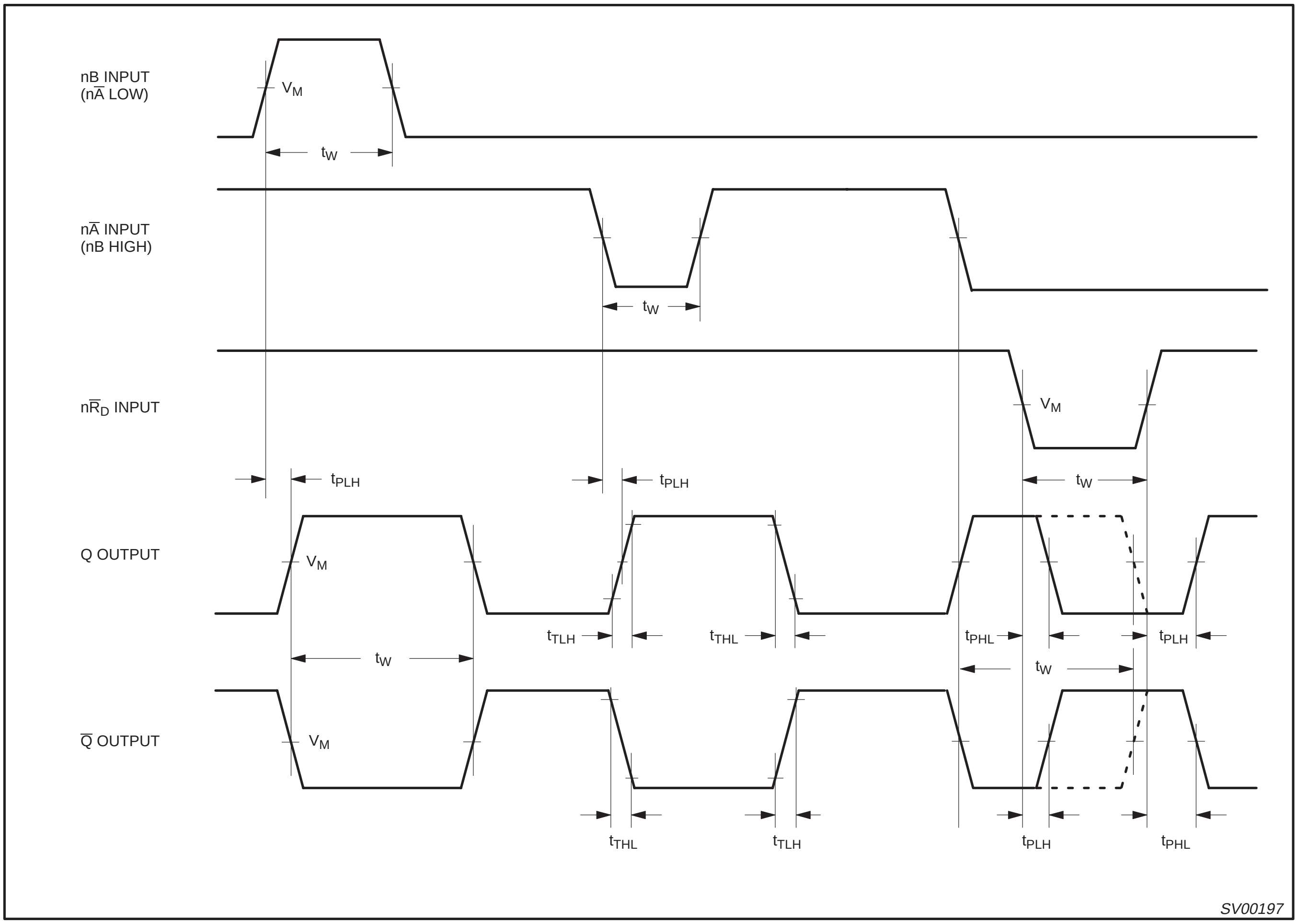


Figure 4. Waveforms showing the input (n$\overline{A}$, nB, n$\overline{R}_D$) to output (nQ, n$\overline{Q}$) propagation delays, the output transition times, and the input and output pulse widths.

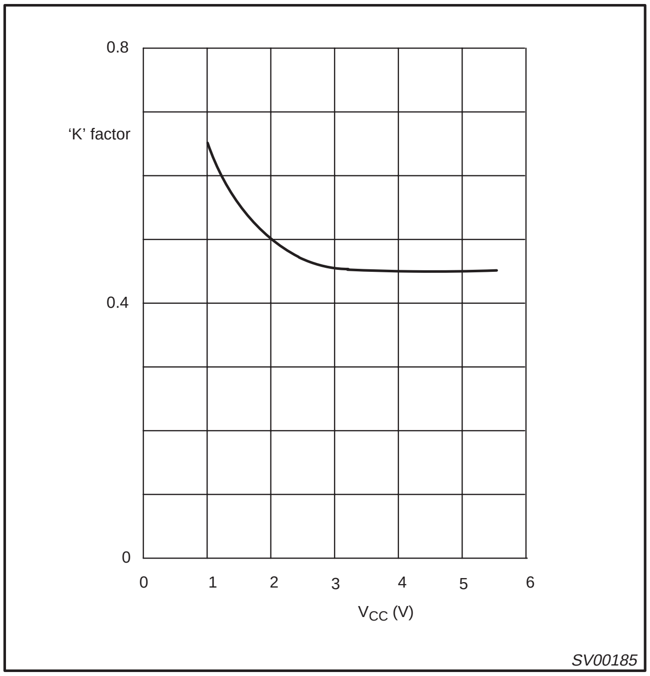


Figure 5. HCT typical "k" factor as a function of V_{CC}; C_X = 10 nF; R_X = 10 kΩ to 100 kΩ.

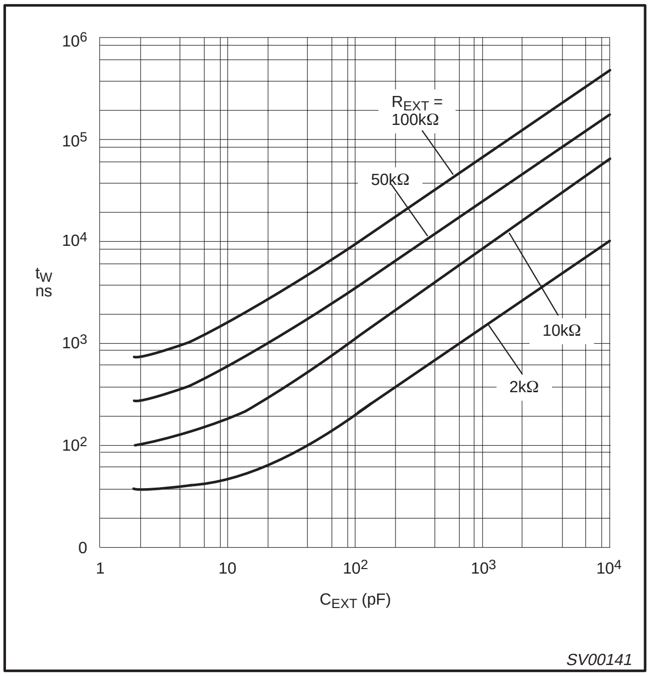


Figure 6. Typical output pulse width as a function of the external capacitor values at V_{CC} = 3.3V and T_{amb} = 25°C.

APPLICATION INFORMATION

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_X and C_X, this output pulse can be eliminated using the circuit shown in Figure 7.

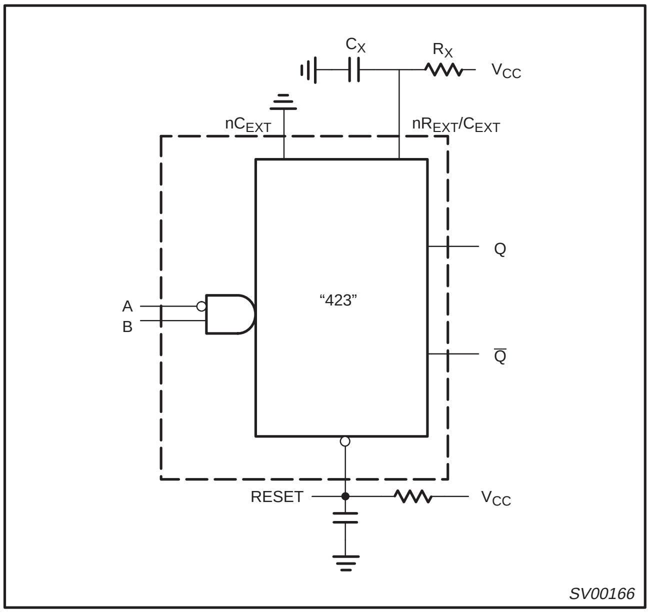


Figure 7. Power-up output pulse elimination circuit

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is power-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 8.

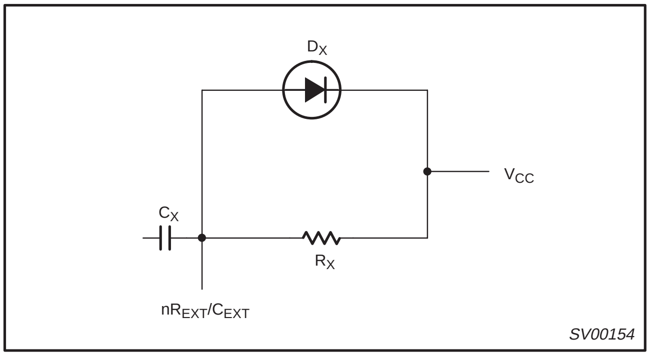
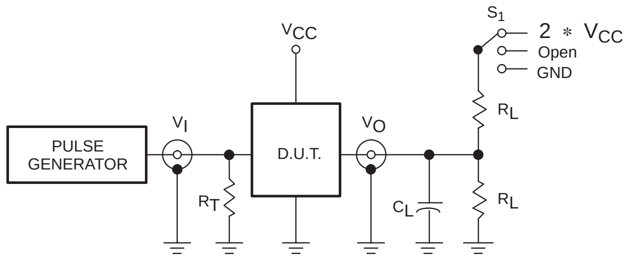


Figure 8. Power-down protection circuit

TEST CIRCUIT



Test Circuit for switching times

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 * V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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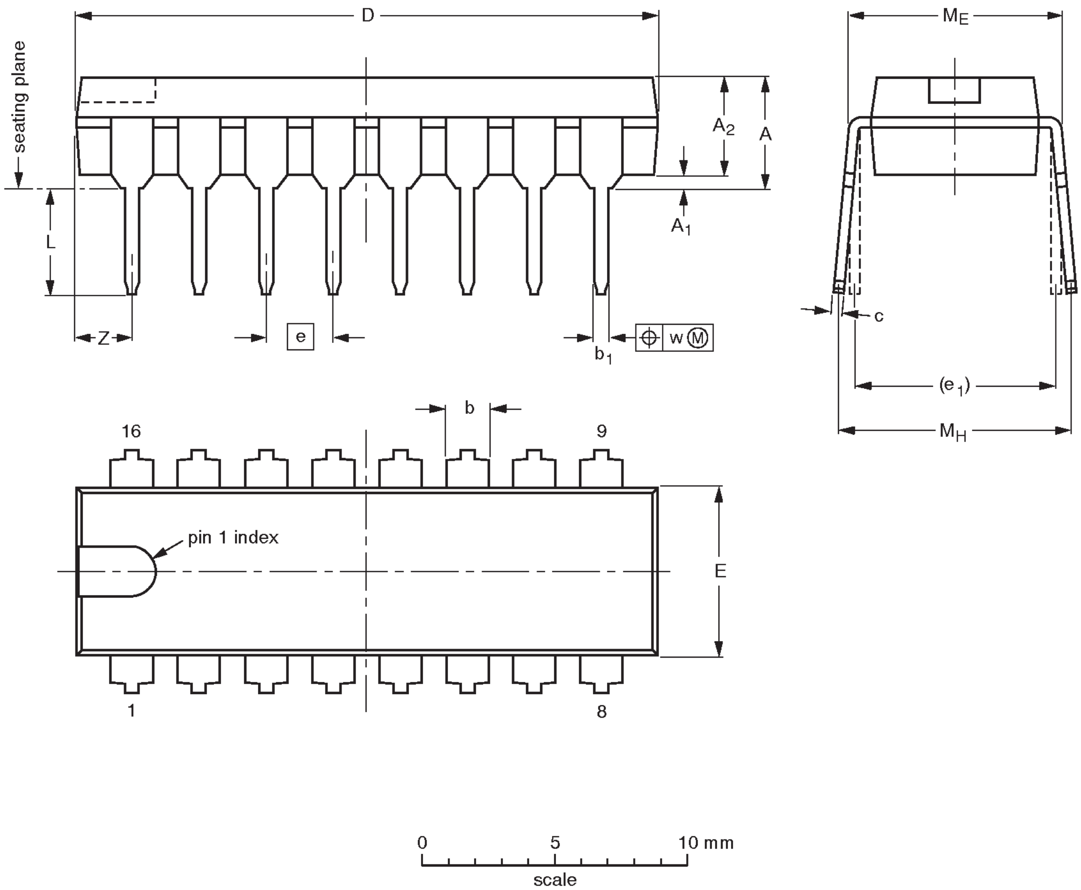
Figure 9. Load circuitry for switching times

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

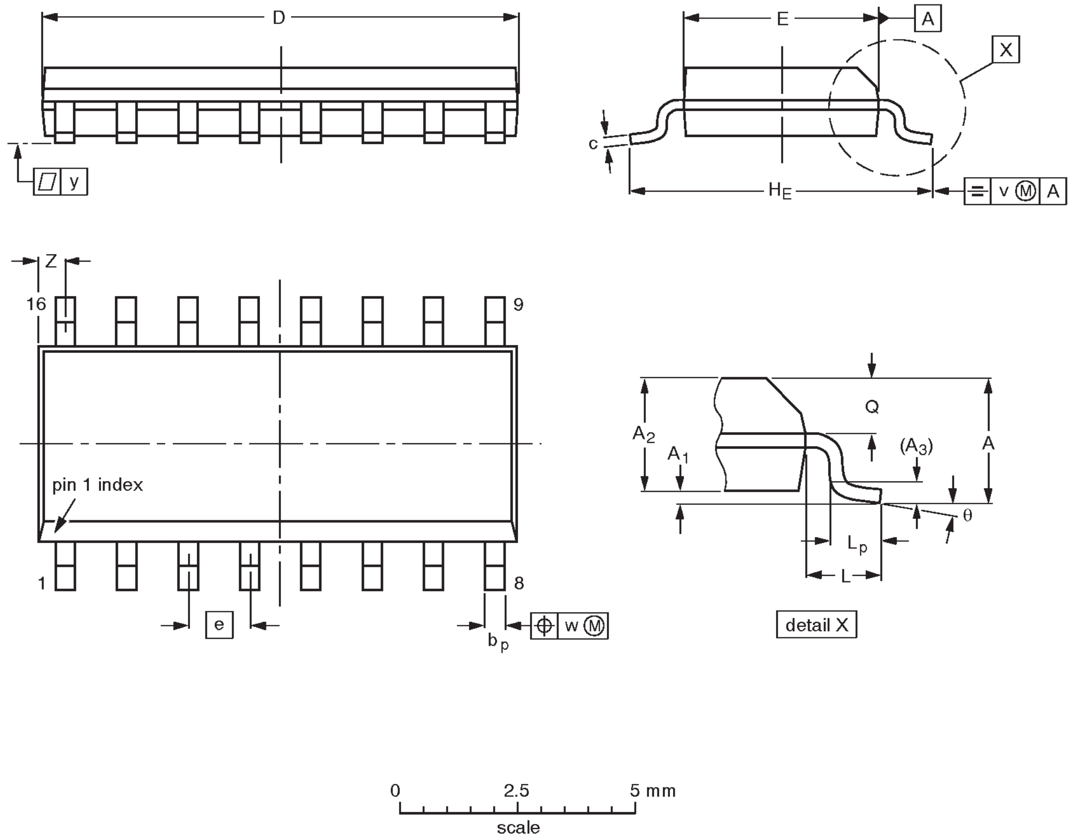
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

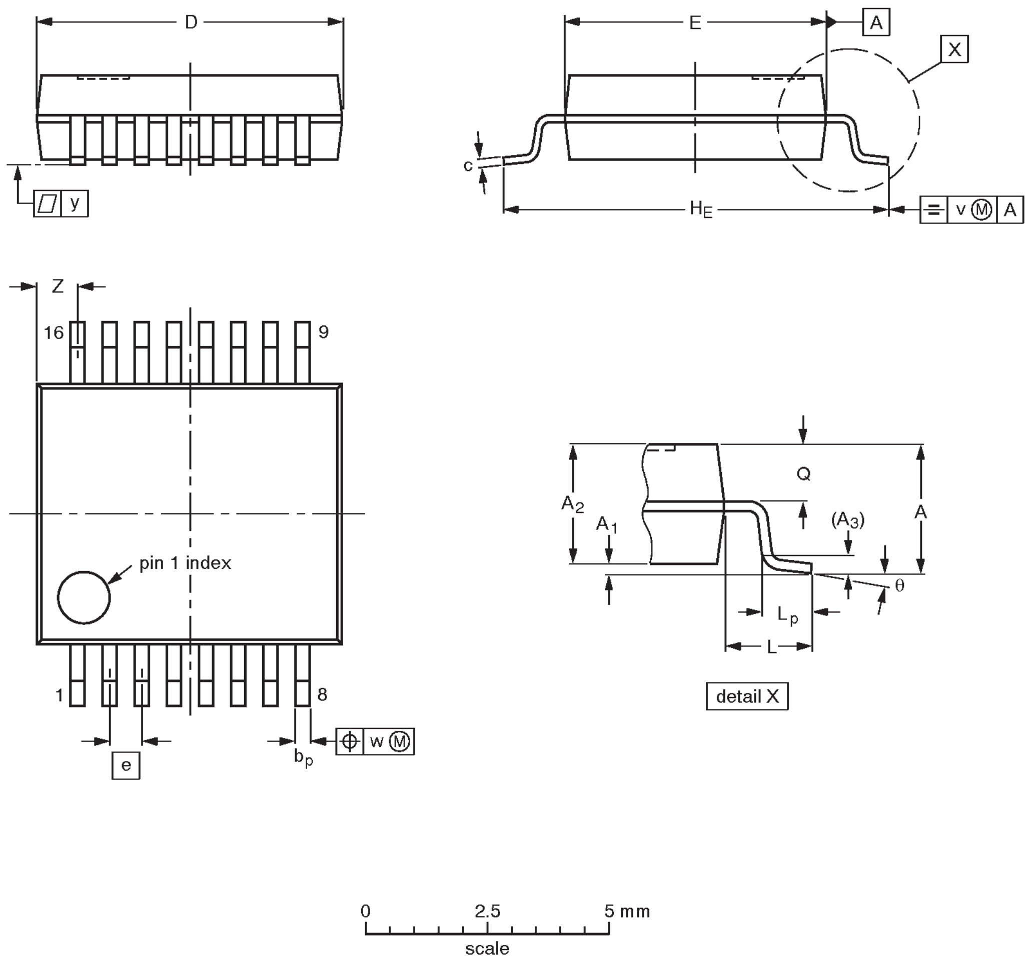
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

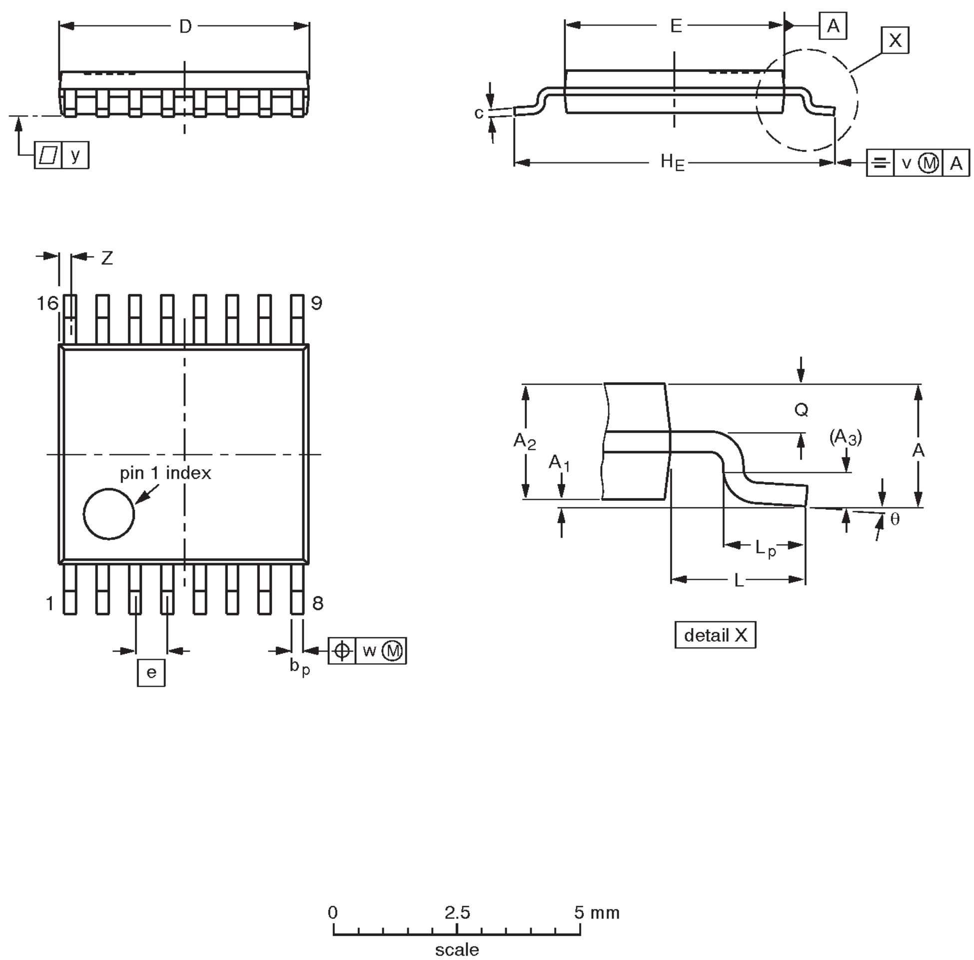
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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