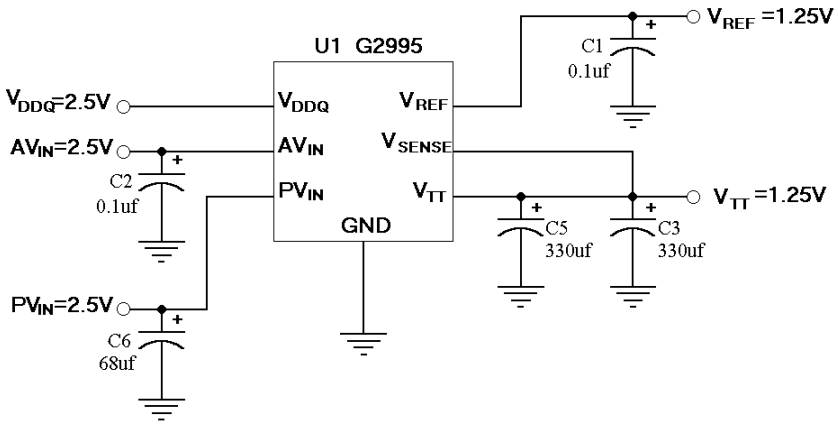
G2995 Evaluation Board Manual

Introduction

The G2995 evaluation board is designed to provide the design engineer with a fully functional prototype system in which to evaluate the G2995 in both a static environment and with a complete memory system. It is one version of the board, which SOP-8L(FD) is used. The application note contains information regarding the board,for more information regarding the G2995 please refer to the datasheet.

Schematic

The following schematic was used to create the layout.



Bill of Material

Name	Qty	Value	Description	Manufacturer	Model Number
U1	1		G2995 DDR Linear Regulator	Global Mixed-mode Technology http://www.gmt.com.tw	G2995
C3, C5	2	330uf	6.3V POSCAP Series	SANYO	6TPD330M
C6	1	68uf	6.3V POSCAP Series	SANYO	6TPB68M
C1, C2	2	0.1uf	0603 Ceramic Capacitor X7R 6.3V	TDK	1068X7R1H104K

Application

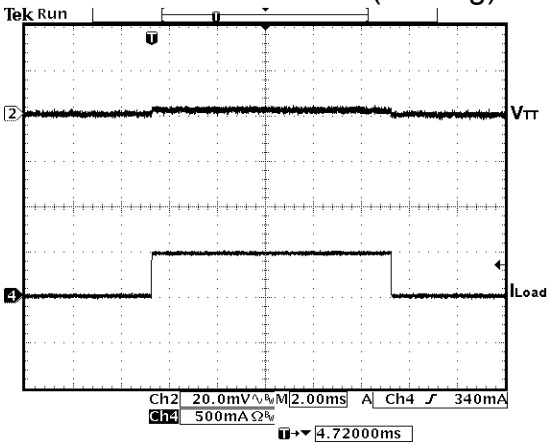
The G2995 evaluation board can be used immediately in either a static test environment to check functionality or in a memory termination scheme on a motherboard. In either implementation the following steps should be taken to ensure correct operation.

1. Correct leads from the evaluation board. The board layout has been designed to allows sockets to be directly soldered.
2. AVIN and PVIN should be connected to a 2.5V power supply.
3. The VDDQ input provides the internal divide by two reference voltage. Both VREF and VTT will track this internal voltage, nominally a 2.5V will be applied.
4. The VREF pad is the output for the VREF from the G2995 after being bypassed by a ceramic capacitor. This can be connected either to a multi-meter for confirmation or directly to the memory controller and DIMMS.
5. The remaining two pads are for the force and sense leads of the VTT output. These should be connected directly to the termination plane or a multi-meter if interested in verification. The output will be regulated where the VSENSE leads connect to the VTT leads permitting the connection to a motherboard without suffering from large resistance drops.

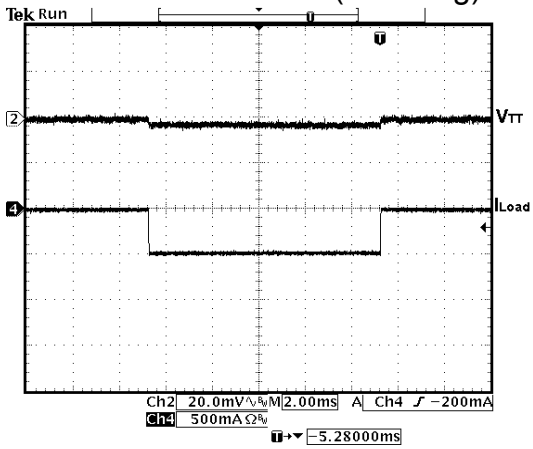
Performance

The following series of scope plots shows the performance of the G2996 evaluation board when it is subjected to various load tests. On each of the six scope plots there are two traces. The upper trace is the V_{TT} output voltage that has been AC coupled with a scale of 20mV per division. The lower trace is the output current with a scale of 500mA per division. All the load transients begin from an initial condition of zero current and show magnitude. Please refer to the title to determine whether the current flow is into (sinking) or out from (sourcing) the V_{TT} pin. The time scale for all the plots is 2mS per division.

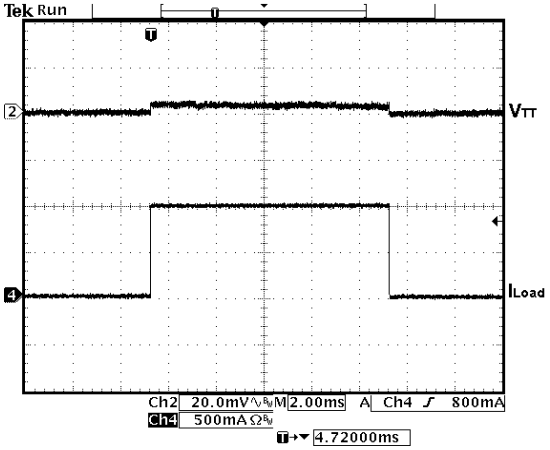
ILoad=0.5A Transient(Sinking)



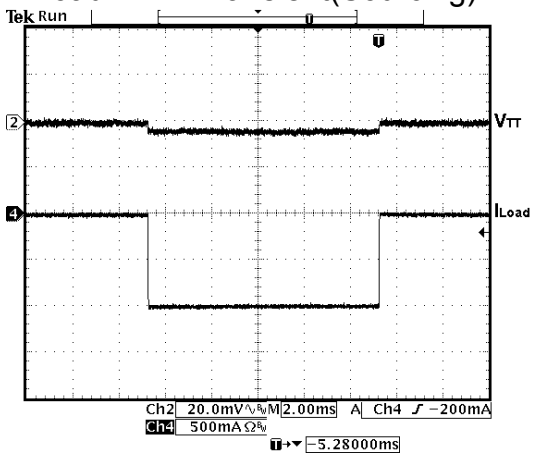
ILoad=0.5A Transient(Sourcing)



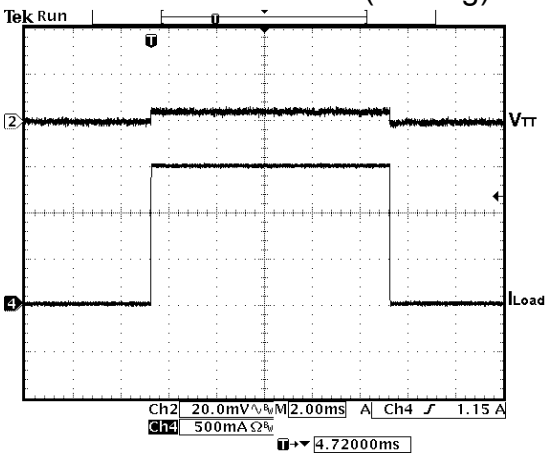
ILoad=1A Transient (Sinking)



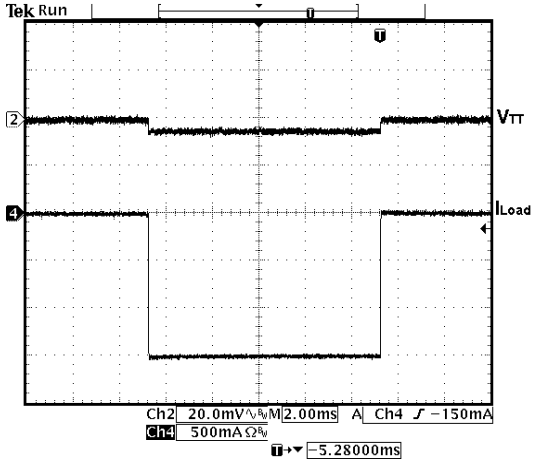
ILoad=1A Transient(Sourcing)



ILoad=1.5A Transient (Sinking)

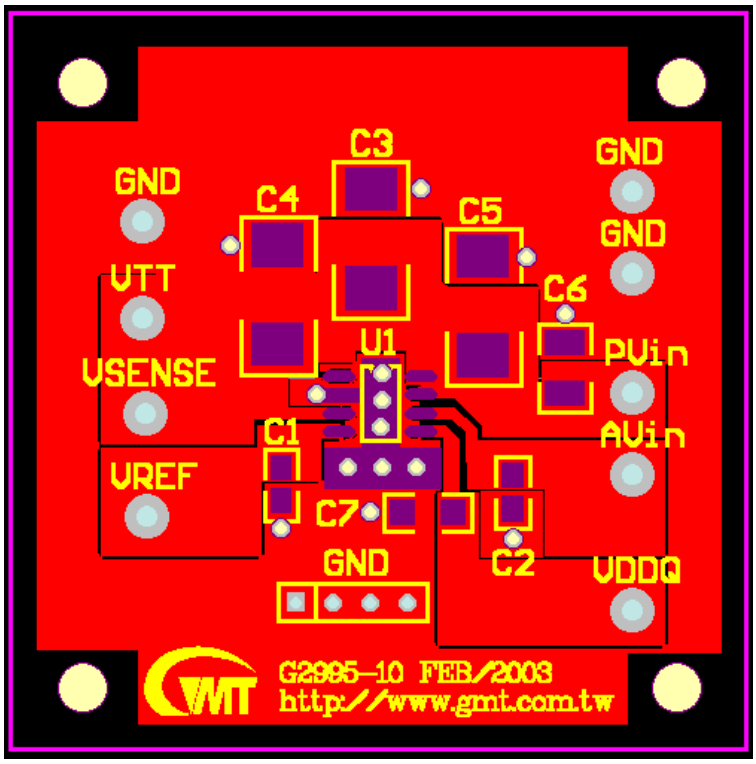


ILoad=1.5A Transient(Sourcing)

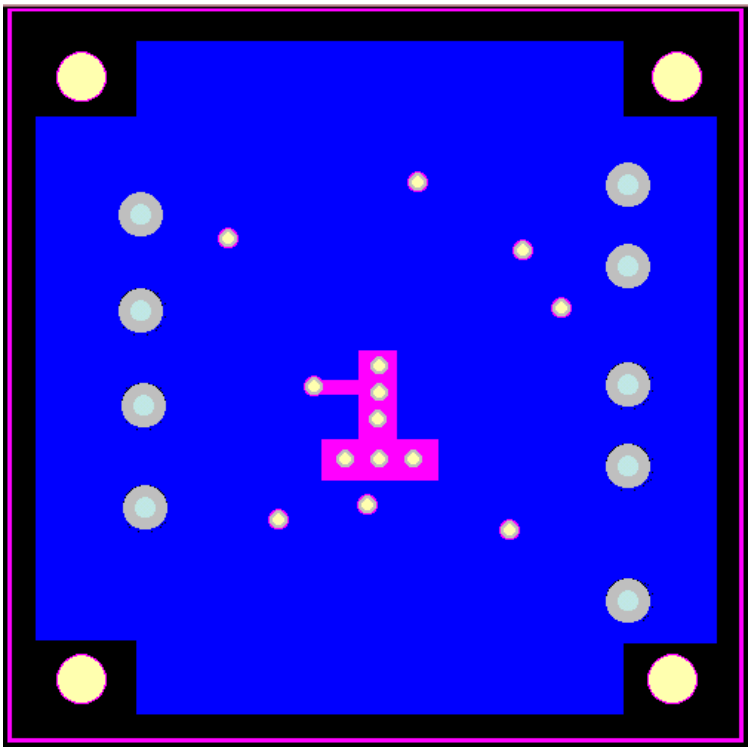


Board Layout

SOP-8L(FD) Top Side



SOP-8L(FD) Bottom Side



Board Layout (Continuous)

Information	SOP- 8L(FD) Board
Board Material	FR4
Size	50mm× 50mm
Board Thickness	1.6mm
Layers	2
Copper Thickness	2 oz
Thermal Vias	6
Thermal Vias Size	28mil