LM114/H, LM114A/AH
Monolithic Dual NPN General Purpose Amplifier

INTERSIL

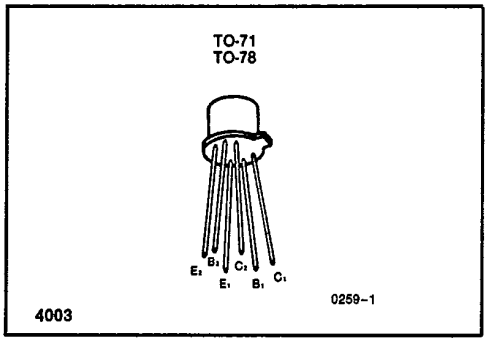
T-29-27

GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10μA collector current. Typical collector-base capacitance is only 1.6 pF at 5V.

PIN CONFIGURATION



FEATURES

- **Low Offset Voltage**
- **Low Drift**
- **High Current Gain**
- **Tight Beta Match**
- **High Breakdown Voltage**
- **Matching Guaranteed Over A 0V to 45V Collector-Base Voltage Range**
- **CMRR > 100dB**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (1)	45V
Collector-Emitter Voltage (1)	45V
Collector-Collector Voltage	45V
Emitter-Base Voltage (1)	6V
Collector Current (1)	20mA
Storage Temperature Range	−65°C to +200°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation (T_C = 25°C)	800mW
Derate above 25°C	14mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-71	TO-78
LM114	LM114H
LM114A	LM114AH

ELECTRICAL CHARACTERISTICS (NOTE 2)

Symbol	Parameter	Test Conditions	Maximum Limits		Units
			LM114A, AH	LM114, H	
V_{BE1-2}	Offset Voltage	1μA ≤ I_C ≤ 100μA	0.5	2.0	mV
I_{B1-2}	Offset Current	I_C = 10μA	2.0	10	nA
	Bias Current	I_C = 1μA	0.5	40	nA
		I_C = 10μA	20		
		I_C = 1μA	3.0		
$\Delta V_{BE}/V$	Offset Voltage Change	0V ≤ V_{CB} ≤ V_{MAX}, I_C = 10μA	0.2	1.5	mV
$\Delta I_B/V$	Offset Current Change		1.0	4.0	nA

10

NOTE: All typical values have been characterized but are not tested.

LM114/H, LM114A/AH

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ELECTRICAL CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Maximum Limits		Units
			LM114A, AH	LM114, H	
$\Delta V_{BE}/\Delta T$	Offset Voltage Drift	$-55°C \le T_A \le +125°C$, $I_C = 10\mu A$	2.0	10	$\mu V/°C$
$\Delta I_{B1-2}/\Delta T$	Offset Current		12	50	nA
$\Delta I_B/\Delta T$	Bias Current		60	150	
I_{CBO}	Collector-Base Leakage Current	$V_{CB} = V_{MAX}$	10	50	pA
		$T_A = 125°C$ (Note 3)	10	50	nA
I_{CEO}	Collector-Emitter Leakage Current	$V_{CE} = V_{MAX}$, $V_{EB} = 0V$	50	200	pA
		$T_A = 125°C$ (Note 3)	50	200	nA
I_{C1-C2}	Collector-Collector Leakage Current	$V_{CC} = V_{MAX}$	100	300	pA
		$T_A = 125°C$ (Note 3)	100	300	nA

NOTES: 1: Per transistor.
2: These specifications apply for $T_A = +25°C$ and $0V \le V_{CB} \le V_{MAX}$, unless otherwise specified. For the LM114 and LM114A, $V_{MAX} = 30V$.
3. For design reference only, not 100% tested.

NOTE: All typical values have been characterized but are not tested.