DATA SHEET

PCD4440T
Analog voice scrambler/descrambler

Product specification
Supersedes data of October 1992
File under Integrated Circuits, IC03

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Philips Semiconductors

PHILIPS

CONTENTS

Analog voice scrambler/descrambler PCD4440T

1 FEATURES

- Scrambler or descrambler function
- Scrambling in frequency domain
- Selectable split frequency (up to 10 selections per second)
- Telephony-band filtering included
- No increase in bandwidth
- No external components required
- Small signal delay
- Insensitive to distortion and group delay of transmission channel
- Control via serial I^2C-bus
- Low transfer loss of speech
- Mute option
- Transparent mode
- High signal input impedance
- Low signal output impedance
- Low power consumption.

2 APPLICATIONS

- Cordless telephones
- Security telephones
- Portable phones
- Private Mobile Radio (PMR).

3 GENERAL DESCRIPTION

The PCD4440T is a silicon gate CMOS integrated circuit intended to be used in cordless telephony, radio, and line telecommunications products utilizing a microcontroller for the control functions. The purpose of the device is to prevent unauthorized ‘listening-in’ on conversations.
A major application is protection of the vulnerable radio link between a CT0 type cordless handset and its base unit.
Analog scrambling/descrambling is based on the split frequency method realized in a sophisticated switched-capacitor technology. The PCD4440T is compatible with most microcontrollers and communicates via a two line bidirectional I^2C-bus.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD4440T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 BLOCK DIAGRAM

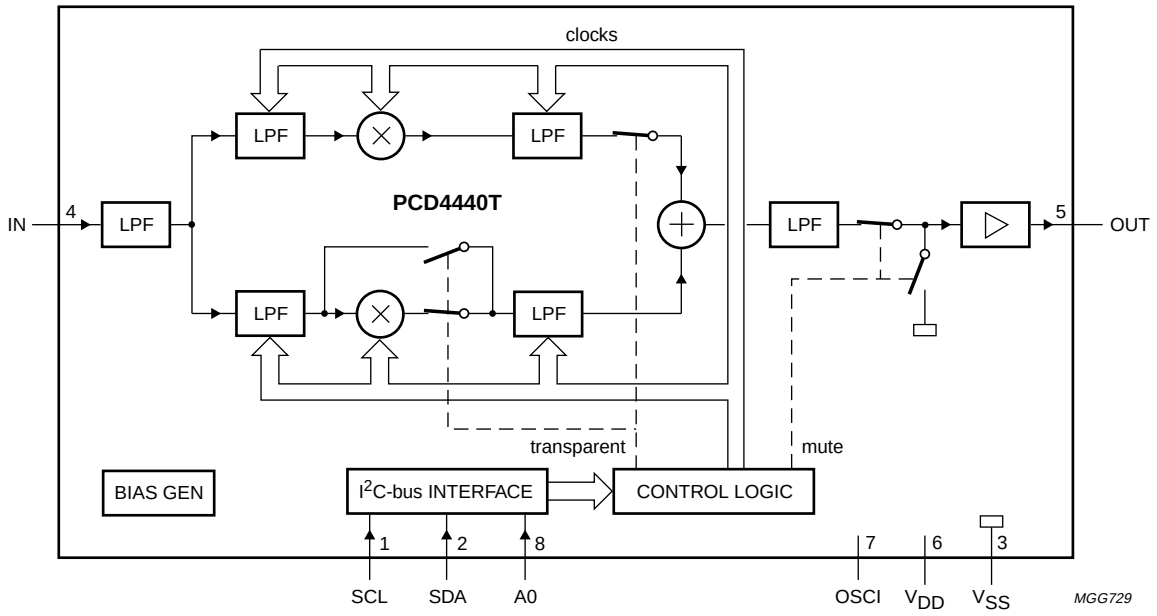


Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

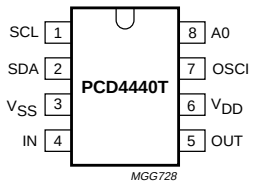


Fig.2 Pin configuration.

6.2 Pin description

SYMBOL	PIN	TYPE	DESCRIPTION
SCL	1	I	serial clock line (I^2C-bus)
SDA	2	I	serial data line (I^2C-bus)
V_{SS}	3	P	negative Supply
IN	4	I	signal input
OUT	5	O	signal output
V_{DD}	6	P	positive supply
OSCI	7	I	oscillator input
A0	8	I	slave address input (I^2C-bus)

7 FUNCTIONAL DESCRIPTION

To provide privacy for the end user of a cordless telephone set, the radio-link audio signal must be scrambled. In the microphone of the handset and the incoming telephone line audio path of the base unit a scrambler circuit has to be implemented. Consequently the audio signal to the telephone line and to the earpiece must be descrambled. Both functions can be fulfilled by the PCD4440T by simply inserting it in the audio path.

7.1 Scrambling

The PCD4440Taccomplishes this task by first filtering the incoming signal, limiting the bandwidth to 3500 Hz. Then the signal is split into a high ($> f_s$) and a low ($< f_s$) frequency band. Both frequency bands are inverted and added again to provide a single output signal. Values for 9 split frequencies f_S can be controlled by a scramble code table in the microcontroller. Control of these split frequencies is accomplished via the serial two-wire I^2C-bus. In addition to the split frequencies (f_s), a transparent mode and mute instruction can be selected (see Table 1).

Figure 3 shows the signal path for both bands. The lower band path (on the left side of the diagram) operates on frequencies $f \leq f_s$ (Split Frequency), the upper band path (on the right side) on frequencies $f \geq f_s$.

The input signal contains frequencies from f_1 up to f_2. In scrambling mode, the output signal is band limited from f_l (300 Hz) to f_h (3500 Hz). In the left path, the input signal is first limited to f_s. The following modulator inverts the lower band. f_l is folded up to f_s, f_s down to f_l. In general, an input frequency f_{in} is folded to $f_{out} = f_s + f_l - f_{in}$. Finally the folded signal is band limited to f_s again.

In the right path, the input signal is first limited to f_h. The following modulator inverts the upper band. f_s is folded up to f_h, f_h down to f_s. In general, an input frequency f_{in} is folded to $f_{out} = f_s + f_h - f_{in}$. Finally, the folded signal is band limited to f_h again. In the last step, the bands are added and buffered.

Because of the symmetry of the scrambling process, descrambling is achieved by passing the signal through another PCD4440T.

In the transparent mode, the input signal is band limited to 3500 Hz. Frequencies from 0 to 300 Hz are not filtered out.

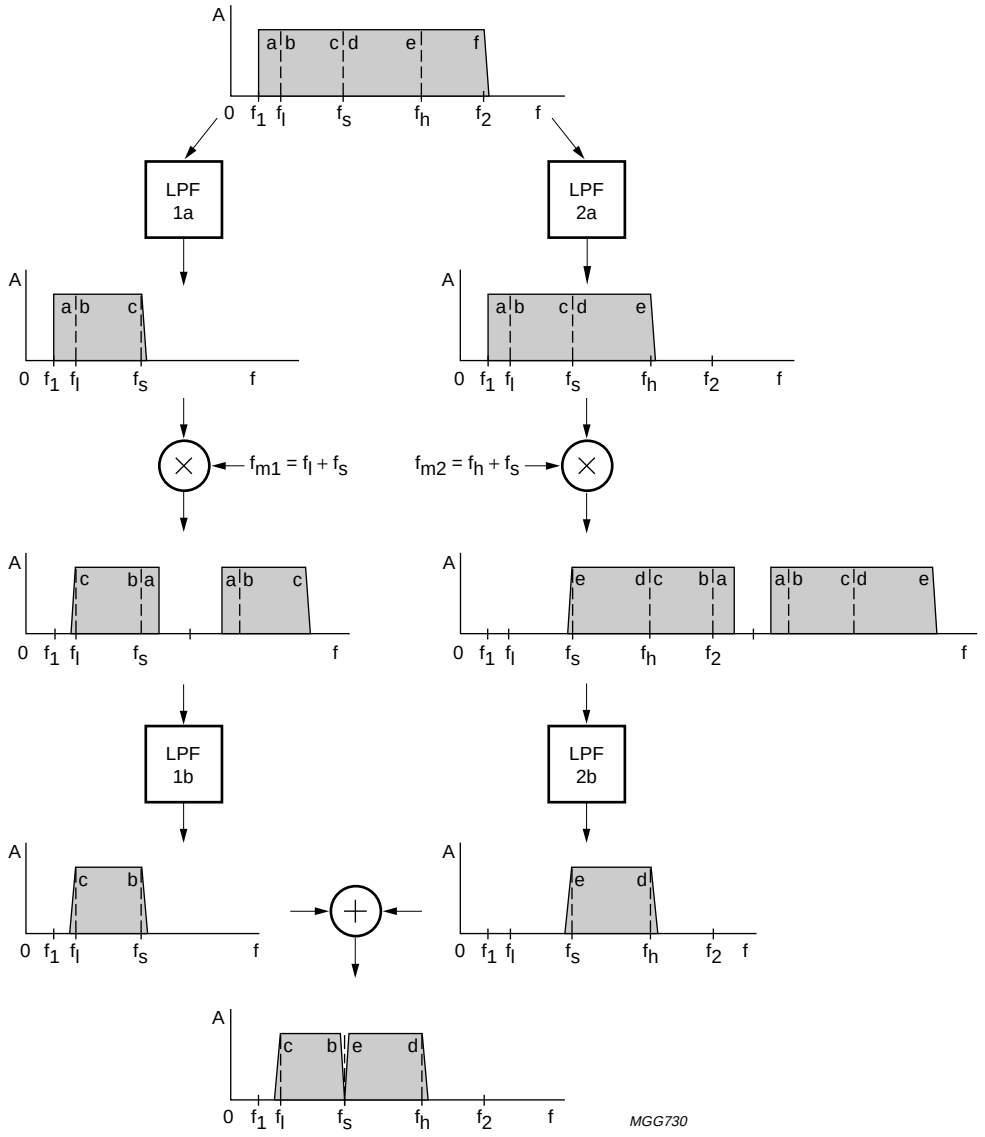


Fig.3 Scrambler signal path.

7.2 Power supply (V_{DD}, V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirement as indicated in the characteristics. To avoid undefined states of the device at power-on, an internal reset circuit clears the logic. The power-on reset has the highest priority; it blocks and resets the complete circuit.

7.3 Oscillator (OSCI)

The time base for the PCD4440T is a 3.58 MHz input signal which can be derived from the oscillator output (OSCO) of Philips microcontroller families PCD33xxA or PCF84CxxxA. Figure 4 shows the OSCI connection.

7.4 Splitting frequency and mode selection

Table 1 shows the input codes required to select the various splitting frequencies, and the mute, transparent and scramble/descramble modes. The codes form part of the serial I^2C-bus message input on the SDA line from the microcontroller.

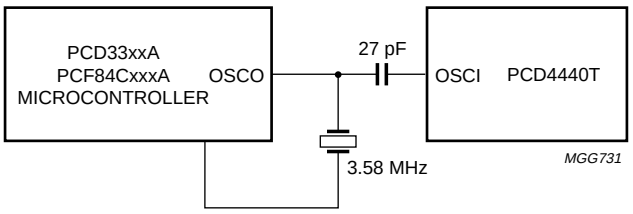


Fig.4 OSCI (oscillator input) connection.

Table 1 Input data codes for splitting frequency and mode selection; note 1

D3	D2	D1	D0	HEX	APPLICATION	f_s(2) (Hz)
0	0	0	1	01	Mute mode	–
0	0	1	0	02	Select f_s	2641
0	0	1	1	03	Select f_s	1853
0	1	0	0	04	Select f_s	1507
0	1	0	1	05	Select f_s	1279
0	1	1	0	06	Select f_s	1117
0	1	1	1	07	Select f_s	1018
1	0	0	0	08	Select f_s	899
1	0	0	1	09	Select f_s	837
1	0	1	0	0A	Select f_s	767
1	0	1	1	0B	Transparent mode	–
1	1	1	1	0F	Start scramble/descramble mode	–

Notes

1. Input codes other than shown in the table are not allowed.
2. Oscillator frequency = 3.58 MHz.

7.5 Serial clock input (SCL), Serial data input (SDA)

SCL and SDA are serial clock and data lines which conform to the I²C-bus specification. Both inputs must be pulled up externally to V_{DD} through resistors of approximately 10 kΩ.

7.6 Address input (A0)

A0 is the slave address input and is used to set one bit of the slave address, so as to identify one of two PCD4440T devices connected to the same I²C-bus. Whether another PCD4440T is connected to the bus or not, A0 must be connected to V_{DD} or V_{SS}. The remaining bits of the slave address are fixed internally.

7.7 I²C-bus data configuration

The PCD4440T is always a slave receiver in the I²C-bus configuration (the R/$\overline{W}$ bit = 0). The slave address consists of 7 bits, where the least significant is set by the input on A0. The more significant bits are fixed internally, as shown in Fig.5. For definition of D0-D4, see Table 1.

7.8 Signal input (IN), Signal output (OUT)

Signal input for the scrambler/descrambler is coupled into a 'Sallen and Key' anti-aliasing filter configuration. A DC bias voltage of $\frac{1}{2}V_{DD}$ is built-in.

The analog signal output is buffered to achieve a relatively low output impedance of roughly 1 kΩ which is sufficient to drive the earpiece amplifier or similar applications.

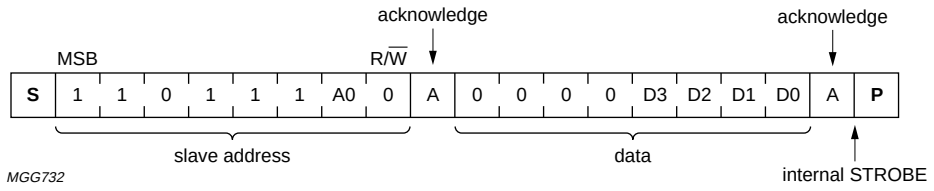


Fig.5 I²C-bus data format.

8 I²C BUS INTERFACE

The I²C-bus is for two-way communication between different ICs or modules. It uses only two lines, a serial data line (SDA) and a serial clock line (SCL), both of which are bi-directional. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.6)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

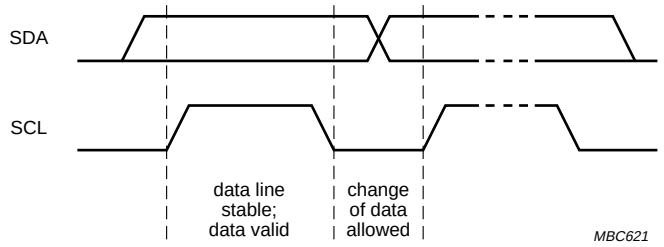


Fig.6 Bit transfer.

8.2 Start and stop conditions (see Fig.7)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

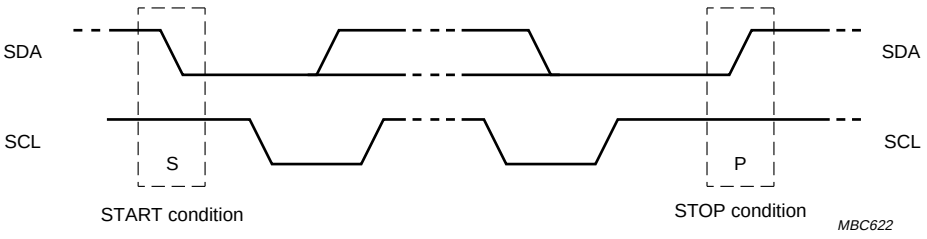


Fig.7 Start and stop conditions.

8.3 **System configuration** (see Fig.8)

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls message transfer is the ‘master’ and the devices that are controlled by the master are the ‘slaves’.

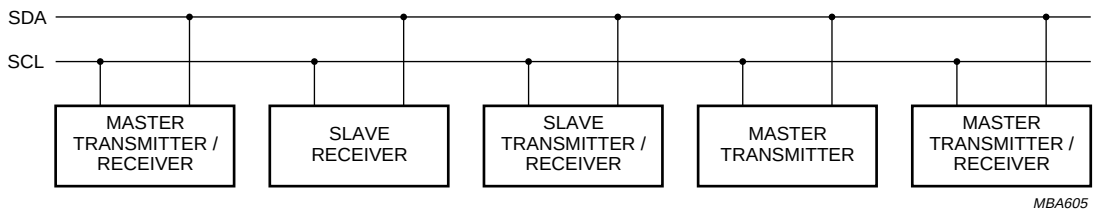


Fig.8 System configuration.

8.4 **Acknowledge** (see Fig.9)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge after the reception of each byte. Also a master must generate an acknowledge after reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge-related clock pulse. Set-up and hold times must be taken into account to ensure that the SDA line is stable LOW during the whole high period of the acknowledge-related clock pulse. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate the stop condition.

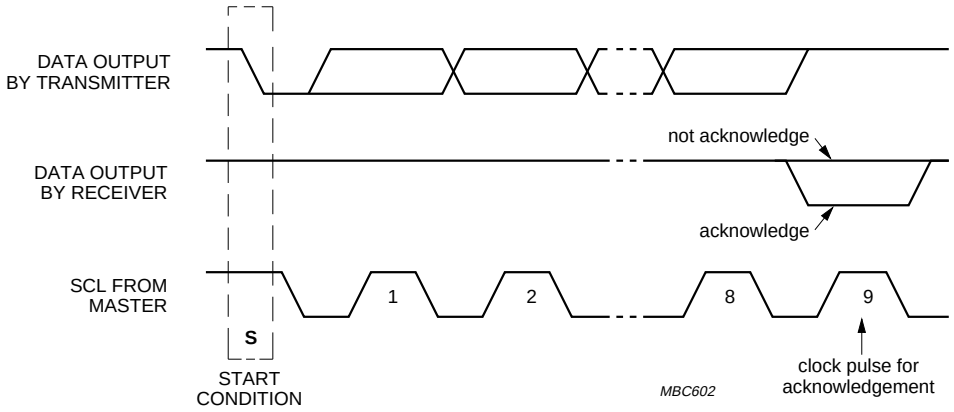


Fig.9 Acknowledgment on the I^2C-bus.

8.5 Timing specifications

The PCD4440T accepts data input from a microcontroller and operates as a ‘slave receiver’ via the I²C-bus. It supports the ‘standard’ mode of the I²C-bus, but not the ‘fast’ mode detailed in *“The I²C-bus and how to use it”* document order no. 9398 393 40011. The timing requirement are as follows:

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10, where the two signal levels are LOW = V_{IL} and HIGH = V_{IH}, see Chapter 12. The time symbols are explained in Table 2. Figure 11 shows a complete data transfer.

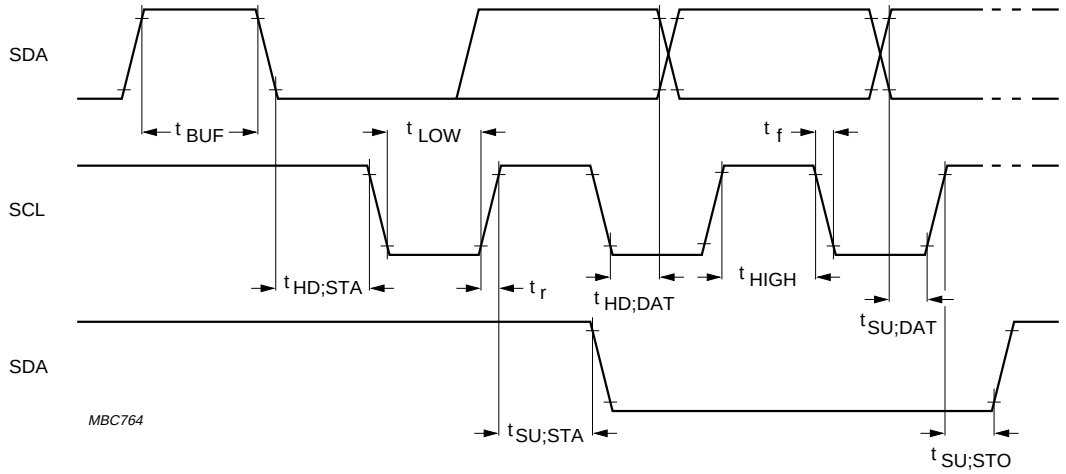
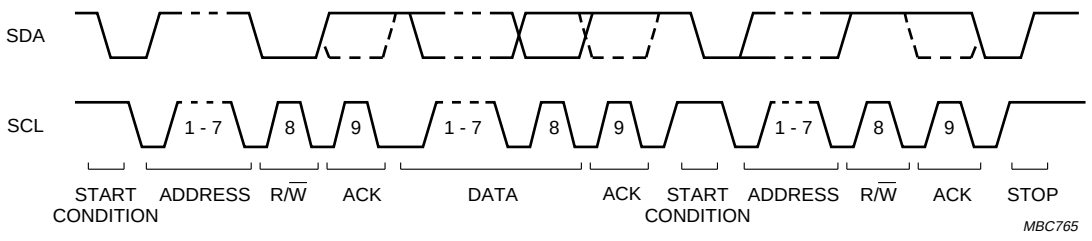


Fig.10 Standard mode timing.



Clock LOW minimum = 4.7 μs; clock HIGH minimum = 4 μs.
The dashed line is the acknowledgment of the receiver.
Mark-to-space ratio = 1 : 1 (LOW-to-HIGH).
Maximum number of bytes is unrestricted.
Premature termination of transfer is allowed by generation of STOP condition.
Acknowledge clock bit must be provided by master.

Fig.11 Complete data transfer in standard mode.

Table 2 Explanation of time symbols used in Fig.10

SYMBOL	PARAMETER	DESCRIPTION	MIN.	MAX.	UNITS
f_{SCL}	SCL clock frequency		0	100	kHz
t_{SW}	tolerable pulse spike width		–	100	ns
t_{BUF}	bus free time	The time that the bus is free (SDA is HIGH) before a new transmission is initiated by SDA going LOW.	4.7	–	µs
$t_{SU;STA}$	set-up time repeated START	Only valid for repeated start code.	4.7	–	µs
$t_{HD;STA}$	hold time START condition	The time between SDA going LOW and the first valid negative-going transition of SCL.	4.0	–	µs
t_{LOW}	SCL LOW time	The LOW period of the SCL clock.	4.7	–	µs
t_{HIGH}	SCL HIGH time	The HIGH period of the SCL clock.	4.0	–	µs
t_r	rise time SDA and SCL		–	1.0	µs
t_f	fall time SDA and SCL		–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	set-up time STOP condition		4.0	–	µs

9 APPLICATIONS

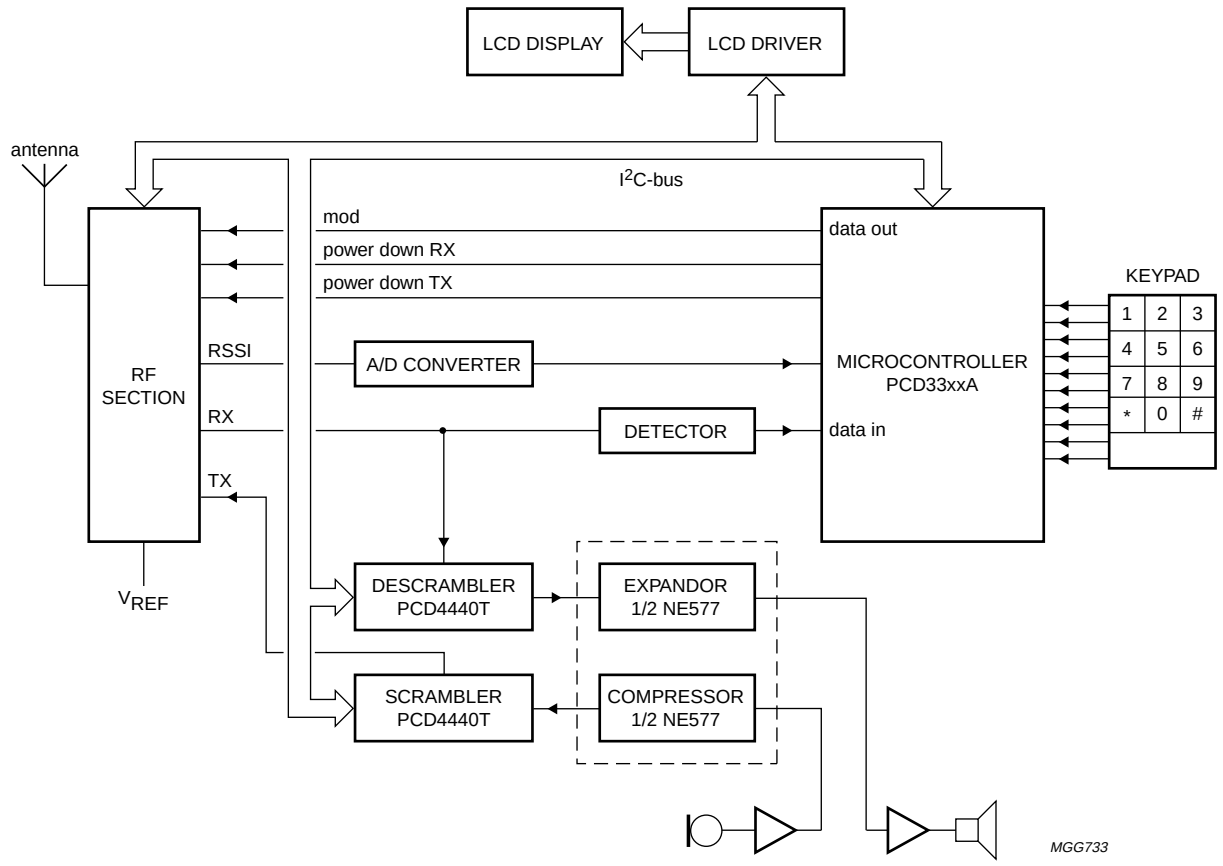


Fig.12 CT0 handset with direct (Manchester code) data system.

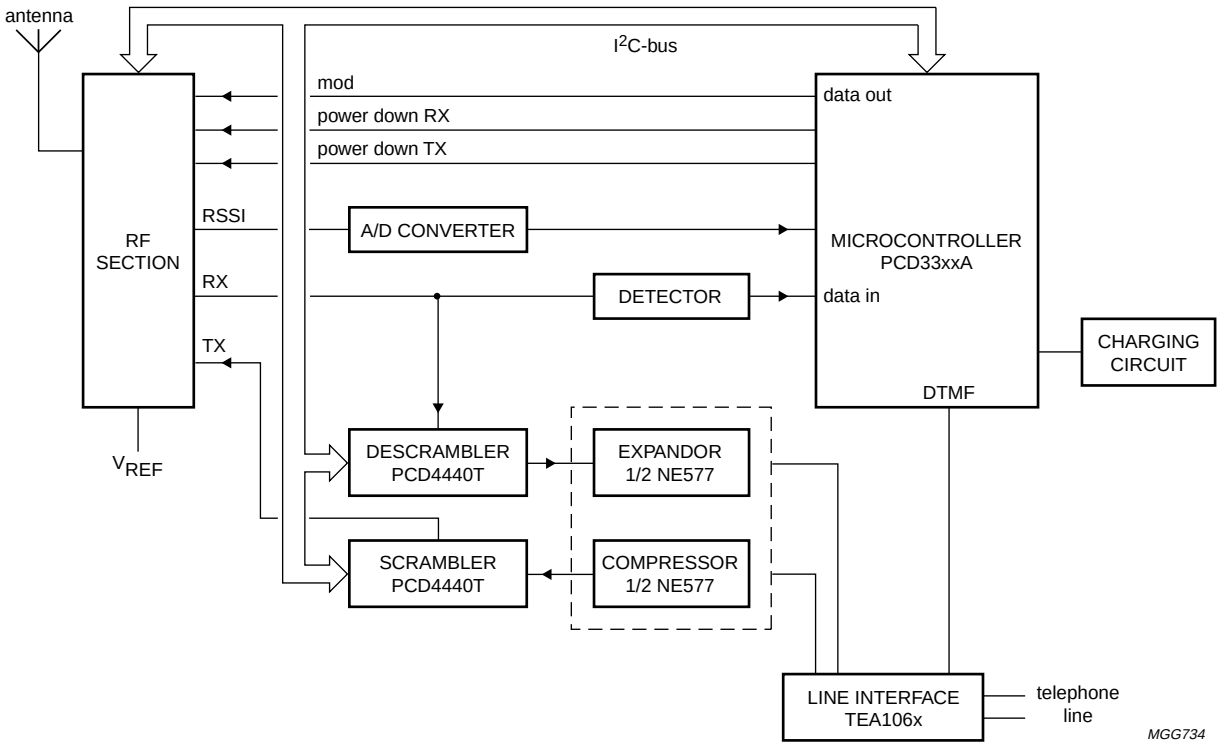


Fig.13 CT0 base unit with direct (Manchester code) data system.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handbook IC03, Section General, Handling MOS devices"*).

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.3	+7.0	V
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−20	+20	mA
P_{tot}	total power dissipation	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

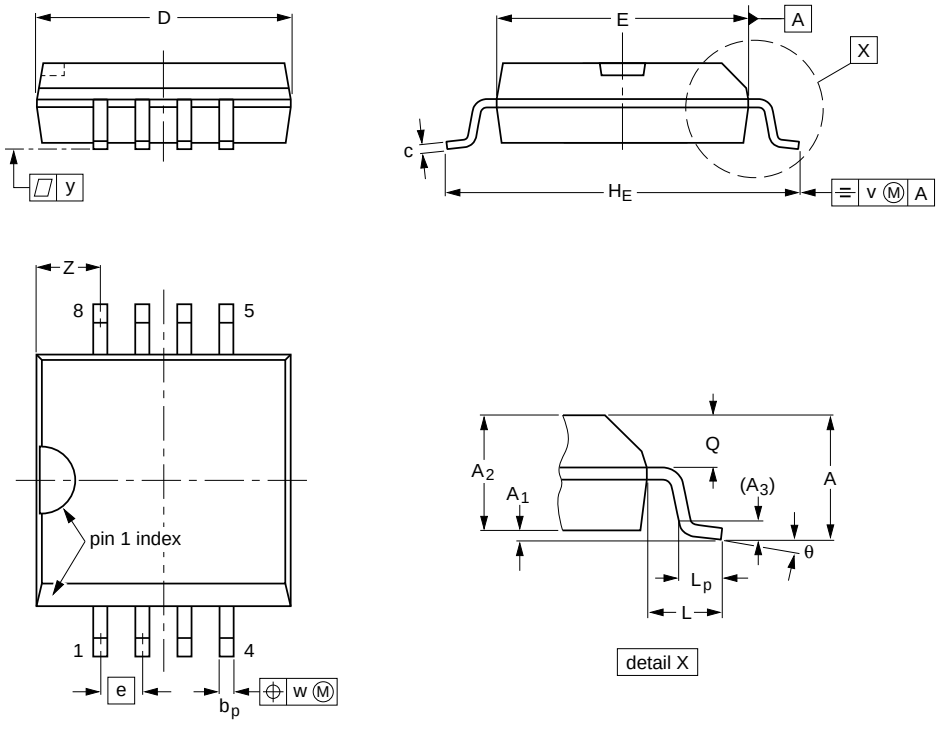
12 CHARACTERISTICS

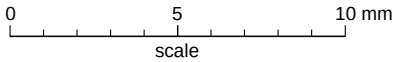
V_{DD} = 5.0 V; V_{SS} = 0 V; T_{amb} = 25 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.579 MHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.8	–	6.0	V
I_{DD}	supply current					
	mute mode	V_{DD} = 3 V	–	2.2	–	mA
	operating mode	V_{DD} = 3 V	–	13	–	mA
Inputs/Outputs: AO, SDA, SCL						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
C_i	input capacitance		–	–	7	pF
I_{OL}	SDA output current LOW	V_{OL} = 0.4 V	3.0	–	–	mA
Signal input: IN						
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$V_{i(P-P)}$	allowed amplitude		–	1.25	V_{DD} − 1	V
$\|Z_i\|$	input impedance	frequency = 1 kHz	–	120	–	kΩ
Signal output: OUT						
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\|Z_o\|$	output impedance	frequency = 1 kHz	–	–	1	kΩ
UFS	unwanted frequency suppression	$V_{i(P-P)}$ = 1.25 V; f_S = 767 or 2461 Hz; f_{in} = 1 kHz; V_{DD} = 3 V or 5 V	35	40	–	dB
V_o/V_i	transfer loss	transparent mode	–	3.5	–	dB
		operating mode	–	0	–	dB
Oscillator frequency input: OSCI						
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V

13 PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.42 0.39	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~91-08-13~~ 95-02-25

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

14.2 Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3 Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

17 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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