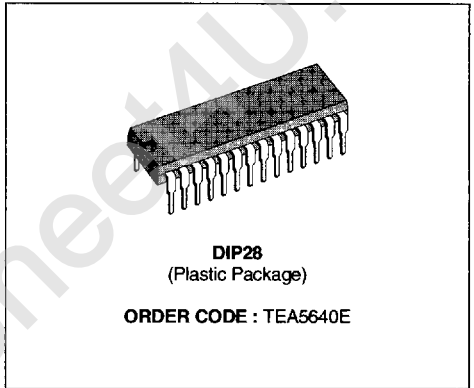




**MULTISTANDARD COLOR TV DECODER**

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL AND NTSC OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

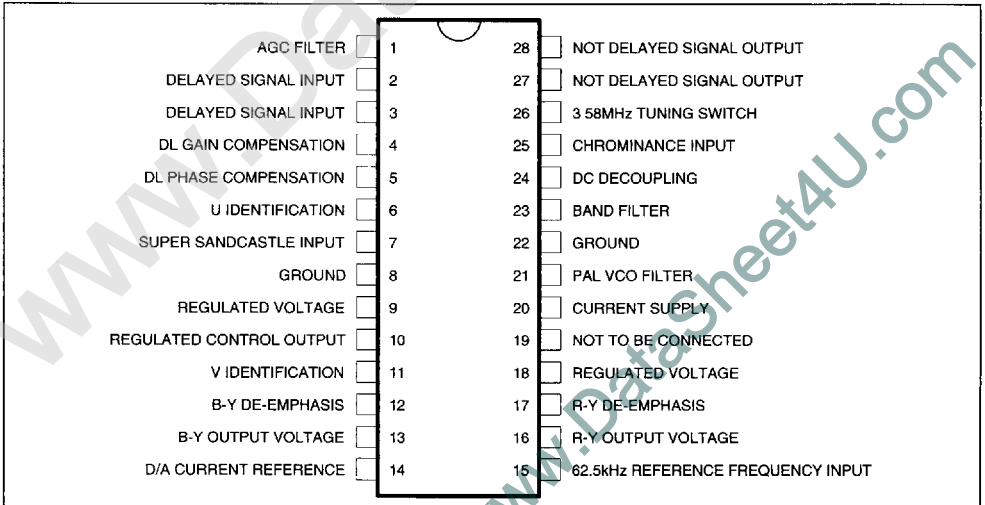
duces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are four numerical frequency locked loops that allow the elimination of PAL and NTSC crystals. The circuit uses an external reference frequency of 62.5kHz generally provided by the frequency synthesis tuner of the TV set.



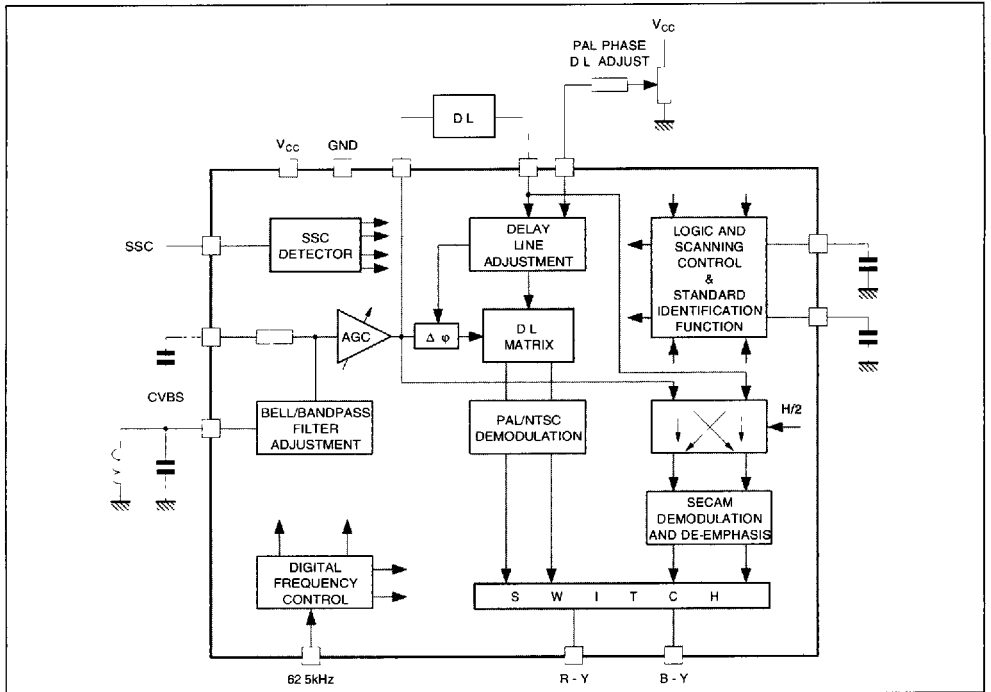
**DESCRIPTION**

The TEA5640E is a multistandard TV decoder for PAL-SECAM NTSC1 (3.58MHz) and NTSC2 (4.43MHz). The circuit automatically selects the standard corresponding to the input signal. It pro-

**PIN CONNECTIONS**



## BLOCK DIAGRAM (simplified)



## FEATURES

- Full automatic multistandard switching :  
The circuit includes a scanning control system that provides all the switchings required for the automatic standard recognition. This system is synchronized by the frame pulse.
- No crystal requirement :  
The PAL and NTSC frequencies are synthesized originally by the external reference frequency of 62.5kHz and data stored in the ROM.
- Automatic gain adjustment of the bell filter :  
By switching an internal capacitor network included in a digital loop.
- Automatic gain adjustment of the delay line compensations :  
This adjustment is made on the burst and is refreshed every line retrace
- Automatic adjustment for PAL and NTSC oscillator :  
This oscillator has a digital and an analogic loop. the PAL and NTSC frequencies are memorized in a ROM connected to the digital loop. The digital loop gives the right frequency and the analogic one holds the phase.

- Automatic adjustment of F0R and F0B in SECAM :  
These frequencies are programmed in the ROM and are sent to two other digital loops when SECAM standard is selected.
- Automatic difference phase error compensation in PAL mode.  
The PAL VCO is locked on the burst and during the line, on the blue picture content (0° axis color vector).

## STANDARD SWITCHING AND INHIBITION

## NTSC inhibition

NTSC 1 and 2 standards can be inhibited by connecting pin 6 to the ground.

## 3.58 MHz filter switching :

Pin 26 can be used to switch external filters when NTSC 1 is selected (For example luma filter).

## SECAM recognition :

- When SECAM on, Pin 12 and Pin 17 DC voltages are lower than 5V.
- For other standards, Pin 12 and Pin 17 DC voltages are regulated Vcc (typical 8V).

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V	Supply Voltage Pins 9 - 18	9.5	V
I	Current Pin 20	200	mA
T <sub>oper</sub>	Operating Temperature Range	0, +70	°C
T <sub>stg</sub>	Storage Temperature	- 40, +150	°C

5640E 01 TEL

## THERMAL DATA

Symbol	Parameter	Value	Unit
R <sub>th (j-a)</sub>	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

5640E 02 TEL

## ELECTRICAL CHARACTERISTICS

T<sub>amb</sub> = 25 °C ; V<sub>CC</sub> = 12V ; With Normalized Color Bar Pattern Input Signal (75%)Subcarrier Level : 320mV<sub>PP</sub>

Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
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## SUPPLIES

V <sub>REG</sub>	Regulated Voltage I <sub>10</sub> = 4mA	Pins 9-18	7.5	8	8.5	V
I <sub>CC</sub>	Supply Current	Pin 9 + Pin 18		90	120	mA
I <sub>9</sub>	Supply Current	Pin 9			90	mA
I <sub>18</sub>	Supply Current	Pin 18			27	mA
V <sub>12L</sub>	DC Voltage at I <sub>20</sub> = 15mA	Pin 20		0.8		V
I <sub>10</sub>	Input Current	Pin 10	2	4	5	mA
	Transfer Characteristic (I <sub>10</sub> = 4.0mA)			250		mA/V

## CURRENT REFERENCE (Pin 14)

V <sub>14</sub>	DC Voltage (I <sub>14</sub> = 0.77mA)	1.2	1.4	1.6	V
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## INTERNAL BIAS (Pin 24)

V <sub>24</sub>	DC Voltage	3.7	4.2	4.7	V
	Impedance (I <sub>out</sub> = 2mA)		90	110	Ω

## REFERENCE CLOCK INPUT (f = 62.5kHz ± 6Hz, Pin 15)

I <sub>15L</sub>	Low Level Input Current (V <sub>15</sub> = 2.1V)	- 20	- 10	- 5	μA
I <sub>15H</sub>	High Level Input Current (V <sub>15</sub> = 3.2V)		5	10	μA
V <sub>15L</sub>	Low Level Input Voltage	R <sub>Source</sub> = 68kΩ		1	V
V <sub>15H</sub>	High Level Input Voltage	R <sub>Source</sub> = 68kΩ	4		V
	Voltage Threshold		2.8		V

## SUPER SANDCASTLE DETECTOR (Pin 7)

V <sub>B</sub>	Blanking Threshold	0.5	0.75	0.9	V
V <sub>L</sub>	Line Threshold	1.6	1.8	1.9	V
V <sub>6</sub>	Burst Gate Threshold	3.2	3.5	3.8	V
	Minimum Frame Blanking Duration	1.15			mS
I <sub>7</sub>	Input Current (V <sub>7</sub> = 1.75V)	- 20		0	μA
	Max Input Voltage Pin 7			6.0	V

## CHROMINACE INPUT (Pin 25)

V <sub>25</sub>	DC Voltage		5.5		V
	Maximum AC Input Voltage			0.64	V <sub>PP</sub>
	Impedance	0.8	1		kΩ

5640E 03 TEL

## ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
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## AUTOMATIC GAIN CONTROL

SECAM MODE					
	0dB Reference Voltage for Measurement on Pins 27-28 (chroma input voltage $V_{25} = 320\text{mV}_{PP}$ )	50	150	250	$\text{mV}_{PP}$
	AC Voltage Variation on Pins 27-28 $V_{25} = + 6\text{dB}$ $V_{25} = - 24\text{dB}$	- 3 - 5		+ 3 + 2	dB dB
PAL/NTSC MODE WITH IDENTIFICATION					
	0dB Reference Voltage for Measurement on Pins 13-16 (chroma input voltage $V_{25} = 320\text{mV}_{PP}$ )				
	AC Voltage Variation on Pins 13-16 $V_{25} = + 6\text{dB}$ $V_{25} = - 24\text{dB}$	- 3 - 5		+ 3 + 2	dB dB

## DEMODULATOR PART

GENERALITIES						
$V_{13}$	B-Y Output DC Voltage	Pin 13	2.7	3.3	4	V
$V_{16}$	R-Y Output DC Voltage	Pin 16	3.0	3.5	4.2	V
	Maximum Sink Current	Pins 13-16	0.4			mA
	Differential Delay Time Between PAL/SECAM				50	nS
	Delay Diff Tolerance				50	nS
	Delay Between Chroma Output and Luma Signal			450		nS
	B-Y Output AC Impedance ( $\pm 50\mu\text{A}$ )			250		$\Omega$
	R-Y Output AC Impedance ( $\pm 50\mu\text{A}$ )			250		$\Omega$
	Blanking Level Offset (% of the pp output signal)				$\pm 2$	%

## SECAM MODE

$V_{BYS}$	B-Y AC Voltage	1.0	1.34	1.6	$V_{PP}$
$V_{RYS}$	R-Y AC Voltage	0.8	1.05	1.3	$V_{PP}$
	B-Y/R-Y Ratio	1.1		1.45	
	Residual Subcarrier		30		$\text{mV}_{PP}$
	Max overshoot on output SECAM signals (see test conditions Note 2)			5	%
	SECAM Rise Time (see test conditions Note 1)			800	ns

## PAL MODE

$V_{BYP}$	B-Y AC Voltage	1.0	1.34	1.6	$V_{PP}$
$V_{RYP}$	R-Y AC Voltage	0.8	1.05	1.3	$V_{PP}$
	B-Y/R-Y Ratio	1.1		1.45	
	Residual Subcarrier		30		$\text{mV}_{PP}$

## PAL/SECAM OUTPUT BALANCE

RYPs	R-Y Output			$\pm 2$	dB
BYPs	B-Y Output			$\pm 2$	dB

## NTSC 4.43

$V_{BYN2}$	B-Y AC Voltage	1.0	1.34	1.6	$V_{PP}$
$V_{RYN2}$	R-Y AC Voltage	0.8	1.05	1.3	$V_{PP}$
	B-Y/R-Y Ratio	1.1		1.45	
	Residual Subcarrier		50		$\text{mV}_{PP}$

## Notes :

## 1. Rise Time Test Conditions

- SECAM Color Bar Patterns 75%
- Generator TEKTRONIX 143
- Standard Application without any output load
- Measure between 10% and 90% on the major transition (Green Violet)

## 2. Overshoot Test Conditions

- Idem than for Rise Time
- Ratio between the value of the overshoot and the peak-to-peak value of the transition after overshoot (on the flat level)

## ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
NTSC 3.58					
V <sub>BYN1</sub>	B-Y AC Voltage	1.0		1.6	V <sub>PP</sub>
V <sub>RYN1</sub>	R-Y AC Voltage	0.8		1.3	V <sub>PP</sub>
	B-Y/R-Y Ratio	1.1		1.45	
	Residual Subcarrier		50		mV <sub>PP</sub>

## DE-EMPHASIS (Pins 12-17)

	DC Voltage SECAM Mode (blanking level)		3.5	4.0	V
	Impedance SECAM Mode		11		kΩ
	DC Voltage PAL NTSC Mode		V <sub>REG</sub>		V
	Impedance PAL Mode		70		kΩ

## REFERENCE OSCILLATOR PLL

	Catching Range in PAL Mode	± 350			Hz
	Holding Range	± 500			Hz

## BAND FILTER (Pin 23)

	Impedance SECAM Mode	3.7	4.7	5.7	kΩ
	Impedance PAL/NTSC Mode	0.85	1.1	1.35	kΩ
	Minimum Switchable Internal Capacitance (all standards)		20		pF
	Maximum Switchable Internal Capacitance (all standards)		50		pF
ΔF	Internal Oscillator Frequency Range for (L = 10μH, C = 68pF)	590			kHz
	frequency Offset, After Automatic Adjustment			± 10	kHz

## UNDELAYED SIGNAL OUTPUTS (Pins 27-28)

V <sub>27</sub> , V <sub>28</sub>	DC Voltage		1.6		V
I <sub>27</sub> , I <sub>28</sub>	Sink Current	1			mA
	Impedance		30		Ω

## IDENTIFICATION

BURST ATTENUATION RANGE / NOMINAL LEVEL					
	SECAM Mode (line identification)	30			dB
	PAL Mode	30			dB
	NTSC Modes	20			dB
SECAM MODE					
V <sub>26</sub>	Pin 26 Voltage (unloaded)	6.9	7.8	8.5	V
V <sub>26</sub>	Pin 26 Impedance	5	13	25	kΩ
PAL AND NTSC 4.43 MODES					
V <sub>26</sub>	Pin 26 Voltage (unloaded)	3.6	4.2	4.9	V
V <sub>26</sub>	Pin 26 Impedance	2	6	15	kΩ
NTSC 3.58 MODE					
V <sub>26</sub>	Pin 26 Voltage (unloaded)		0.0	0.3	V
V <sub>26</sub>	Pin 26 Impedance		0.1	1	kΩ

## TINT CONTROL (NTSC Modes)

	Range of Phase Change for V <sub>Pin 5</sub> Changing from 2 to 4.5V		± 40		degree
V <sub>5</sub>	DC Voltage for 0 Degree TINT Change	Pin 5	3.5		V
I <sub>5</sub>	Input Current	Pin 5	0.08	0.2	mA

## NTSC DETECTION

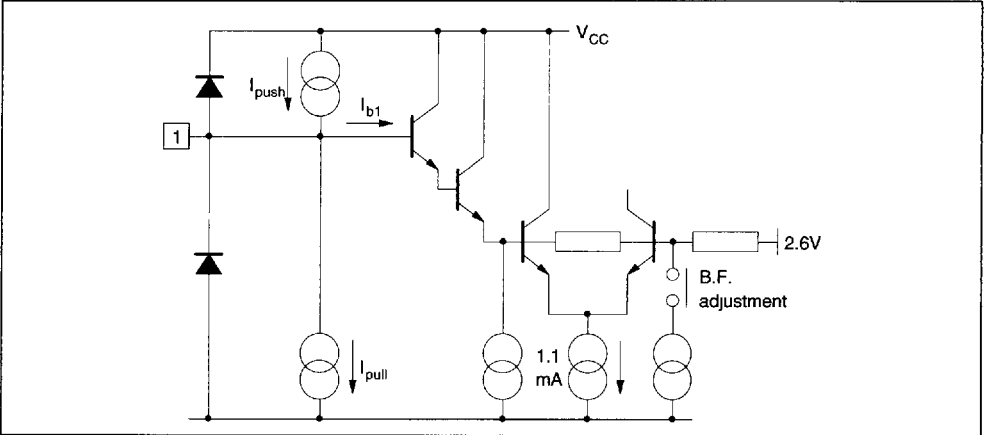
	Detection Threshold	Pin 6	3	3.5	4	V
	NTSC Mode Inhibition Threshold		0.5		2.5	V
	Leakage Current			0.5		μA

**ELECTRICAL CHARACTERISTICS** (continued)

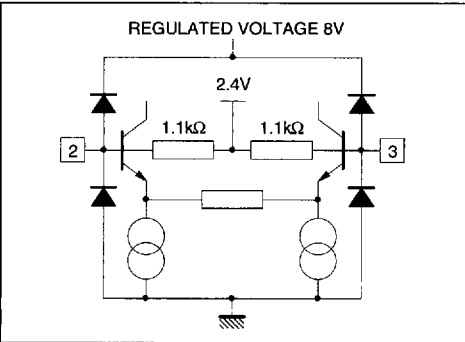
Symbol	Parameter	Min.	Typ.	Max.	Unit
<b>DELAYED SIGNAL INPUT (Pins 2-3)</b>					
	DC Voltage in PAL Mode		2.4		V
	Input Impedance	0.88	1.1	1.32	kΩ
<b>DELAY LINE ATTENUATION COMPENSATION</b>					
	Range of Automatic Attenuation Compensation	-3	-9	-15	dB
<b>DELAY LINE PHASE SHIFT COMPENSATION</b>					
	Range of Phase Shift Compensation with a 100kΩ Potentiometer (see application diagram)	± 30			degree
<b>ALTERNATION LINE DETECTION PAL OR SECAM (Pin 11)</b>					
V <sub>TH-H</sub>	High Differential Threshold (V <sub>TH-H</sub> = V <sub>11H</sub> - V <sub>24</sub> )	200		350	mV
V <sub>TH-L</sub>	Low Differential Threshold (V <sub>TH-L</sub> = V <sub>11L</sub> - V <sub>24</sub> )	-350		-200	mV
	Leakage Current Threshold (V <sub>11</sub> = V <sub>24</sub> + 1V)			0.5	μA

**INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS**

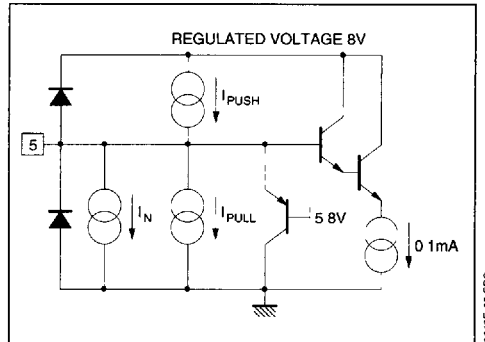
Pin 1



Pins 2-3

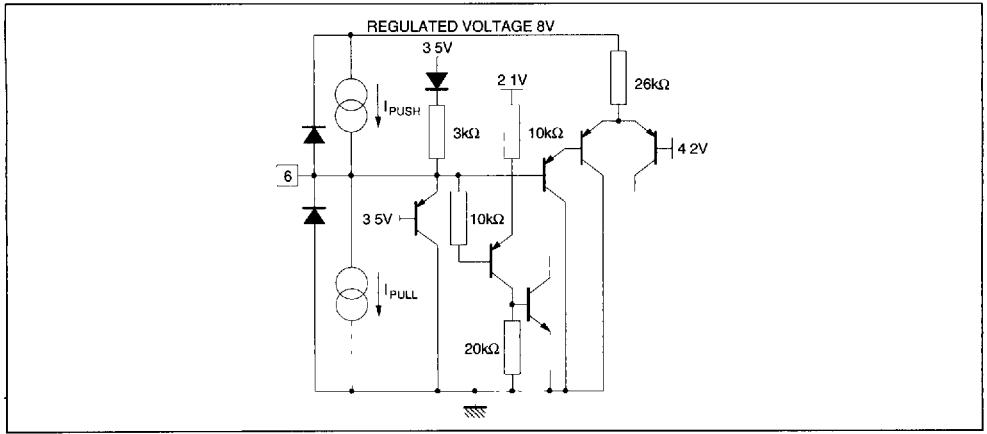


Pin 5



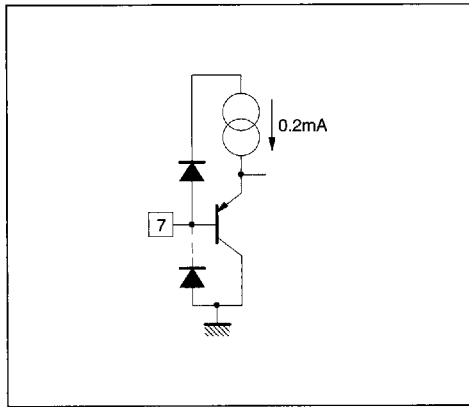
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

Pin 6



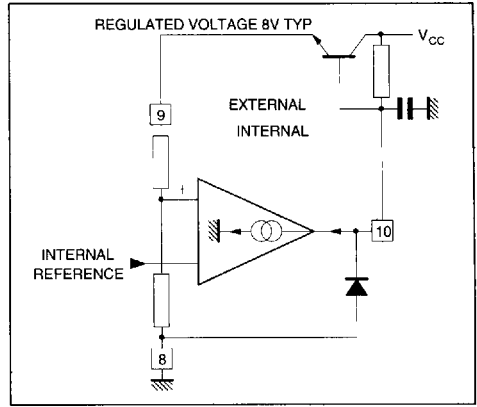
5640E 06 EPS

Pin 7



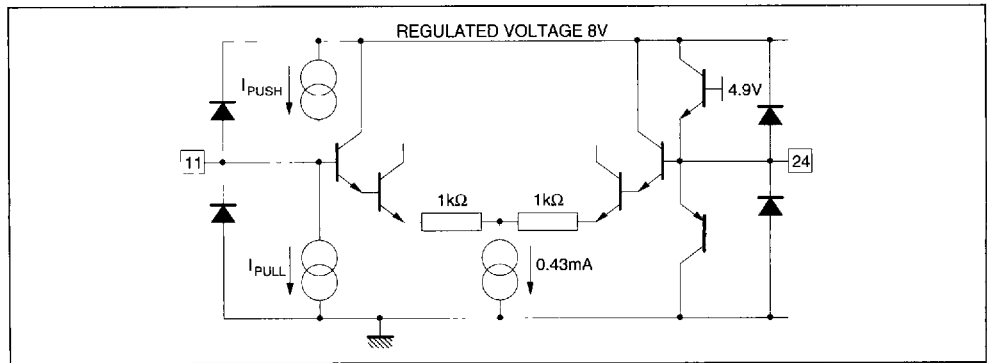
5640E 07 EPS

Pins 8-9-10



5640E 08 EPS

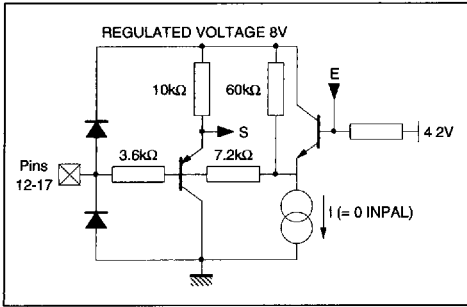
Pins 11-24



5640E 09 EPS

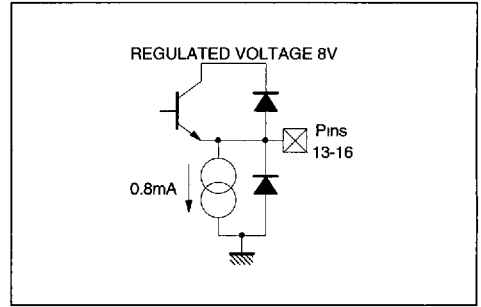
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

Pins 12-17



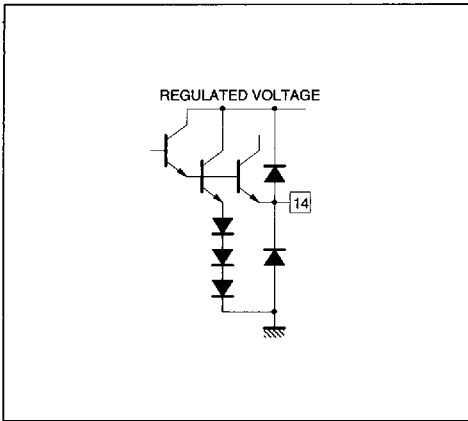
5640E-10 EPS

Pins 13 - 16



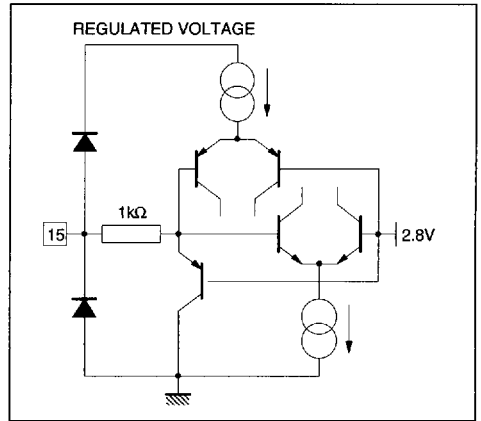
5640E-11 EPS

Pin 14



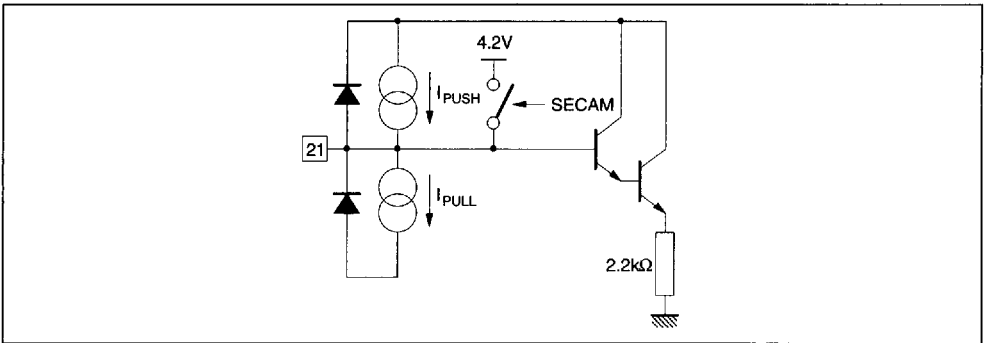
5640E-12 EPS

Pin 15



5640E-13 EPS

Pin 21

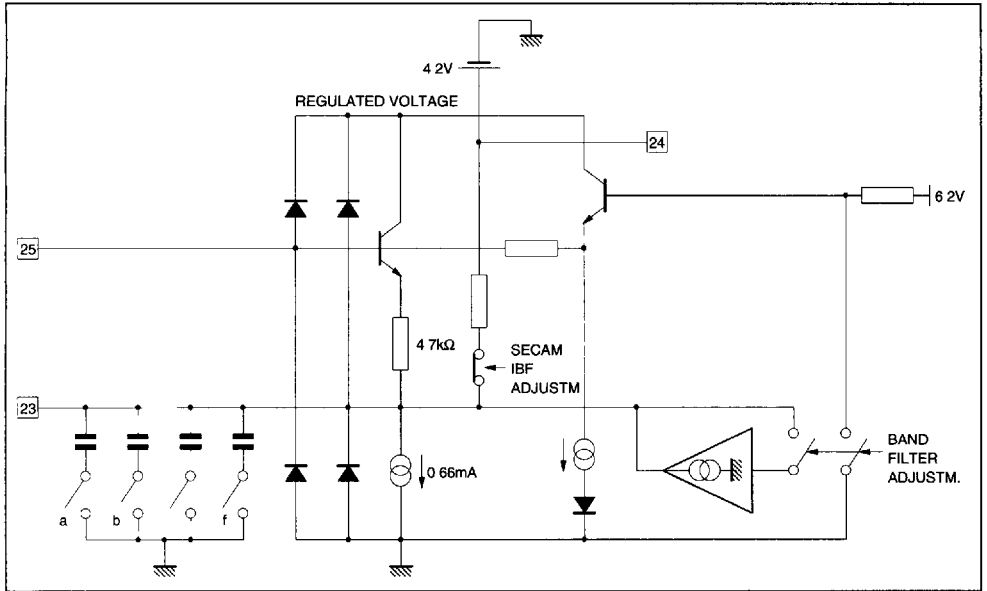


5640E-14 EPS



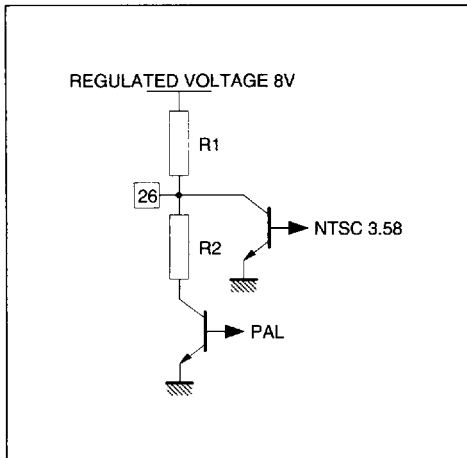
## INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

Pins 23-24-25



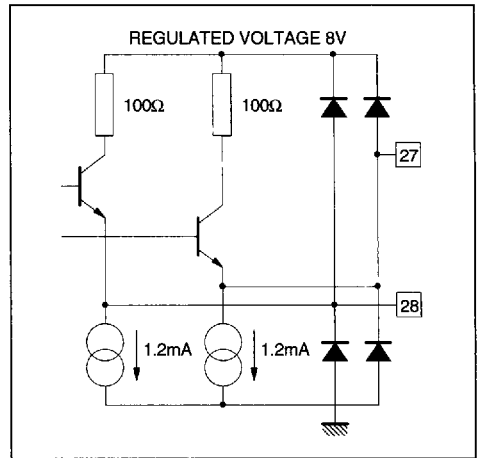
5640E 15 EFS

Pin 26



5640E 16 EFS

Pins 27 - 28



5640E 17 EFS



