

# OKI semiconductor

## MSM51C256RS/JS

T-46-23-15

262, 144 WORD X 1-BITS DYNAMIC RAM

### GENERAL DESCRIPTION

The MSM51C256 is a new generation dynamic RAM organized as 262,144 words by 1 bit. The technology used to fabricate the MSM51C256 is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

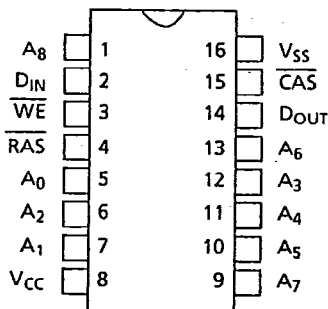
### FEATURES

- Silicon gate, double polysilicon CMOS, 1-transistor memory cell
- Standard 16 lead plastic DIP/18 lead PLCC
- 262,144 words by 1 bit
- Family organization

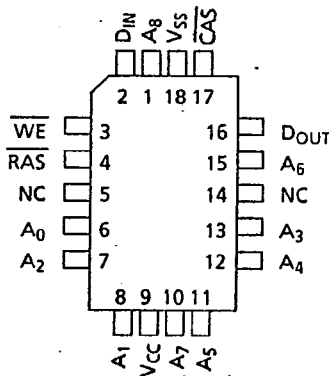
Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM51C256-8	80 ns	145 ns	330 mW	20 mW
MSM51C256-10	100 ns	175 ns	275 mW	
MSM51C256-12	120 ns	205 ns	248 mW	

- Single +5V supply,  $\pm 10\%$  tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 256 cycles/4 ms
- Common I/O capability using "Early Write" operation
- Fast page mode, read/write capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  hidden refresh, RAS only refresh capability
- "Gated"  $\overline{\text{CAS}}$
- Built-in  $V_{\text{BB}}$  generator circuit

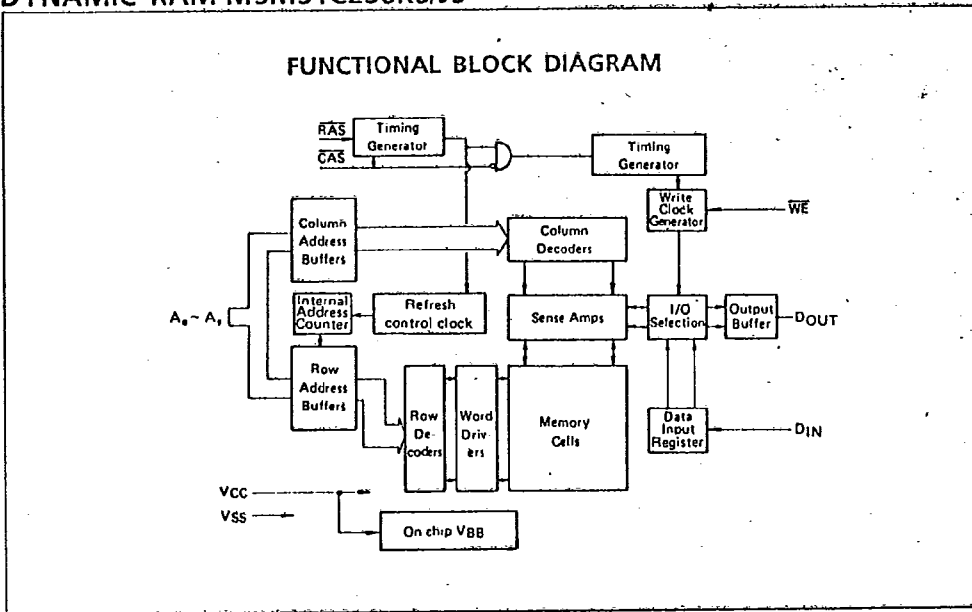
MSM51C256RS  
16 Lead Plastic DIP PIN CONFIGURATION  
Top View



MSM51C256JS  
18 Lead PLCC Package PIN CONFIGURATION  
Top View



DYNAMIC RAM-MSM51C256RS/JS



ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Rating	Symbol	Condition	Value	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	T <sub>a</sub> = 25°C	- 1.0 to + 7.0	V
Short circuit output current	I <sub>OS</sub>	T <sub>a</sub> = 25°C	50	mA
Power dissipation	P <sub>D</sub>	T <sub>a</sub> = 25°C	1	W
Operating temperature	T <sub>opr</sub>	-	0 to + 70	°C
Storage temperature	T <sub>stg</sub>	-	- 55 to + 125	°C

● Recommended Operating Conditions  
(T<sub>a</sub> = 0 to + 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	-	4.5	5.0	5.5	V
	V <sub>SS</sub>	-	0	0	0	V
Input high voltage	V <sub>IH</sub>	-	2.4	-	V <sub>CC</sub> + 1.0	V
Input low voltage	V <sub>IL</sub>	-	- 1.0	-	0.8	V

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● DC Characteristics

( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0$  to  $+70^\circ C$ )

Parameter	Symbol	Conditions	MSM51C256 -8		MSM51C256 -10		MSM51C256 -12		Unit	Note	
			Min	Max	Min	Max	Min	Max			
Output high voltage	$V_{OH}$	$I_{OH} = -5.0mA$	2.4	-	2.4	-	2.4	-	V		
Output low voltage	$V_{OL}$	$I_{OL} = 4.2mA$	-	0.4	-	0.4	-	0.4	V		
Input leakage current	$I_{LI}$	$V_{SS} \leq V_I \leq V_{CC}$ all other pins not under test = 0V	-10	10	-10	10	-10	10	$\mu A$		
Output leakage current	$I_{LO}$	$D_{OUT}$ disable $V_{SS} \leq V_O \leq V_{CC}$	-10	10	-10	10	-10	10	$\mu A$		
Average power supply current* (Operating)	$I_{CC1}$	$\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = \min$	-	60	-	50	-	45	mA		
Power supply current* (Standby)	$I_{CC2}$	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IH}$ $D_{OUT} = Hz$	TTL	-	3.5	-	3.5	-	3.5	mA	
			MOS	-	2.5	-	2.5	-	2.5	mA	
Average power supply current* (RAS only refresh)	$I_{CC3}$	$\overline{RAS} = \text{cycling}$ , $\overline{CAS} = V_{IH}$ $t_{RC} = \min$	-	60	-	50	-	45	mA		
Average power supply current* (CAS before RAS refresh)	$I_{CC6}$	$\overline{RAS} = \text{cycling}$ , $\overline{CAS}$ before RAS	-	60	-	50	-	45	mA		
Average power supply current* (Fast page mode)	$I_{CC7}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS} = \text{cycling}$ $t_{PC} = \min$	-	40	-	35	-	30	mA		

\*Note:  $I_{CC}$  is dependent on output loading and cycle. Specified values are obtained with the output open.

● Capacitance

( $T_a = 25^\circ C$ ,  $f = 1 MHz$ )

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance ( $A_0$ to $A_8$ , $D_{IN}$ )	$C_{IN1}$	-	-	4	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	$C_{IN2}$	-	-	5	pF
Output capacitance ( $D_{OUT}$ )	$C_{OUT}$	-	-	6	pF

● AC Characteristics

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to +70°C)

Note 1, 2, 3

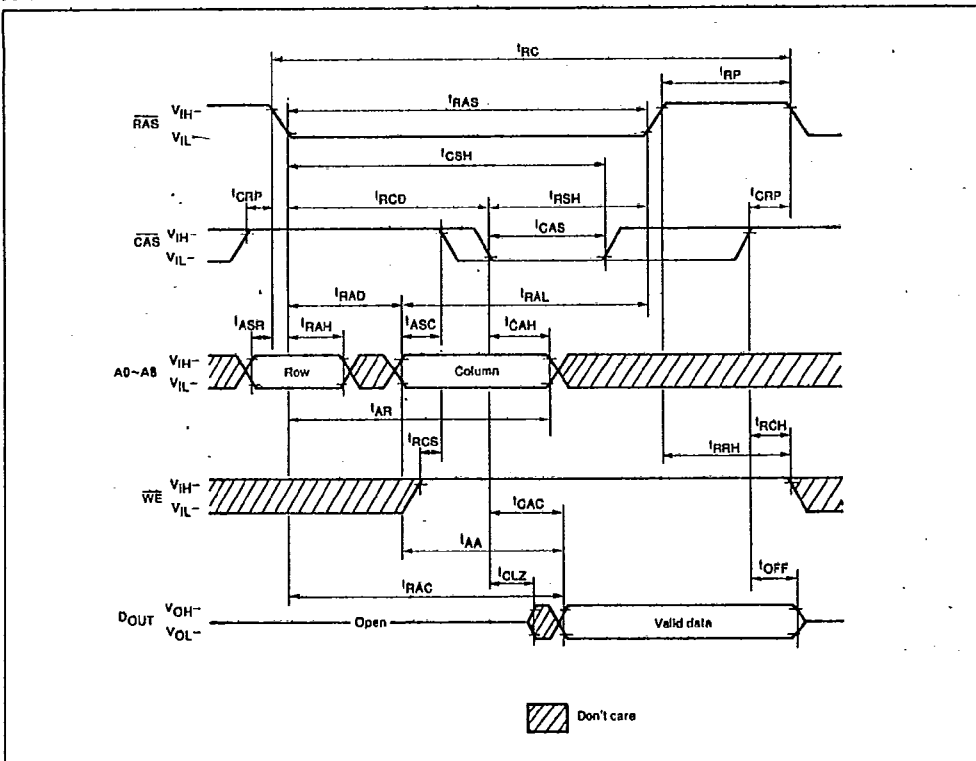
Parameter	Symbol	MSM51C256 -8		MSM51C256 -10		MSM51C256 -12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Refresh period	t <sub>REF</sub>	-	4	-	4	-	4	ms	
Random read or write cycle time	t <sub>RC</sub>	145	-	175	-	205	-	ns	
Read/write cycle time	t <sub>RWC</sub>	180	-	210	-	245	-	ns	
Fast page mode cycle time	t <sub>PC</sub>	55	-	60	-	70	-	ns	
Fast page mode read/write cycle time	t <sub>PRWC</sub>	85	-	95	-	110	-	ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	-	80	-	100	-	120	ns	4.5
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	-	20	-	25	-	30	ns	4.5
Access time from column address	t <sub>AA</sub>	-	40	-	45	-	55	ns	4.6
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>	-	50	-	55	-	65	ns	4
Output low impedance time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	-	0	-	0	-	ns	4
Output buffer turn-off delay	t <sub>OFF</sub>	0	20	0	25	0	30	ns	
Transition time	t <sub>T</sub>	3	50	3	50	3	50	ns	3
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	55	-	65	-	75	-	ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	80	16K	100	16K	120	16K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	25	-	30	-	35	-	ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode cycle only)	t <sub>CP</sub>	15	-	20	-	25	-	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	25	16K	30	16K	35	16K	ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	80	-	100	-	120	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCDD</sub>	25	60	25	75	25	90	ns	5
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	20	40	20	55	20	65	ns	6
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	15	-	15	-	20	-	ns	
Row address set-up time	t <sub>ASR</sub>	0	-	0	-	0	-	ns	
Row address hold time	t <sub>RAH</sub>	15	-	15	-	15	-	ns	
Column address set-up time	t <sub>ASC</sub>	0	-	0	-	0	-	ns	
Column address hold time	t <sub>CAH</sub>	15	-	20	-	25	-	ns	

● AC Characteristics (Cont.)

Parameter	Symbol	MSM51C256 -8		MSM51C256 -10		MSM51C256 -12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Column address hold time from $\overline{\text{RAS}}$	$t_{AR}$	65	-	70	-	80	-	ns	
Column address to $\overline{\text{RAS}}$ lead time	$t_{RAL}$	40	-	45	-	55	-	ns	
Read command set-up time	$t_{RCS}$	0	-	0	-	0	-	ns	
Read command hold time	$t_{RCH}$	0	-	0	-	0	-	ns	8
Write command hold time from $\overline{\text{RAS}}$	$t_{WCR}$	65	-	70	-	80	-	ns	
Write command set-up time	$t_{WCS}$	0	-	0	-	0	-	ns	7
Write command hold time	$t_{WCH}$	15	-	20	-	25	-	ns	
Write command pulse width	$t_{Wp}$	15	-	20	-	25	-	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{RWL}$	25	-	30	-	35	-	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{CWL}$	25	-	30	-	35	-	ns	
Data-in set-up time	$t_{DS}$	0	-	0	-	0	-	ns	
Data-in hold time	$t_{DH}$	15	-	20	-	25	-	ns	
Data-in hold time from $\overline{\text{RAS}}$	$t_{DHR}$	65	-	70	-	80	-	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	$t_{CWD}$	20	-	25	-	30	-	ns	7
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	$t_{RWD}$	85	-	100	-	120	-	ns	7
Column address to $\overline{\text{WE}}$ delay time	$t_{AWD}$	40	-	45	-	55	-	ns	7
Read command hold time reference to $\overline{\text{RAS}}$	$t_{RRH}$	10	-	10	-	10	-	ns	8
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	$t_{CSR}$	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	$t_{CHR}$	25	-	30	-	40	-	ns	
$\overline{\text{CAS}}$ active delay from $\overline{\text{RAS}}$ precharge	$t_{RPC}$	0	-	0	-	0	-	ns	
$\overline{\text{CAS}}$ precharge time (Refresh counter test)	$t_{CPT}$	45	-	50	-	60	-	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CPN}$	15	-	20	-	25	-	ns	

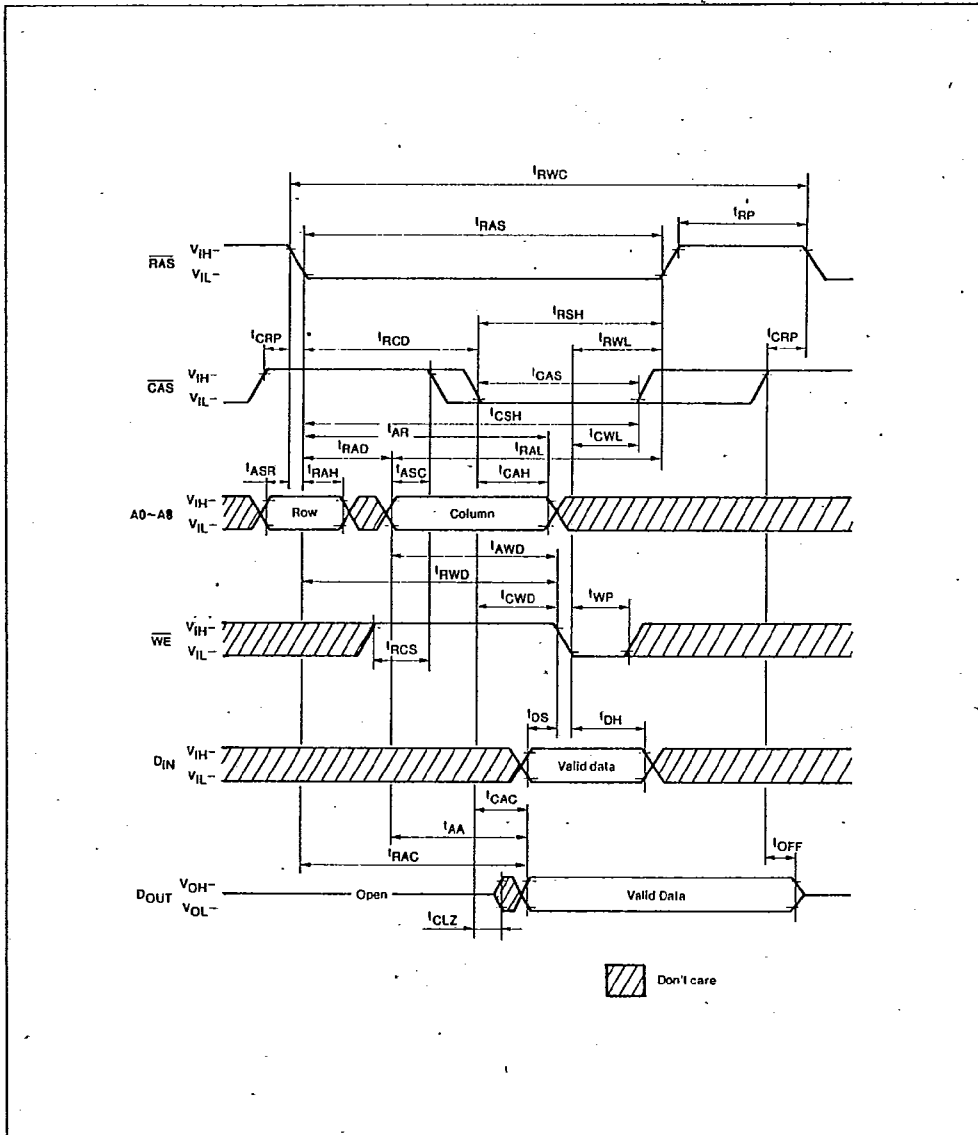
- Notes:
1. An initial pause of 100  $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles (Example:  $\overline{\text{RAS}}$  only) before proper device operation is achieved.
  2. The AC characteristics assume at  $t_T = 5$  ns.
  3.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. Measured with a load circuit equivalent to 2TTL + 100 pF.
  5. Operation within the  $t_{RCD}$  (max.) limit insures that  $t_{RAC}$  (max.) can be met.  $t_{RCD}$  (max.) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.) limit, then access time is controlled exclusively by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (max.) limit insures that  $t_{RAC}$  (max.) can be met.  $t_{RAD}$  (max.) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, then access time is controlled exclusively by  $t_{AA}$ .
  7.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}$  (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD}$  (min.),  $t_{RWD} \geq t_{RWD}$  (min.) and  $t_{AWD} \geq t_{RWD}$  (min.) the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
  8. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.

READ CYCLE





READ/WRITE CYCLE

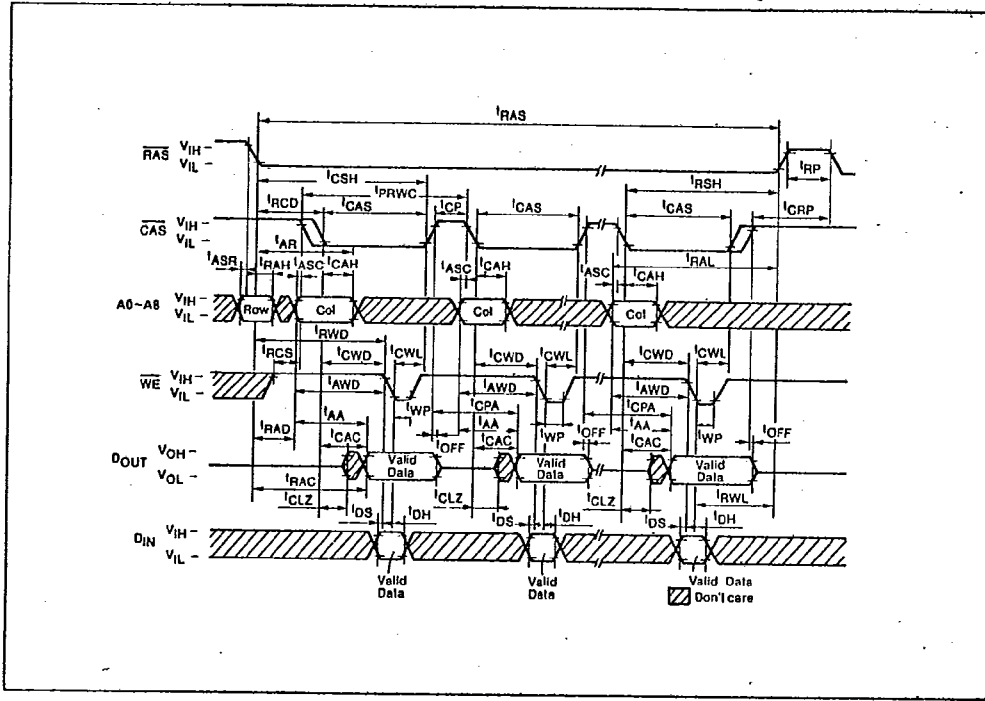




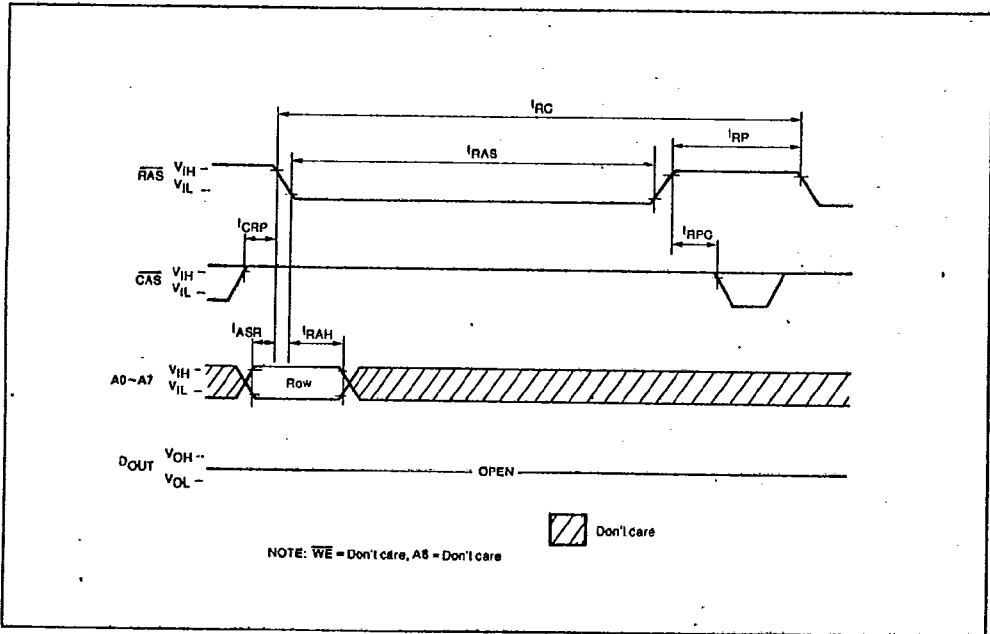




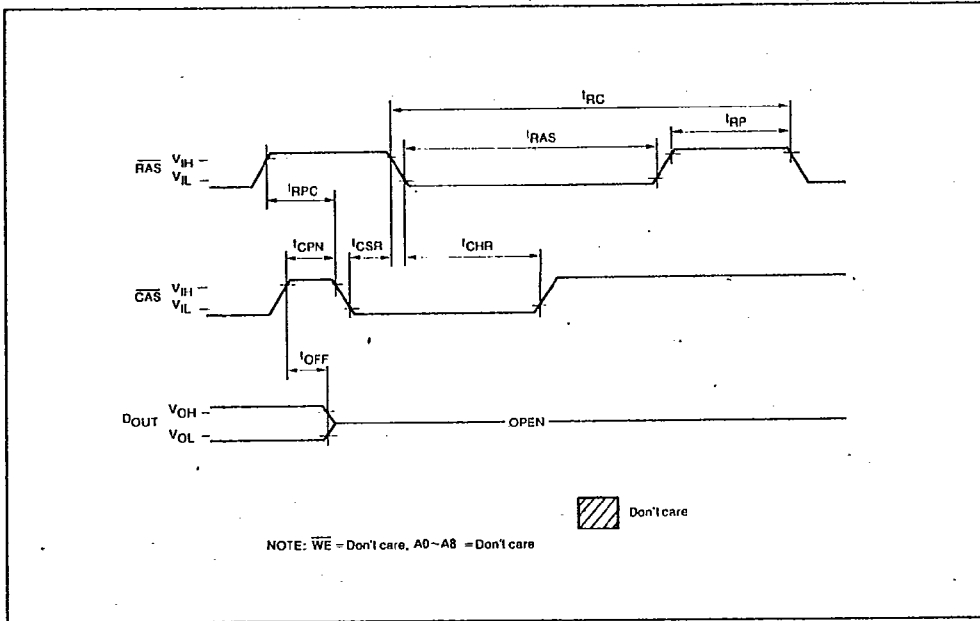
FAST PAGE MODE READ/WRITE CYCLE



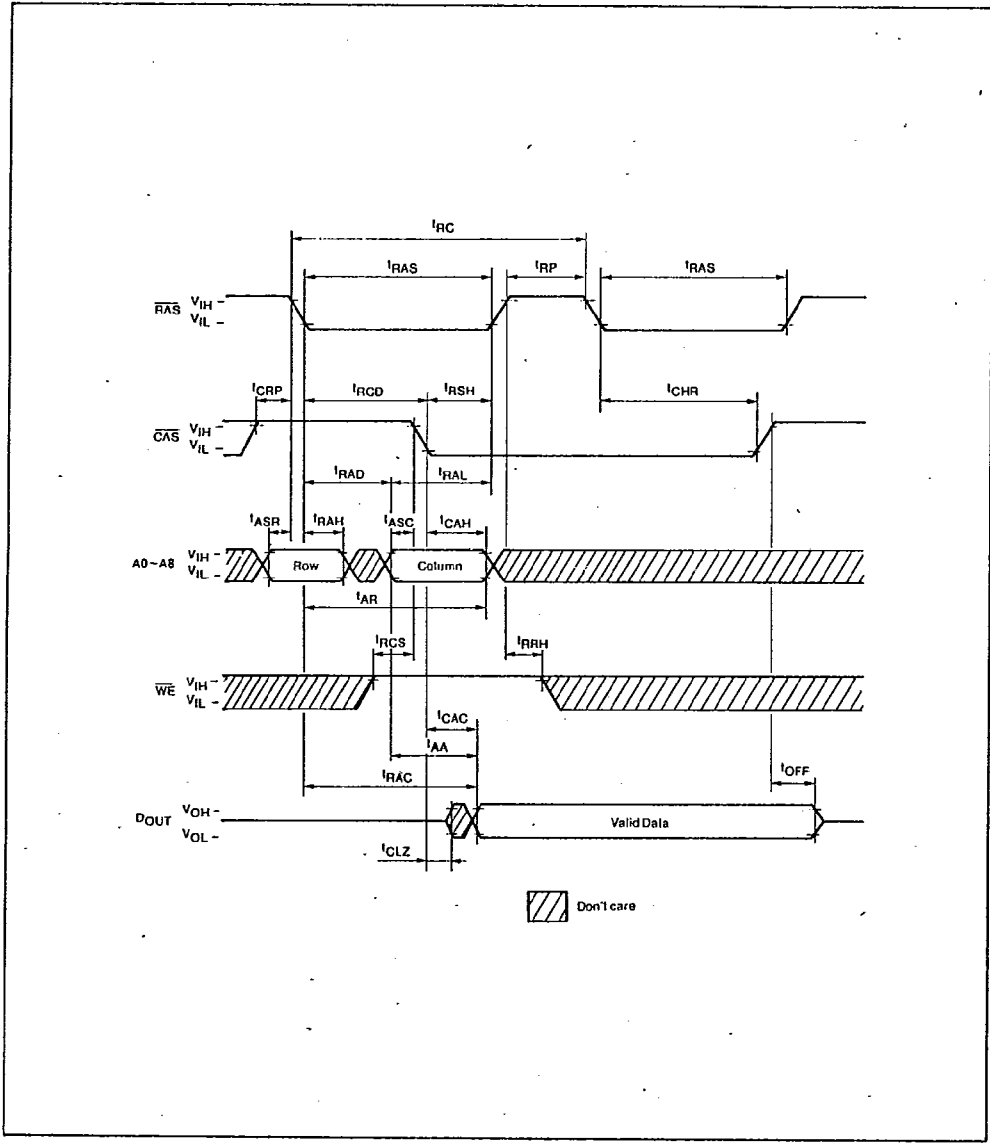
RAS ONLY REFRESH CYCLE



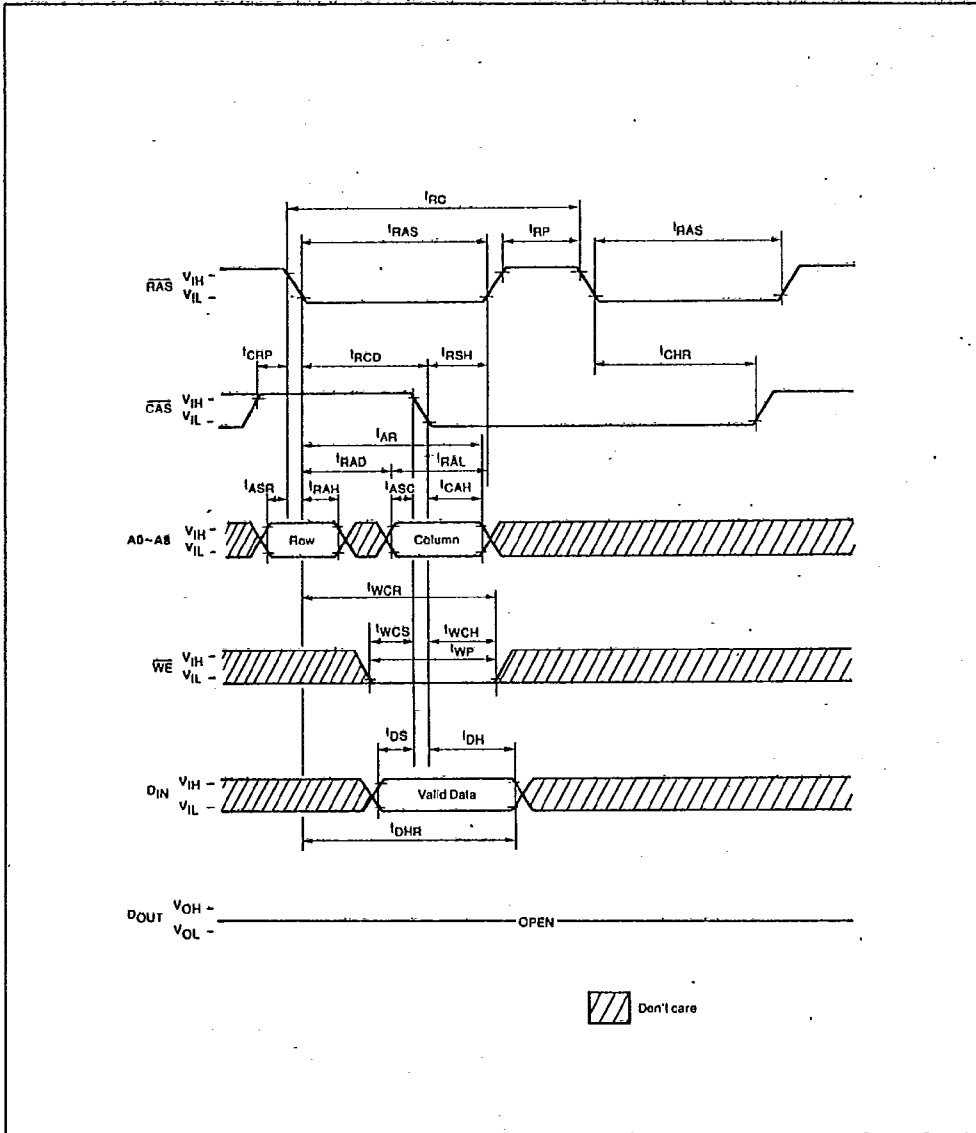
CAS BEFORE RAS REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



## FUNCTIONAL DESCRIPTION

T-46-23-15

**Simple timing Requirements:**

The MSM51C256 is a CMOS dynamic RAM optimized for high speed access time operations, low power applications. It is functionally similar to a traditional dynamic RAM. The MSM51C256 reads and writes data by multiplexing 18-bit address into 9-bit row and 9-bit column address. Because access time is primarily dependent on a valid column address rather than the precise time that  $\overline{\text{CAS}}$  edge occurs, the delay time from  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  ( $t_{\text{RCO}}$ ) has little effect on the access time. And the MSM51C256 can commit better memory system through-put during operations in an interleaved system.

**Fast-Read-While-Write Cycle:**

The MSM51C256 has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of  $\overline{\text{WE}}$  when  $\overline{\text{CAS}}$  goes low. When  $\overline{\text{WE}}$  is low during  $\overline{\text{CAS}}$  transition to low, the MSM51C256 goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when  $\overline{\text{WE}}$  goes low after  $t_{\text{CWD}}$  following  $\overline{\text{CAS}}$  transition to low, the MSM51C256 goes to delayed write mode where the output contains the data from the cell selected and the data from  $D_{\text{IN}}$  is written into the cell selected. Therefore, very fast read write cycle becomes available.

**Address Inputs:**

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM51C256. Nine row-address bits are established on the input pins ( $A_0$  through  $A_8$ ) and latched with the Row Address Strobe ( $\overline{\text{RAS}}$ ). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ( $\overline{\text{CAS}}$ ). All input addresses must be stable on or before the falling edge of  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  is internally inhibited (or "gated") by  $\overline{\text{RAS}}$  to permit triggering of  $\overline{\text{CAS}}$  as soon as the Row Address Hold Time ( $t_{\text{RAH}}$ ) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

**Write Enable:**

The read or write mode is selected with the  $\overline{\text{WE}}$  input. A logic "high" on  $\overline{\text{WE}}$  dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

**Data Input:**

Data is written into the MSM51C256 during a write or read-write cycle. The last falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$  is a strobe for the Data in ( $D_{\text{IN}}$ ) register. In a write cycle, if  $\overline{\text{WE}}$  is brought "low" (write mode) before  $\overline{\text{CAS}}$ ,  $D_{\text{IN}}$  is strobed by  $\overline{\text{CAS}}$ , and the set-up and hold times are referenced to  $\overline{\text{CAS}}$ . In a read-write cycle,  $\overline{\text{WE}}$  will be delayed until  $\overline{\text{CAS}}$  has made its negative transition. Thus  $D_{\text{IN}}$  is strobed by  $\overline{\text{WE}}$ , and set-up and hold times are referenced to  $\overline{\text{WE}}$ .

**Data Output:**

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until  $\overline{\text{CAS}}$  is brought "low". In a read cycle, or a read-write cycle, the output is valid after  $t_{\text{RAC}}$  from transition of  $\overline{\text{RAS}}$  when  $t_{\text{RCD}}$  (max) is satisfied, or after  $t_{\text{CAC}}$  from transition of  $\overline{\text{CAS}}$  when the transition occurs after  $t_{\text{RCD}}$  (max.). Data remain valid until  $\overline{\text{CAS}}$  is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

**Page Mode:**

Page-mode operation permits strobing the row-address while maintaining  $\overline{\text{RAS}}$  at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of  $\overline{\text{RAS}}$  is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

 **$\overline{\text{RAS}}$  Only Refresh:**

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ( $A_0$  to  $A_7$ ) at least every 4 milliseconds.  $\overline{\text{RAS}}$  only refresh avoids any output during refresh because the output buffer is in the high impedance state unless  $\overline{\text{CAS}}$  is brought low. Strobing each of the 256 row-addresses ( $A_0$  to  $A_7$ ) with  $\overline{\text{RAS}}$  will cause all bits in each row to be refreshed. Further  $\overline{\text{RAS}}$  only refresh results in a substantial reduction in power dissipation.

 **$\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh:**

$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refreshing available on the MSM51C256 offers an alternate refresh method. If  $\overline{\text{CAS}}$  is held on low for the specified period ( $t_{\text{FCS}}$ ) before  $\overline{\text{RAS}}$  goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh operation.

**Hidden Refresh:**

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending  $\overline{\text{CAS}}$  active time from the previous memory read cycle. In MSM51C256 hidden refresh means  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh and the internal refresh addresses from the counter are used to refresh addresses, because  $\overline{\text{CAS}}$  is always low when  $\overline{\text{RAS}}$  goes to low in this mode.