# 2304-BIT BIPOLAR RAM (256×9) 82S212 (T.S.)

## DESCRIPTION

The organization of the 82S212 allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

The 82S212 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The 82S212 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to 75°C) specify N82S212F or N and for the military temperature range (−55°C to +125°C) specify S82S212F.

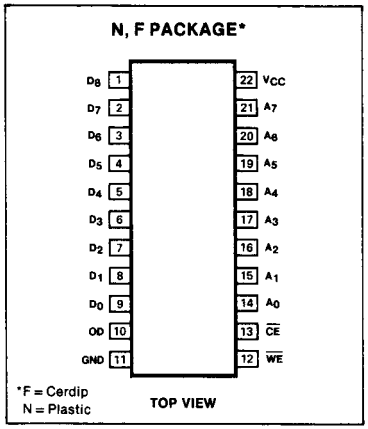
## FEATURES

- **Address access time:**
  **N82S212: 45ns max**
  **S82S212: 70ns max**
- **Power dissipation: 0.3mW/bit**
- **Tri-state outputs**
- **Schottky clamped TTL**

## APPLICATIONS

- **Cache memory**
- **Buffer storage**
- **Writable control store**

## PIN CONFIGURATION

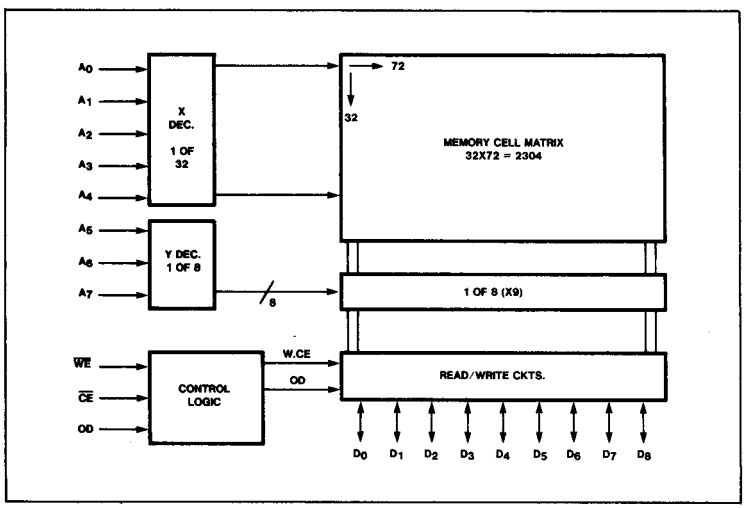



## TRUTH TABLE

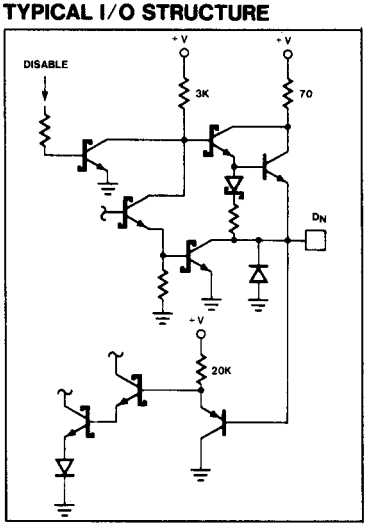
| MODE | $\overline{WE}$ | $\overline{CE}$ | OD | $D_N$ IN/OUT |
|---|---|---|---|---|
| Disable output | X | X | 1 | High Z |
| Disable R/W | X | 1 | X | High Z |
| Write | 0 | 0 | 1 | Data in |
| Read | 1 | 0 | 0 | Data out |

X = Don't care

## BLOCK DIAGRAM




## TYPICAL I/O STRUCTURE




## ABSOLUTE MAXIMUM RATINGS

| | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7 | Vdc |
| $V_{IN}$ | Input voltage | +5.5 | Vdc |
| $V_O$ | Off-state output voltage | +5.5 | Vdc |
| | Temperature range | | °C |
| $T_A$ | Operating | | |
| | Commercial | 0 to +75 | |
| | Military | −55 to +125 | |
| $T_{STG}$ | Storage | −65 to +150 | |

## DC ELECTRICAL CHARACTERISTICS[1]

N82S212: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S212: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

| PARAMETER[1] | TEST CONDITIONS | N82S212 | | | S82S212 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input voltage | | | | | | | | V |
| $V_{IL}$ Low | $V_{CC}$ = Min | | | .85 | | | .80 | |
| $V_{IH}$ High | $V_{CC}$ = Max | 2.0 | | | 2.2 | | | |
| $V_{IC}$ Clamp[2] | $V_{CC}$ = Min, $I_{IN}$ = −12mA | | | −1.5 | | | −1.5 | |
| Output voltage | | | | | | | | V |
| $V_{OL}$ Low[3] | $V_{CC}$ = Min, $I_{OL}$ = 8.0mA | | | 0.5 | | | 0.5 | |
| Input current | | | | | | | | μA |
| $I_{IL}$ Low | $V_{IN}$ = 0.45V | | | −100 | | | −150 | |
| $I_{IH}$ High | $V_{IN}$ = 5.5V | | | 25 | | | 40 | |
| Output current | | | | | | | | |
| $I_{O(OFF)}$ Hi-Z state | $\overline{CE}$ = High or OD = High, $V_{OUT}$ = 5.5V | | | 40 | | | 60 | μA |
| | $\overline{CE}$ = High or OD = High, $V_{OUT}$ = 0.5V | | | −100 | | | −100 | |
| $I_{OS}$ Short circuit[4, 5] | $\overline{CE}$ = OD = Low, $V_{OUT}$ = 0V | −20 | | −70 | −15 | | −80 | mA |
| $I_{CC}$ $V_{CC}$ supply current[5] | $V_{CC}$ = Max | | 135 | 185 | | | 200 | mA |
| Capacitance | $V_{CC}$ = 5.0V | | | | | | | pF |
| $C_{IN}$ Input | $V_{IN}$ = 2.0V | | 5 | | | 5 | | |
| $C_{OUT}$ Output | $V_{OUT}$ = 2.0V | | 8 | | | 8 | | |

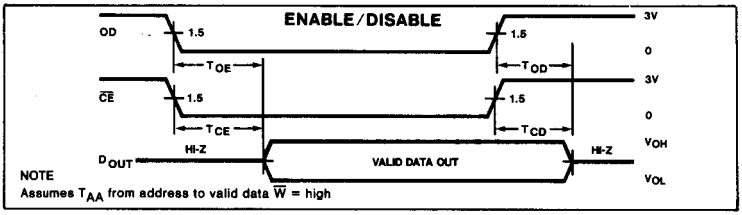
## AC ELECTRICAL CHARACTERISTICS[1]

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S212: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S212: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

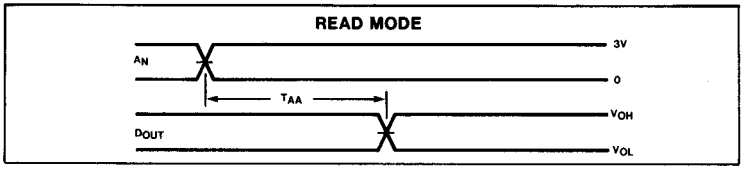
| PARAMETER | TO | FROM | N82S212 | | | S82S212 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[3] | Max | Min | Typ[3] | Max | |
| Access time | | | | | | | | | ns |
| $T_{AA}$ Address | Output | Address | | | 45 | | | 70 | |
| Enable time | | | | | | | | | ns |
| $T_{OE}$ Output | Output | OD | 5 | | 25 | | | 50 | |
| $T_{CE}$ Output | Output | Chip enable | | | 25 | | | 50 | |
| Disable time | | | | | | | | | ns |
| $T_{OD}$ Output | Output | OD | | | 25 | | | 50 | |
| $T_{CD}$ Output | Output | Chip enable | | | 25 | | | 50 | |
| Pulse width | | | | | | | | | ns |
| $T_{WP}$ Write | | | 25 | | | 45 | | | |
| $T_{WSC}$ Setup time | Write | Chip enable | 5 | | | 10 | | | |
| $T_{WHD}$ Hold time | Chip enable | Write | 5 | | | 10 | | | |
| $T_{WSD}$ Setup time | Write | Data | 25 | | | 45 | | | |
| $T_{WHD}$ Hold time | Data | Write | 5 | | | 5 | | | |
| $T_{WSA}$ Setup time | Write | Address | 5 | | | 10 | | | |
| $T_{WHA}$ Hold time | Address | Write | 5 | | | 15 | | | |
| $T_{SO}$ Setup time (from disabled state) | Chip enable | OD | 5 | | | 5 | | | |
| $T_{HO}$ Hold time | OD | Chip enable | 5 | | | 5 | | | |

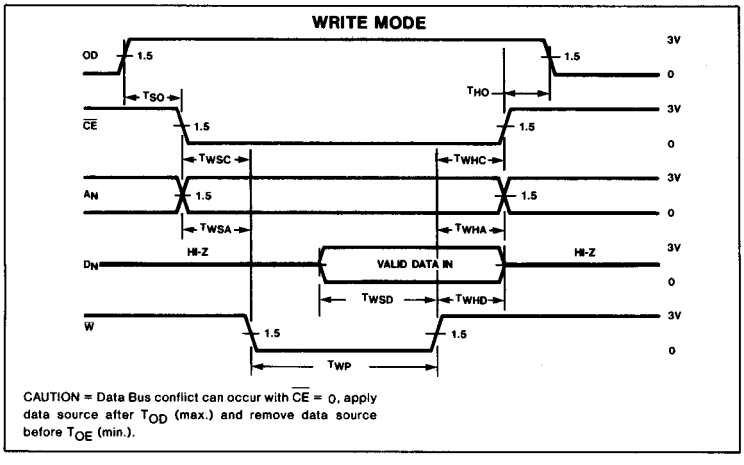
NOTES
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Measured on one pin at a time.
5. Duration of $I_{OS}$ test should not exceed one second.

## TIMING DIAGRAMS



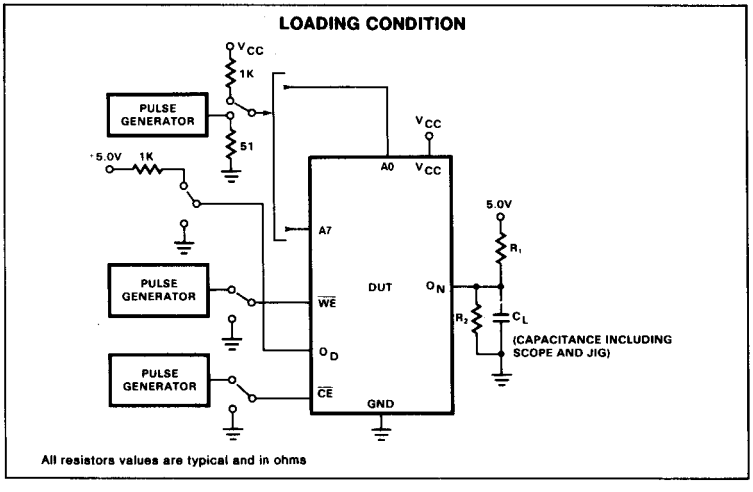

NOTE
Assumes $T_{AA}$ from address to valid data $\overline{W}$ = high




CAUTION = Data Bus conflict can occur with $\overline{CE}$ = 0, apply data source after $T_{OD}$ (max.) and remove data source before $T_{OE}$ (min.).

## TEST LOAD CIRCUIT




All resistors values are typical and in ohms

## VOLTAGE WAVEFORM