NEC
ELECTRON DEVICE

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC661

VIDEO SIGNAL PROCESSING 6-BIT A/D CONVERTER WITH BUILT-IN ANALOG MULTIPLEXER AND CLAMPER

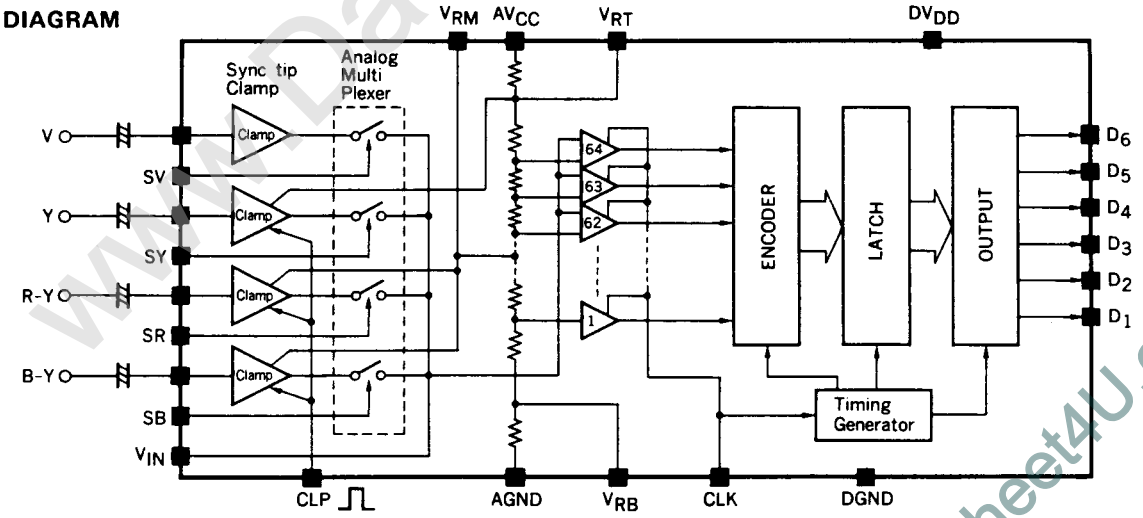
The μPC661 is a 6-bit A/D converter for video systems. The high-speed/high-precision bipolar processing technology embodied in this IC realizes 20 Msps and ±0.5 LSB (MAX.). The low power consumption design provide wide applicability of this IC to digital systems in various fields, such as digital TV systems, PIP (Picture-in-picture) system, or high speed facsimile system.

This IC has a built-in analog multiplexer for four inputs together with a clamper for each input for selective A/D conversion of video signal. In addition, a reference voltage generator is also built in for simpler circuit configurations.

CHARACTERISTICS

- Resolution: 6 bits
- Conversion Rate: 20 Msps
- Non-Linearity Error: ±0.5 LSB
- +5 V Single Power Supply
- Input voltage Range: 1.0 V_{p-p}
- Built-in Clamp circuit.
- Built-in reference voltage generator: V_{RB} = 2.5 V, V_{RM} = 3.0 V, V_{RT} = 3.5 V
- Built-in Analog Multiplexer. (For 4 inputs.)
- Power Consumption: 200 mW (TYP.)
- Package: 24-pin SHD, 24-pin SOP (375 mil)

BLOCK DIAGRAM

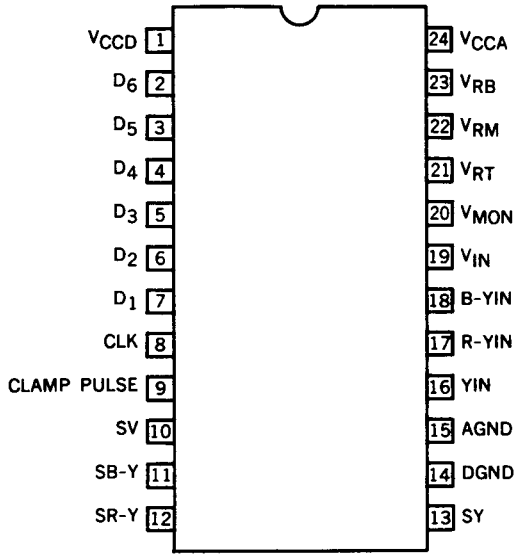


ORDER INFORMATION

Order name	Package
μPC661CA	24-pin SHD (300 mil)
μPC661G	24-pin SOP (375 mil)

The specifications of this product are subject to change without prior notice.

PIN CONNECTION DIAGRAM (Top View)



Pin number	Symbol	Pin name	Pin number	Symbol	Pin name
1	V_{CCD}	Digital power supply	13	SY	Luminance signal selector (Y)
2	D_6	Digital output (LSB)	14	DGND	GND
3	D_5	Digital output	15	AGND	GND
4	D_4	Digital output	16	YIN	Luminance signal input (Y)
5	D_3	Digital output	17	R-YIN	Color difference signal input (R-Y)
6	D_2	Digital output	18	B-YIN	Color difference signal input (B-Y)
7	D_1	Digital output (MSB)	19	V_{IN}	Video signal input
8	CLK	Clock input	20	V_{MON}	Analog Monitor
9	CLAMP PULSE	Clamp pulse input	21	V_{RT}	Reference voltage (high-level voltage)
10	SV	Video signal selector	22	V_{RM}	Reference voltage (intermediate-level voltage)
11	SB-Y	Color difference signal selector (B-Y)	23	V_{RB}	Reference voltage (lower voltage)
12	SR-Y	Color difference signal selector (R-Y)	24	V_{CCA}	Analog power supply

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	AV_{CC}, DV_{CC}	−0.3 to +5.7	V
Input Voltage on Each Pin	V_I	−0.3 to V_{CC}+0.3	V
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

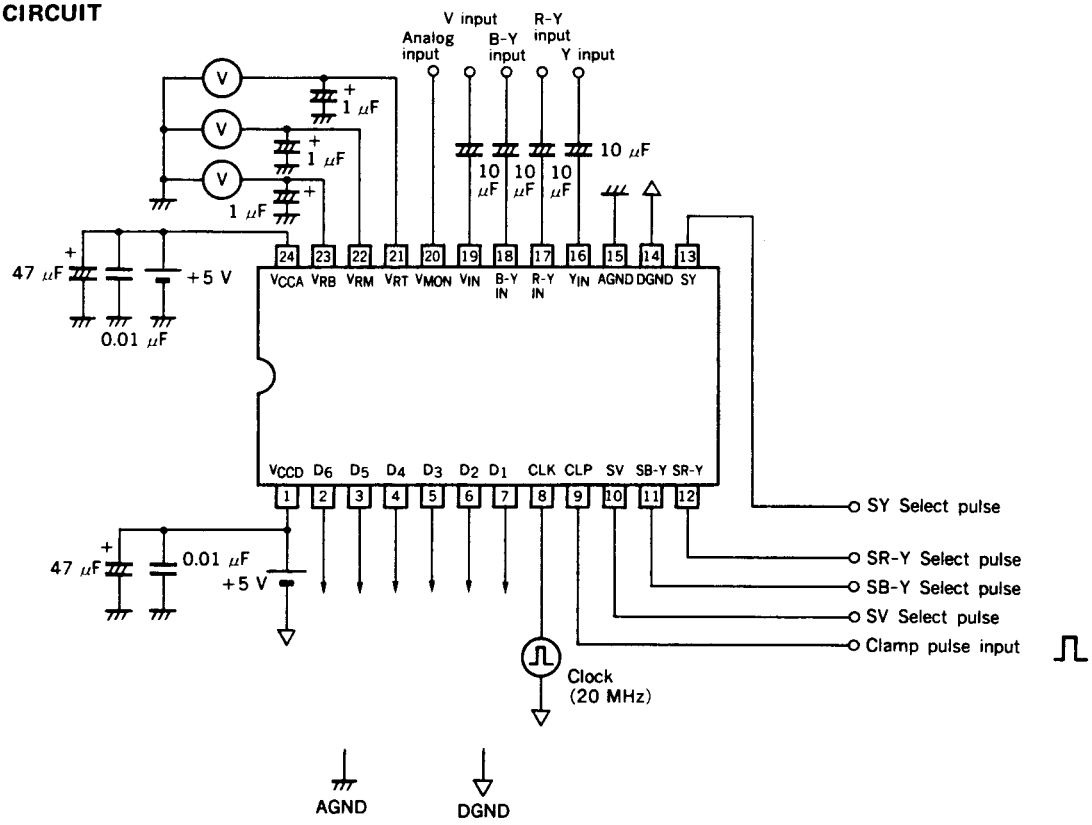
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply voltage	AV_{CC}, DV_{CC}	4.5	5.0	5.5	V	AGND = DGND = 0 V
Analog input voltage	V_{INA}	V_{RB}−0.4		V_{RT}+0.4	V	
Sampling clock	f_{samp}	1		20	MHz	
Sampling clock low-level pulse width	t_{PWL}	20			ns	
Sampling clock high-level pulse width	t_{PWH}	20			ns	
Select pulse high-level width	t_{se}	150			ns	
Clamp pulse high-level pulse width	t_{PWCH}	1			μs	
Clamp pulse low-level width	t_{PWCL}			100	μs	Clamp capacitance C_{CL} = 10 μF
Clamp capacitance	C_{CL}		10		μF	
Digital input high-level voltage	V_{INDH}	2.7			V	
Digital input low-level voltage	V_{INDL}			0.4	V	

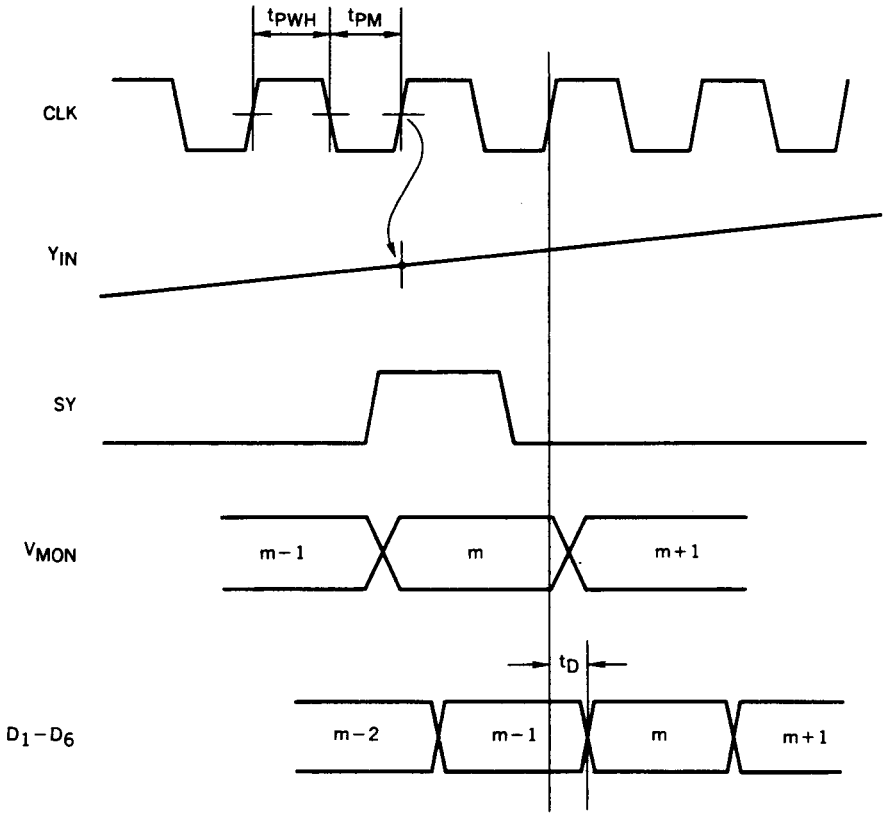
ELECTRICAL RATINGS (T_a = −20 to +75 °C, AV_{CC} = DV_{CC} = 5.0±0.5 V)

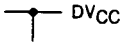
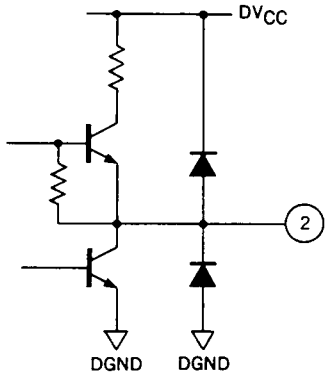
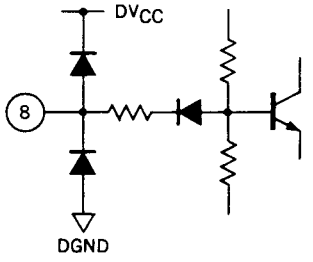
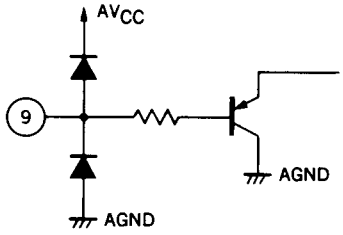
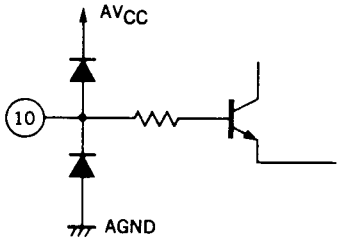
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power consumption	I_{CC}	32	46	60	mA	AV_{CC} = DV_{CC} = 5.0 V, T_a = 25 °C
Nonlinearity error	NL			±0.25	LSB	V_{CC} = 5.0 V, T_a = 0 to 60 °C, V_{INA} = 1 V_{p-p} f_{samp} = 20 MHz
Differential linearity error	DNL			±0.25	LSB	V_{CC} = 5.0 V, T_a = 0 to 60 °C, V_{INA} = 1 V_{p-p} f_{samp} = 20 MHz
Data output delay time	t_D		12		ns	Delay time from the rise of the clock signal, D_1 to D_6
Digital low-level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
Digital high-level output voltage	V_{OH}	2.7			V	I_{OH} = −400 μA
Digital low-level input current	I_{INDL}			−300	μA	I_{INDL} = 0.8 V
Digital high-level input current	I_{INDH}			20	μA	V_{INDH} = 2.0 V
Reference voltage (low-voltage side)	V_{RB}	2.2	2.5	2.8	V	V_{CCA} = 5.0 V
Reference voltage (intermediate-voltage side)	V_{RM}	2.7	3.0	3.3	V	V_{CCA} = 5.0 V
Reference voltage (high-voltage side)	V_{RT}	3.2	3.5	3.8	V	V_{CCA} = 5.0 V
Analog input capacitance	C_{IN}			7	pF	V_{IN} = V_{RB}
Clock input capacitance	C_{CLK}		2	5	pF	

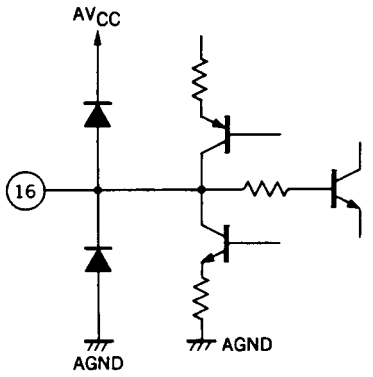
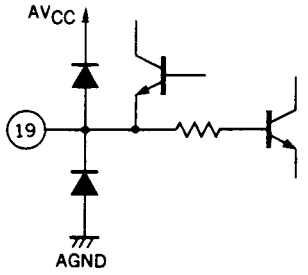
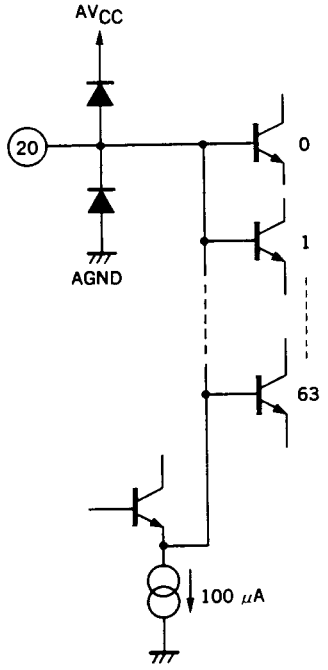
MEASUREMENT CIRCUIT

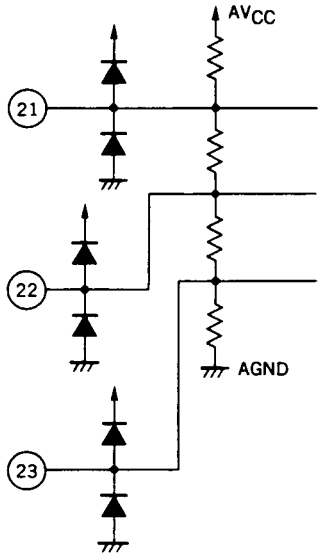


TIMING CHART



PIN NUMBER	EQUIVALENT CIRCUIT DIAGRAM	DESCRIPTION OF FUNCTIONS
1		Digital system power supply
2, 3, 4, 5, 6, 7		2: Digital data output (MSB) 3: Digital data output (5th) 4: Digital data output (4th) 5: Digital data output (3rd) 6: Digital data output (2nd) 7: Digital data output (1st) Digital data output terminals. The data is output one digital output delay period (t_D) after the rise of the clock. (Refer to the Timing Chart). Output at the TTL level.
8		Clock signal input terminal. Analog input is fetched and digital data is output at the rise of the signal input to this terminal.
9		Clamp pulse input terminal for color difference signal (R-Y, B-Y) and luminance signal (Y). The signal is clamped when this terminal is high.
10, 11, 12, 13		10: Analog multiplexer switching signal input (SV). This terminal selects the signal from the V_{IN} terminal (Pin 19) while this terminal is high. 11: Analog multiplexer switching signal input (SB-Y). This terminal selects the signal from the B-YIN terminal (Pin 18) while this terminal is high. 12: Analog multiplexer switching signal input (SR-Y). This terminal selects the signal from the R-YIN terminal (Pin 17) while this terminal is high. 13: Analog multiplexer switching signal input (SY) This terminal selects the signal from the YIN terminal (Pin 16) while this terminal is high.

PIN NUMBER	EQUIVALENT CIRCUIT DIAGRAM	DESCRIPTION OF FUNCTIONS
14		Digital system grounding terminal.
15		Analog system grounding terminal.
16, 17, 18		16: Luminance signal (Y) input terminal and clamper. Input level: 1 V_{p-p}. Clamping level: V_{RT}. 17: R-Y input terminal and clamper. Input level: 1 V_{p-p}. Clamping level: V_{RM}. 18: B-Y input terminal and clamper. Input level: 1 V_{p-p}. Clamping level: V_{RM}.
19		Composite video signal input terminal and clamper. Input level: 1 V_{p-p}. The clamp is a sink chip (minimum value) clamp.
20		Analog multiplexer output monitor terminal. This terminal monitors the input signal selected by pins 10 to 13. This terminal is normally open.

PIN NUMBER	EQUIVALENT CIRCUIT DIAGRAM	DESCRIPTION OF FUNCTIONS
21 22 23		21: Reference voltage output terminal (high-voltage side). V_{RT}. 22: Reference voltage output terminal (Intermediate-voltage side). V_{RM}. 23: Reference voltage output terminal (low-voltage side). V_{RB}.
24		24: Analog system power supply.

SUPPLEMENT

Clamp Operation

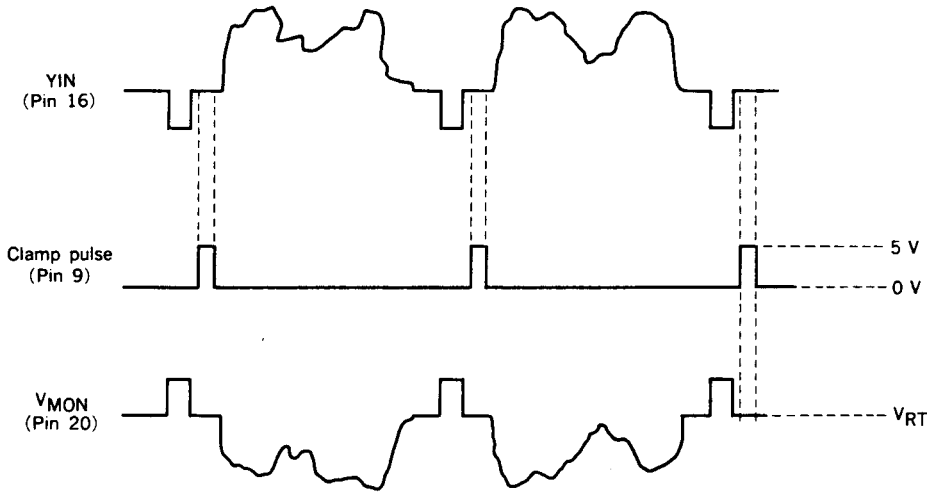
This IC has a built-in clamper that clamps using the coupling capacitance of the respective analog signal input terminals 16 to 19.

1) Clamping of the video signal input, V_{IN} (Pin 19)

The clamping here is based on the minimum value clamping system, which is mainly used for clamping the video sink chip. The voltage during clamping is generated by the internal regulator. Note that this clamper operates independently from the clamp pulse on the pin 9.

2) Clamping of the luminance signal input, YIN (Pin 16)

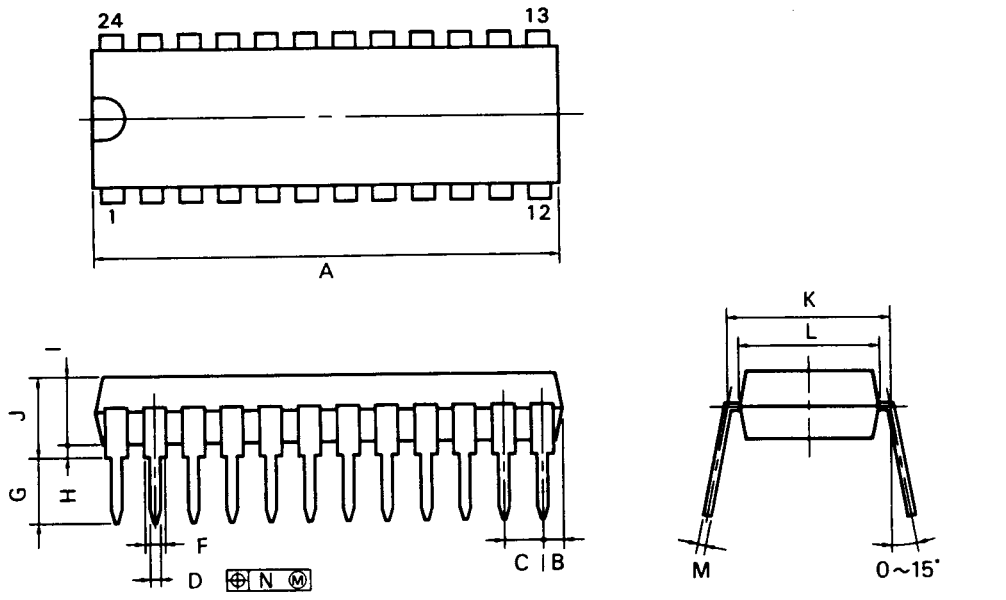
Clamping here is executed when the clamp pulse on pin 9 is high. When the clamp pulse is high, the signal voltage supplied from the pin 16 is clamped to V_{RT} (reference high voltage) at the V_{INA} terminal (Pin 20). The timing and the level of the clamping by the pedestal are as follows:



3) Clamping of the color difference signals: R-YIN (Pin 17) and B-YIN (Pin 18)

This clamping is executed while the clamp pulse at pin 9 is high. When the clamp pulse is high, the signal voltage supplied from the pin 17 or 18 is clamped to V_{RM} (intermediate reference voltage) at the V_{IN} (Pin 20) terminal.

24-PIN PLASTIC SHRINK DIP (300 mil) (Unit : mm)



S24C-70-300B

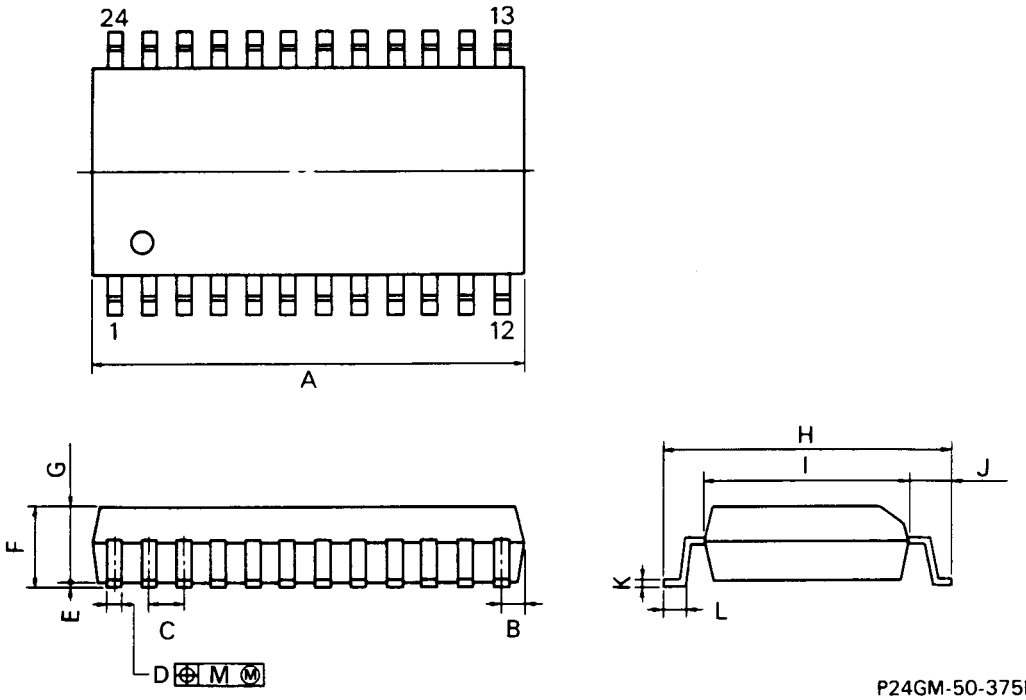
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24-PIN PLASTIC SOP (375 mil) (Unit : mm)



P24GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

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