PWM Optimized Power MOSFETs for Low-Voltage DC/DC Conversion

Designers of low-voltage dc-to-dc converters have two main concerns: reducing size and reducing losses. As a way of reducing size, designers are increasing switching frequencies. But the result has been reduced converter efficiency. To minimize losses, MOSFET manufacturers have generally focused on lowering on-resistance. But the results have not been optimal for dc-to-dc conversion designs, since gate charge and switching speed issues have been largely ignored. The dominant losses associated with MOSFETs were once conduction losses, but this is no longer the case.

Vishay Siliconix's new family of PWM optimized MOSFETs has been designed to give the highest efficiency available for a given on-resistance in switching applications such as dc-to-dc conversion. These new devices provide a very low gate charge per unit of on-resistance, in addition to fast switching times. The result is reduced gate drive and crossover losses, allowing designers of dc-to-dc converters to simultaneously reduce the design footprint and increase efficiency.

MOSFET Losses

A simplistic model of power loss in a MOSFET used in a dc-to-dc converter (Figure 1) can be calculated if we know the RMS, the current through the MOSFET, the duty cycle, the gate voltage, and the $r_{DS(on)}$ of the MOSFET. This model can then be used to compare the efficiency of designs using Vishay Siliconix's new PWM optimized MOSFETs versus conventional and low-threshold power MOSFETs.

The equation that defines the losses associated only with on-resistance and the gate drive is:

$$P = I^2RMS \times r_{DS(on)}\left[V_{GS}\right]\left[T_J\right] \times D + Q_g\left[V_{GS}\right] \times V_{GS} \times f \quad \text{(Watts)} \quad \text{Eq1}$$

[ ] The value of the parameter before the parenthesis is dependent on the parameter within the parenthesis.

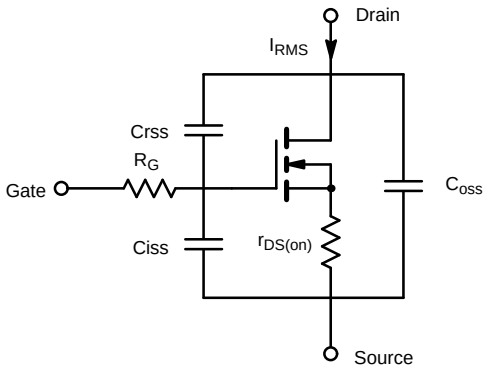

FIGURE 1. Generic MOSFET model with body diode omitted.

where:

I^2RMS	The RMS current in the MOSFET (A)
$r_{DS(on)}$	On-resistance of the device for a given drive voltage and junction temperature.
V_{GS}	The peak driver gate voltage for the MOSFET (V)
$[T_J]$	Junction temperature of the MOSFET
D	Duty factor of the MOSFET (Ratio of on time to off time)
Q_g	Total gate charge for the MOSFET at a given gate voltage (C)
f	Frequency of MOSFET switching (Hz)

Using Equation 1 we can obtain a plot of power loss (gate loss + $r_{DS(on)}$ loss) as a function of gate voltage at varying switching frequencies (Figure 2). [1]

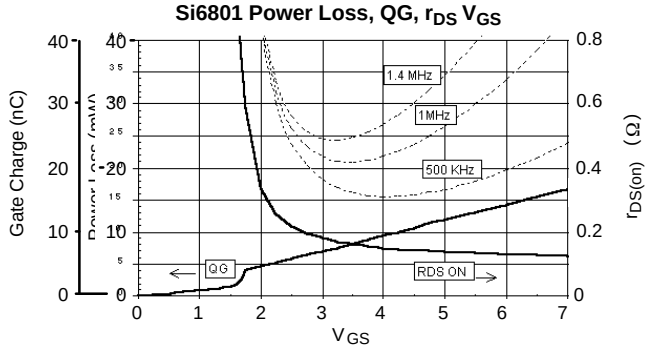

FIGURE 2. Power loss for PWM optimized Si6801 p-channel MOSFET as a function of V_{GS} and switching frequency.

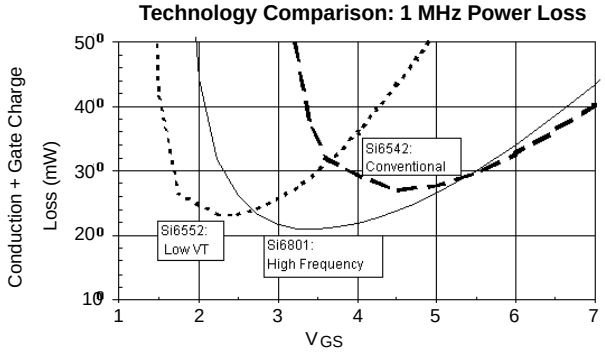

FIGURE 3. Gate losses and on-resistance losses for PWM optimized power MOSFET (Si6801DQ) versus conventional (Si6542DQ) and low-threshold (Si6552DQ) power MOSFETs.

Figure 2 shows the respective contribution of on-resistance and gate charge to overall losses for the p-channel Si6801DQ at three different switching frequencies. At low gate-source voltages, the $r_{DS(on)}$ of the MOSFET is high and therefore on-resistance losses dominate. At higher gate-source voltages, on-resistance becomes almost a constant and the gate charge losses controlled by Q_g dominate. Gate losses increase with the switching frequency, causing a narrowing in the optimum gate voltage. Therefore, the optimum drive voltage will be at a level which is just enough to take the $r_{DS(on)}$ into its constant region, but no further. Typically, this drive voltage is between 3 and 5 V, which is what most controller ICs provide.

Figure 3 compares the power losses, at a switching frequency of 1 MHz, of Vishay Siliconix's PWM optimized Si6801DQ, a conventional power MOSFET (Si6542DQ), and a low-threshold power MOSFET (Si6552DQ).

Power losses for the PWM optimized MOSFET at gate drives between 2.5 and 5.5 V are significantly lower than both conventional and low-threshold MOSFETs, making the optimized device the obvious choice for all switching applications.[7.]

The PWM Optimized MOSFET in a Real Application

The PWM optimized power MOSFET is best viewed in the context of a real application. In the example used here, the Si6801DQ is paired with the Si9160BQ switching regulator IC to create a synchronous boost converter for cellular telephones with the following specifications:

Input voltage: 2.7 V to 5 V (single-cell lithium ion battery is 2.7 V to 4.2 V)
Output voltage: 5 V
Output current: 1 A maximum
Gate drive voltage: 4.5 V
Control scheme: Constant frequency voltage mode control
Switching frequency: Varied by RC value from 300 kHz to 1.8 MHz

All results shown are with V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 600 mA, f = 1 MHz unless otherwise stated.

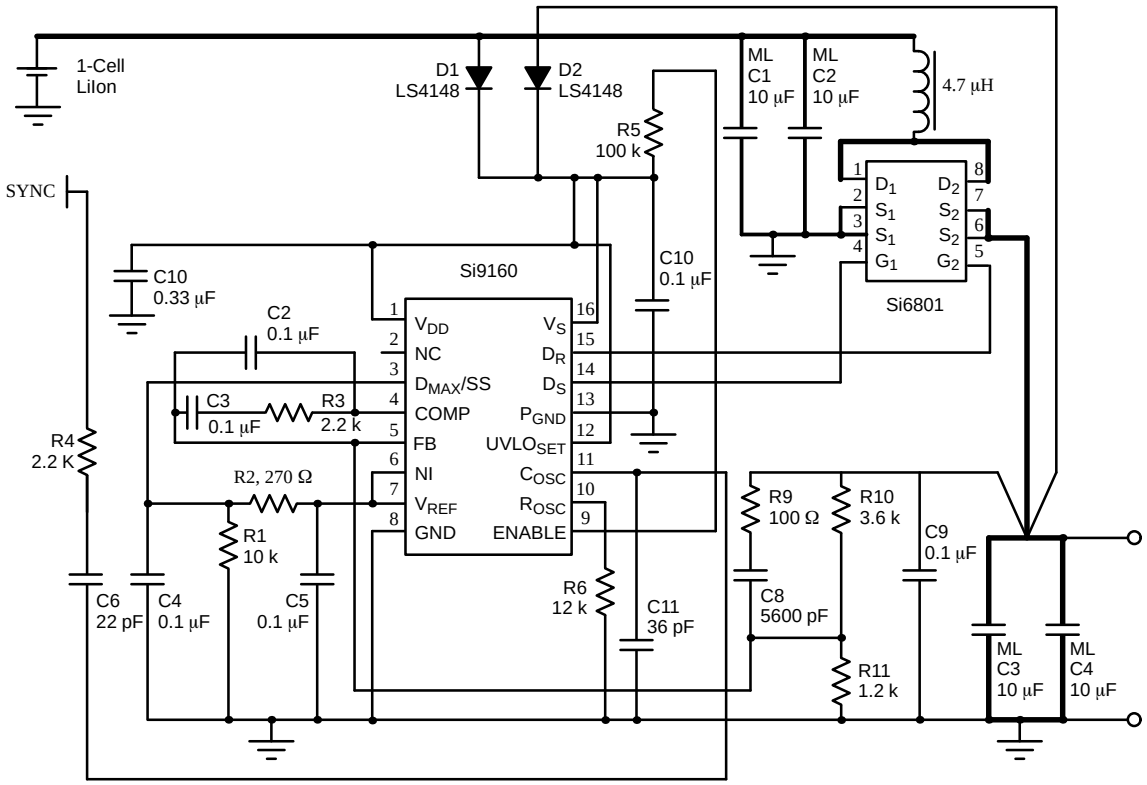

FIGURE 4. Si9160 Boost converter test circuit used to compare MOSFET technologies.

7. Neither Figure 2 nor Figure 3 is intended for exacting power loss calculations. These figures should only be used as a comparative measure for various MOSFET technologies.

The following complementary n- and p-channel MOSFETs, all LITTLE FOOT TSSOP-8 devices, represent the three technologies under test:

PWM optimized MOSFET Si6801DQ
Conventional MOSFET Si6542DQ
Low-threshold MOSFET Si6552DQ

Figure 4 shows test circuit used.

PWM Optimized MOSFET Performance

Reducing gate charge is one way in which PWM optimized MOSFETs cut power losses. In a real application, another component of power loss is crossover losses. These are also minimized by the PWM optimized power MOSFET design, and are discussed in detail in Appendix A.

Figure 5 shows oscillograms of the boost converter switching waveform using the three different types of power MOSFETs.

The switching speeds are 4 ns for the Si6801DQ PWM optimized MOSFET and 11 ns for the conventional MOSFET. The Si6801DQ provides a nearly threefold improvement and thus lower losses. In addition to the increase in basic switching speed, notice that the PWM optimized MOSFET does not exhibit a large characteristic step in the voltage waveform. This step is due to the feedback capacitance from drain to gate of the MOSFET or “Miller” capacitance (C_{rss} in Figure 1) being charged when the drain voltage is lower than the gate voltage during a switching transition from an OFF state to an ON state. Effectively the gate voltage is “stalled” while the Miller capacitance is charged, and this is reflected in the voltage waveform from drain to source. This is obviously an unwanted characteristic and has largely been eliminated with PWM optimized MOSFET technology.

A final component that affects the switching speed of a MOSFET is the effective gate resistance (R_G in Figure 1). The effective gate resistance defines how fast the MOSFET capacitance can be charged. It is therefore one of the dominant factors in determining how fast a MOSFET will switch. Vishay Siliconix’s PWM optimized MOSFETs provide a minimum effective gate resistance.

DRAIN-SOURCE VOLTAGE OF N-CHANNEL MOSFET IN A SI9160 BOOST CONVERTER

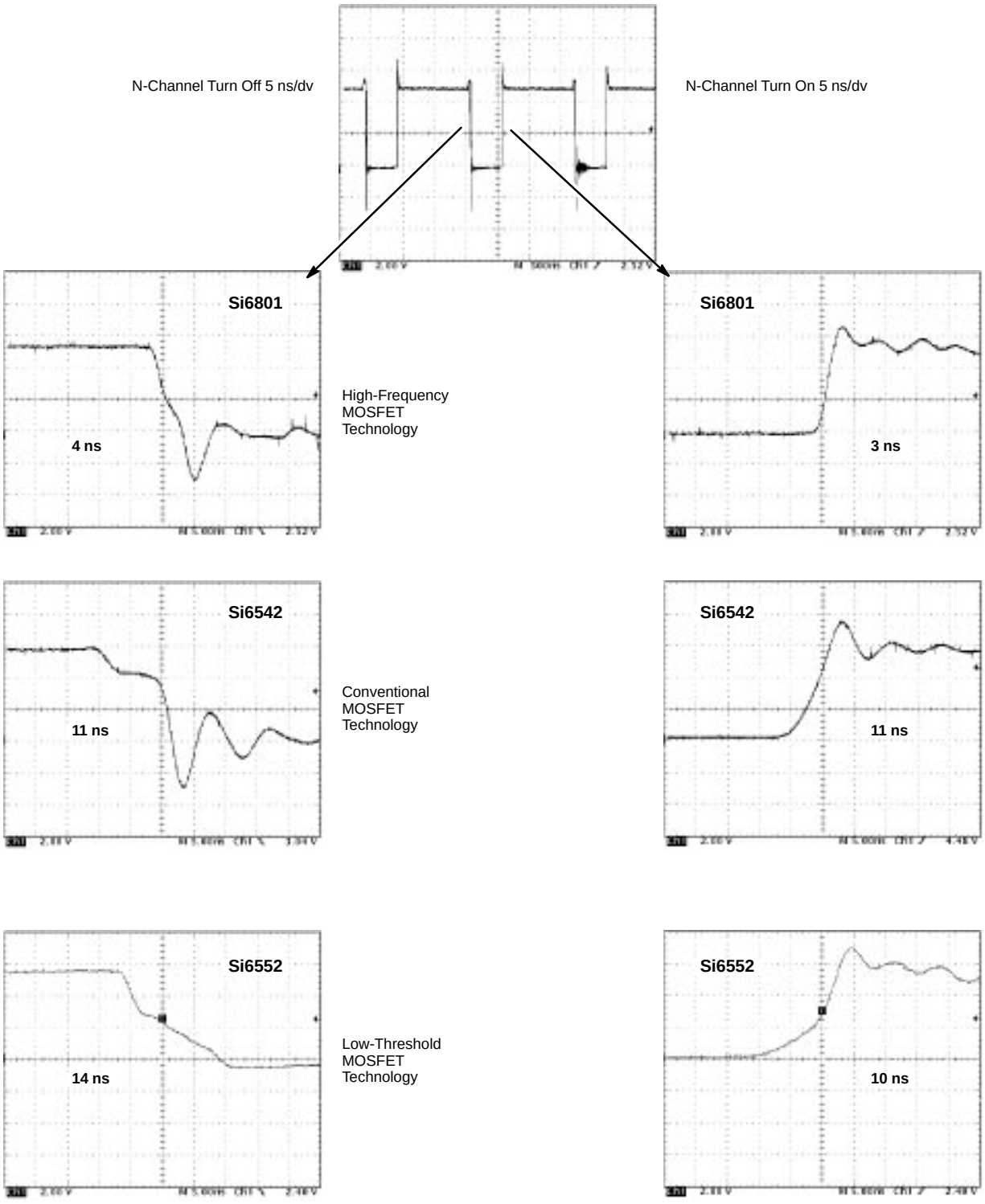

FIGURE 5. Switching speed comparison between high-frequency, conventional, and low-threshold power MOSFETs.

A power MOSFET is made up of many single MOSFET cells arranged in a parallel combination. In an ideal MOSFET all the cells will turn on together when activated by a gate signal, and a minimum switching time transition will be obtained. This does not happen in a conventional MOSFET layout because the gate signal has to propagate across the silicon in a turn-on “wave,” where the cells nearest the gate bus turn on first with the outer cells following. The PWM optimized MOSFET has symmetrical gate bussing, and its bonding and layout structures minimize the turn-on “wave,” thus increasing the switching speed of the device.

Efficiency

How much extra efficiency does the PWM optimized MOSFET provide? A comparison of the efficiency of the synchronous boost converter (Figure 4) using three different MOSFET technologies shows that an improvement on the order of 5% can be made if an optimized device is used.

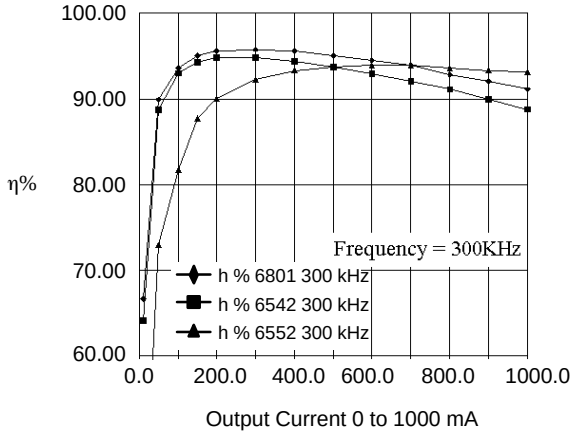

FIGURE 6. Efficiency comparison between high-frequency, conventional, and low-threshold MOSFETs at a switching frequency of 300 kHz.

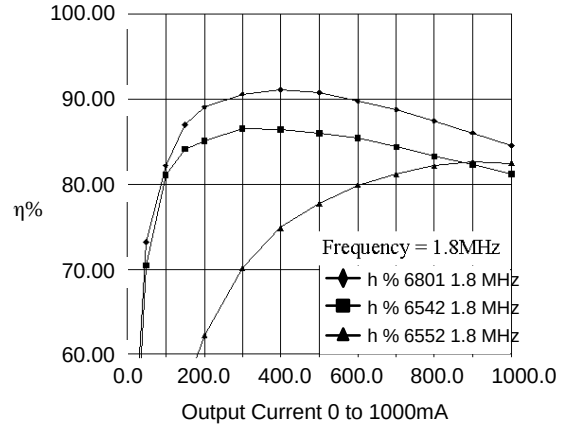

FIGURE 8. Efficiency comparison between high-frequency, conventional, and low-threshold MOSFETs at a switching frequency of 1.8 MHz.

Figures 6, 7, and 8 show efficiency at switching frequencies ranging from 300 kHz to 1.8 MHz, while Figure 9 summarizes the efficiencies of the three technologies against switching frequency at an output current of 400 mA. For all the results shown, the input voltage for the synchronous boost converter was 3.6 V, with an output voltage of 5 V.

The PWM optimized MOSFET surpasses all other technologies while maintaining the highest efficiencies over the broadest load ranges at all switching frequencies. The conventional MOSFET technology provides the same breadth of efficiency but at a reduced value. The low- threshold technology is clearly unsuited to switching at higher switching frequencies with a gate voltage of 4.5 V.

As summarized in Table 1, at all switching frequencies the PWM optimized MOSFET technology gives superior performance, both in highest peak efficiencies and over the broadest load range, making it the ideal choice for most low-voltage dc-to-dc designs.

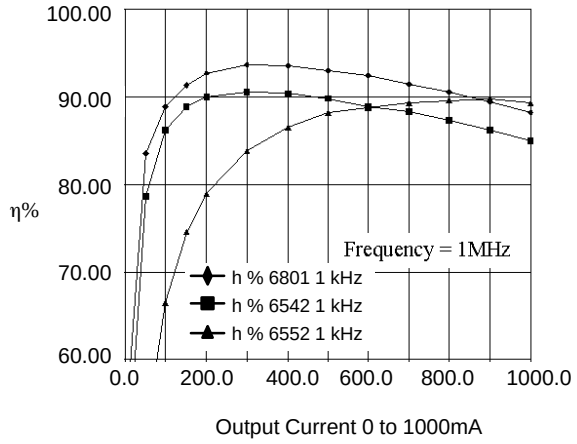

FIGURE 7. Efficiency comparison between high-frequency, conventional and low-threshold MOSFETs at a switching frequency of 300 kHz

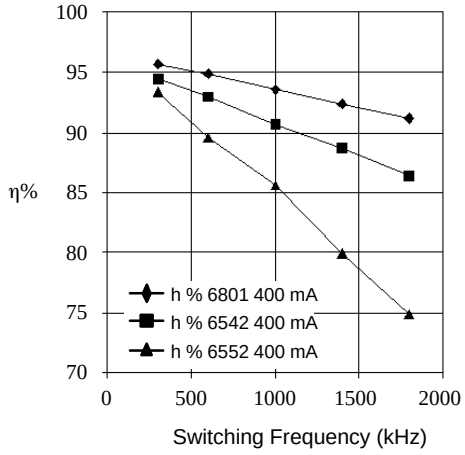

FIGURE 9. Efficiency vs. switching frequency comparing the PWM optimized MOSFET technology with conventional and low-threshold technologies

TABLE 1. COMPARISON OF MOSFET PERFORMANCE

Type of MOSFET	Typical On-Resistance at 4.5 V (mΩ)	Specific Gate Charge	Normalized Gate Charge per 100 mΩ (nc)
PWM Optimized	120	1.7	1.4
Conventional	100	4.0	4.0
Low- Threshold	73	16.0	22.0

Figure of Merit for the PWM Optimized MOSFET Technology

Normalized gate charge serves as a quick figure of merit for comparing the high-frequency, conventional, and low-threshold MOSFETs. This was calculated by normalizing the on-resistance and gate charge of the n-channel MOSFET to 100 mΩ:

Similar performance advantages will be seen for the p-channel process as well.

Application Areas

Ideal applications for Vishay Siliconix's PWM optimized MOSFETs include mobile communication equipment and other hand-held battery-operated systems, where dc-to-dc converters are becoming essential, and any other application where small size and high efficiency are design criteria. A good example is the demonstration board used as an example in this application note. The Si9160BQ and Si6801DQ chip set is targeted for the cellular phone market where single-cell lithium ion batteries are becoming more popular and high-efficiency boost converters are required. The buck converter in notebook computers is another key application for Vishay Siliconix's PWM optimized MOSFETs. Most buck converter controller ICs today support synchronous operation and require all n-channel MOSFETs. A typical synchronous buck converter is shown in Figure 10.

In addition to non-isolated buck and boost topologies, Vishay Siliconix's PWM optimized MOSFETs are also very useful in the application of synchronous rectification for isolated converters (Figure 11). The replacement of Schottky diodes with MOSFETs on the output of isolated topologies is becoming more popular and even a necessity as output voltages drop below the 3-V level. This makes Schottky diodes impractical for efficiency reasons. The biggest disadvantage to MOSFETs in isolated synchronous rectification is that MOSFETs have to be driven and Schottkies don't. Vishay Siliconix's PWM optimized MOSFETs have a lower gate charge per unit ohm, making it a lot easier and more efficient to implement a given drive scheme.

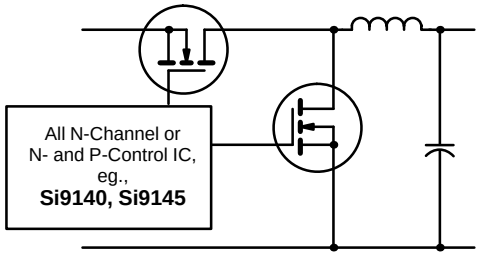

FIGURE 10. All n-channel synchronous buck converter.

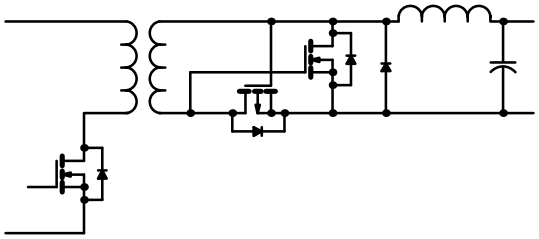

FIGURE 11. Implementation for synchronous rectification in a resonant reset forward converter.

Conclusions

Vishay Siliconix's PWM optimized MOSFET technology goes beyond the traditional improvements in on-resistance that have been the standard benchmark for MOSFETs. This technology addresses gate, crossover and conduction losses giving the dc-to-dc converter designer several valuable advantages, including faster switching times, lower gate losses, and higher overall converter efficiency with a minimum footprint.

References

Spice Analysis of low loss control/Power MOSFET Chip set for High Frequency DC-DC Converter Design. Jeff Berwick, John Huang, Wayne Grabowski and Richard K. Williams. Siliconix Inc. Charles Hymowitz and Steve Sandler. Intusoft Inc. HFPC Power Conversion, September 1996 Proceedings.

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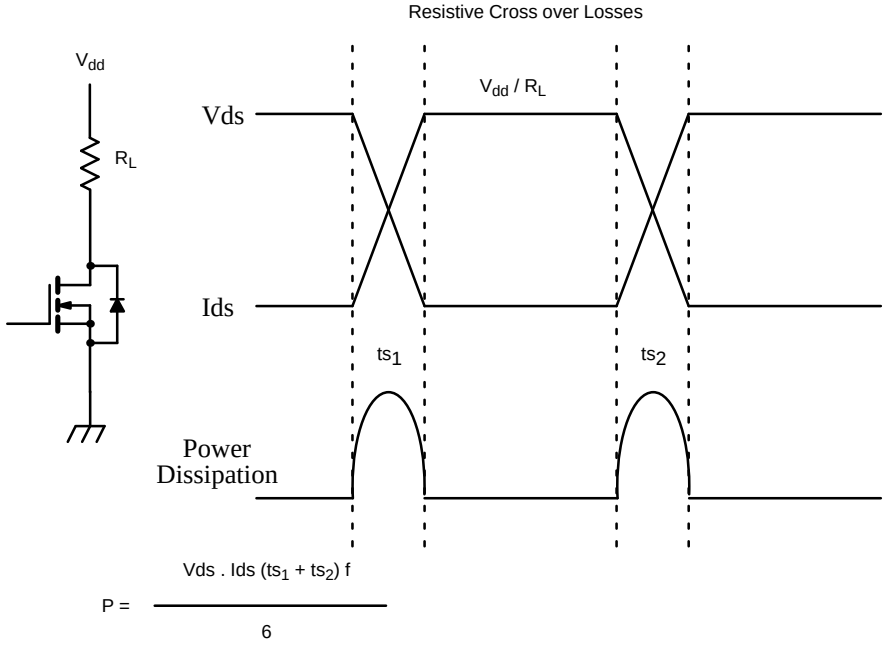
Andrew Cowell, Si9160 Boost Converter for Mobile Communications, May 1996.

APPENDIX A CROSSOVER LOSSES

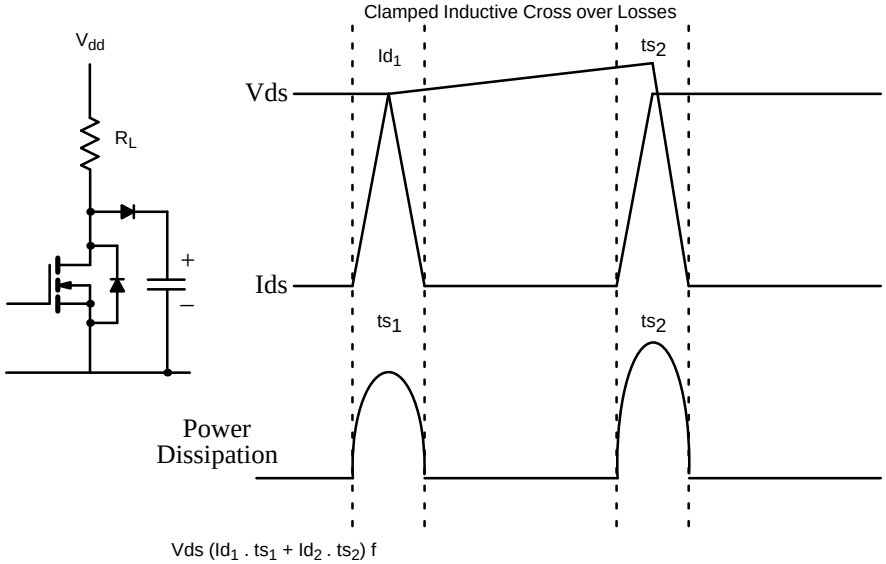
Power loss due to crossover or switching transition loss can be calculated from the generic expression below

$$P_S = f\left[tts_1 \int_0^{ts_1} V_{DS} \times I_D \, dt + ts_2 \int_0^{ts_2} V_{DS} \times I_D \, dt \right]$$

From this equation we can define the crossover losses generically for both resistive and clamped inductive loads.



$$P = \frac{Vds \cdot Ids \, (ts_1 + ts_2) \, f}{6}$$



$$P = \frac{Vds \, (Id_1 \cdot ts_1 + Id_2 \cdot ts_2) \, f}{2}$$