Bt485A

170MHz Monolithic CMOS True-Color RAMDAC™

Distinguishing Features

- 32-Bit Input Pixel Port
- 170, 150, 135, 110 MHz Pipeline Operation
- Register Compatible with Bt484/485
- 8:1, 4:1, 2:1, 1:1 Multiplexed Pixel Ports
- 24-Bit True Color 1:1, 4/3:1
- Output Current Accuracy Better than 5%
- Separate 8-Bit VGA Port
- 2x Clock Multiplier
- Differential Clock Inputs
- 64 x 64 x 2 Programmable Cursor
- Signature Analysis Registers
- Triple 8-Bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 3 x 8 Cursor Color Palettes
- Optional Sync on All Three Channels
- Voltage Reference
- Antisparkle Circuitry
- Power-Down Mode
- VRAM Shift Clock
- VGA Support in a True-Color Window
- 84-Pin PLCC Package

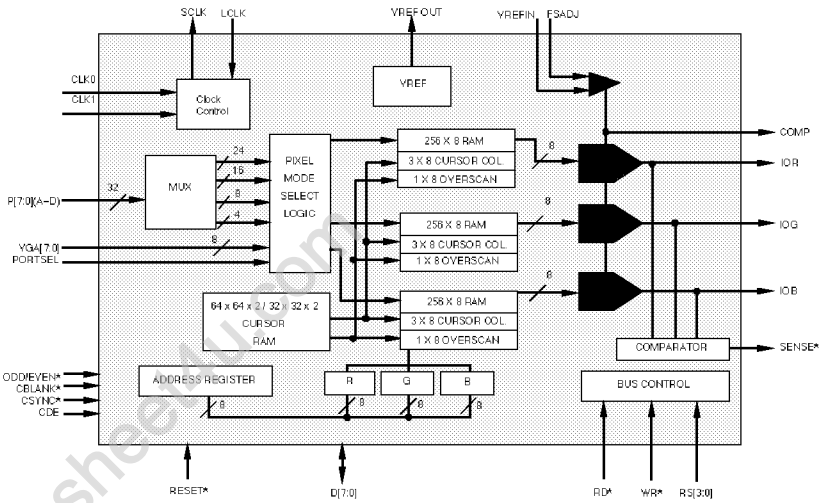
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt484
- Bt485

Functional Block Diagram



Product Description

The Bt485A RAMDAC is designed specifically for high-performance, high-resolution color graphics applications. The wide input pixel port and internal multiplexing modes enable TTL-compatible interfacing to the frame buffer, while maintaining video data rates required for high refresh rate, high-resolution color graphics. The Bt485A is functionally and software backwards-compatible to the Bt484 and Bt485.

Included are eight byte-wide pixel input ports, three 256 x 8 color lookup tables with triple 8-bit video D/A converters (configurable for either 6-bit or 8-bit D/A converter operation), and a programmable 64 x 64 x 2 cursor with its own color palette. The Bt485A may alternately be configured for a lower performance VGA mode, where 8 bits of VGA pixel data (from a VGA controller) are input through a separate VGA pixel port.

Several operational modes are supported by the 32 pins allocated for the P[0:7] (A–D) port including 8-bit pseudo color, 16- and 24-bit true color, and various packed and sparse pixel formats. The color palette may be bypassed in any of the true-color modes.

The Bt485A generates RS-343A-compatible video signals into a doubly terminated 75 Ω load.

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Circuit Description

Introduction

Bt485A is a 170 MHz RAMDAC that provides multiple multiplex operating modes and maintains Bt484/485 register compatibility. Bt485A's input pixel port can be software configured in a variety of formats for 8, 15/16, or 24-bit-per-pixel operation. Bt485A features 32-bit packed pixel format (4/3:1) which allows 24-bit true color for a 640 x 480 resolution display in only 1 MByte of frame buffer memory.

A separate VGA port is also provided on the Bt485A. A VGA controller may input 8 bits of VGA pixel data through the VGA port. The selection of the VGA or pixel port may be done through the PORTSEL input pin or programmed via a control register. In 1:1 multiplexing modes, the PORTSEL pin may be used to switch between the pixel and VGA ports on a pixel-by-pixel basis.

The pixel clock input may be provided to the Bt485A by a TTL clock. The rate of the input clock may be doubled by the Bt485A internal 2 x TTL clock multiplier. Alternatively, a differential ECL clock may be used for high-speed operation.

The color palette bypass bit controls the selection between color palette usage or bypass. Users can use the Lookup Table (LUT) for gamma correction or they can bypass the LUT for pixel sizes of 16 and 24 bits.

For battery-powered applications, a power-down mode is available. In this mode, the RAM and DACs are turned off. The RAM retains data and may be accessed for read or write operations by the MPU.

A video RAM Shift Clock (SCLK) is provided by the Bt485A, changing the cycle frequency in correspondence with the multiplex factor. This simplifies timing requirements to develop external logic for VRAM timing generation.

Circuit Description *(continued)*

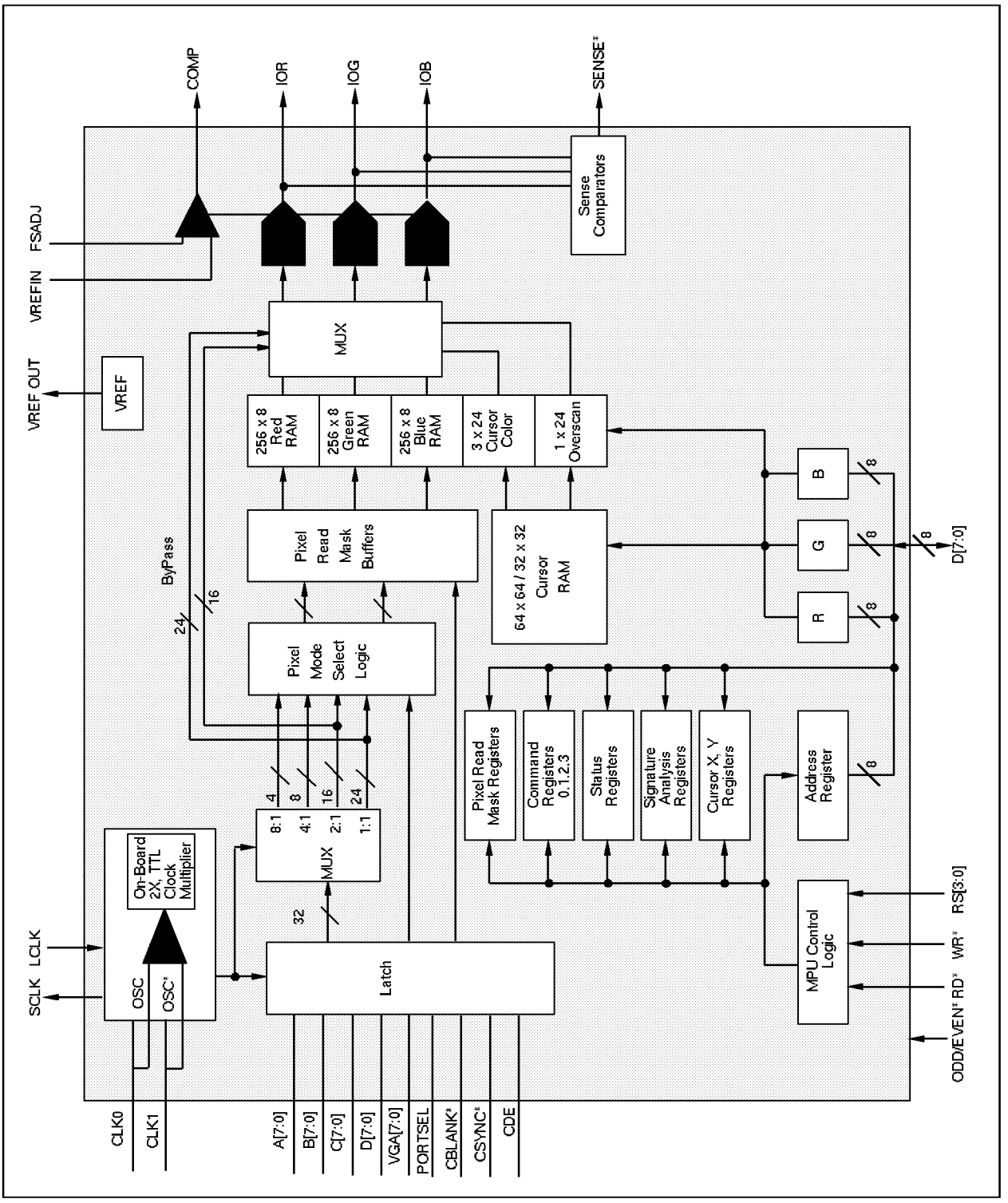


Figure 1. Bt485A Detailed Block Diagram.

Circuit Description *(continued)*

MPU Interface

As illustrated in Figure 1, the Bt485A supports a standard MPU bus interface, allowing the MPU to access the internal control registers and color palettes. MPU data is transferred in and out of the RAMDAC with D[7:0] data pins, while read/write timing is controlled by the RD* and WR* inputs.

Table 1 illustrates how the RS3–RS0 control inputs specify which control register, color palette RAM entry, overscan register, or cursor register will be accessed by the MPU. Command registers 3 and 4, and the signature analysis registers must be accessed indirectly through the status register.

The reset pin presets all the command register bits to zero, putting the device in VGA mode. The pixel read mask register is not initialized on reset and must be initialized to logical ones for proper operation.

The 8-bit address register (ADDR[7:0]) is used to address the internal color and control registers, eliminating the need for external address multiplexers. ADDR[0] corresponds to D[0] and is the least significant bit.

Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location, cursor RAM location, overscan color register, or cursor color register to be modified. RS[3:0] lines must be used to select the appropriate address register. For example, RS[3:0]=0000 selects the address register for a palette RAM or cursor RAM write operation, while RS[3:0]=0100 selects the address register for a cursor color or overscan color write operation.

The command bit CR01 is used to specify whether the MPU is reading and writing 8 bits or 6 bits of color information during each cycle. Bit CR01 must be set to a 1 if reading or writing 8-bit data.

The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS[3:0] to select the color register. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written by writing in start address and performing continuous Red, Green, Blue (RGB) write cycles until the entire block has been written. The Timing Waveforms section contains further information.

To read color data, the MPU loads the address register with the address of the color palette RAM location, cursor RAM location, overscan color register, or cursor color register to be read. RS[3:0] lines must be used to select the appropriate address register. For example, RS[3:0]=0011 selects the address register for a palette RAM or cursor RAM read operation, while RS[3:0]=0111 selects the address register for a cursor color or overscan color read operation. The contents of the color palette RAM are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color register. Following the blue read cycle, the color data is copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

To keep track of the RGB read/write cycles, the address register has two additional bits (ADDRa and ADDRb) that count modulo three (Table 2). They are reset to zero when the MPU writes to the address register but not when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of (ADDR[7:0]) are accessible to the MPU. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

When the cursor color register or overscan register are addressed, the six MSBs of the address register are don't-care conditions. Therefore, when the address register is read after an access to the cursor color register or overscan register, address register bits 7–2 may be returned as either ones or zeros.

Circuit Description *(continued)*

RS[3:0]	Access	Addressed by MPU
0000	R/W	Address Register; Palette/Cursor RAM Write
0001	R/W	6/8-bit Color Palette Data
0010	R/W	Pixel Mask Register
0011	R/W	Address Register; Palette/Cursor Ram Read
0100	R/W	Address Register; Cursor/Overscan Color Write
0101	R/W	Cursor Overscan and Color Data
0110	R/W	Command Register 0
0111	R/W	Address Register; Cursor/Overscan Color Read
1000	R/W	Command Register 1
1001	R/W	Command Register 2
1010	Read Only	Status Register
1010	R/W	Extended Register through Status Register
1011	R/W	Cursor RAM Array Data
1100	R/W	Cursor x-Low Register
1101	R/W	Cursor x-High Register
1110	R/W	Cursor y-Low Register
1111	R/W	Cursor y-High Register

Table 1. Control Input Truth Table (RS3 = MSB and RS0 = LSB).

Circuit Description *(continued)*

ADDR[9,8] (CR31, 30)	ADDR[7:0] (counts binary)	ADDR[a,b] (counts modulo 3)	RS3	RS2	RS1	RS0	Addressed by MPU
00	$00-$FF	00	0	0	0	1	Color Palette RAM (Red Component)
		01	0	0	0	1	Color Palette RAM (Green Component)
		10	0	0	0	1	Color Palette RAM (Blue Component)
00	xxxx xx00	00	0	1	0	1	Overscan Color (Red Component)
		01	0	1	0	1	Overscan Color (Green Component)
		10	0	1	0	1	Overscan Color (Blue Component)
00	xxxx xx01	00	0	1	0	1	Cursor Color 1 Red Component
		01	0	1	0	1	Cursor Color 1 Green Component
		10	0	1	0	1	Cursor Color 1 Blue Component
00	xxxx xx10	00	0	1	0	1	Cursor Color 2 Red Component
		01	0	1	0	1	Cursor Color 2 Green Component
		10	0	1	0	1	Cursor Color 2 Blue Component
00	xxxx xx11	00	0	1	0	1	Cursor Color 3 Red Component
		01	0	1	0	1	Cursor Color 3 Green Component
		10	0	1	0	1	Cursor Color 3 Blue Component
00	$00-$7F	N/A	1	0	1	1	Cursor RAM Array, Plane 0 (32 x 32 x 2 Cursor Only)
00	$80-$FF	N/A	1	0	1	1	Cursor RAM Array, Plane 1 (32 x 32 x 2 Cursor Only)
00	$00-$FF	N/A	1	0	1	1	Cursor RAM Array, Plane 0 (64 x 64 x 2 Cursor Only)
01	$00-$FF	N/A	1	0	1	1	Cursor RAM Array, Plane 0 (64 x 64 x 2 Cursor Only)
10	$00-$FF	N/A	1	0	1	1	Cursor RAM Array, Plane 1 (64 x 64 x 2 Cursor Only)
11	$00-$FF	N/A	1	0	1	1	Cursor RAM Array, Plane 1 (64 x 64 x 2 Cursor Only)

Table 2. Address Register Operation and Auto-Incrementing.

Circuit Description *(continued)*

Additional Information

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM and the color registers (R, G, and B in Figure 1) are synchronized by internal logic, and take place in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between RGB registers and lookup table RAMs occurs.

The control registers can also be accessed through the address register in conjunction with the RS[3:0] inputs as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

Accessing the Cursor RAM Array

Bt485A's cursor RAM is accessed in a planar format, where the upper address bit is used to determine whether plane 0 or 1 of cursor RAM is being accessed. When the 32 x 32 x 2 cursor RAM is accessed, only seven address bits are used. The eighth bit determines which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1.

The 64 x 64 x 2 cursor RAM is also accessed in a planar format. The larger cursor RAM can be accessed after bit CR32 in Command Register 3 has been set to a logical one. Bits CR30 and CR31 in Command Register 3 become the load inputs to the two Most Significant Bits (MSBs) of a 10-bit address counter; therefore, these bits must be written in Command Register 3 before the lower 8 bits are written to the address counter through the MPU port. In the planar format, only 9 address bits are used. The 10th bit is to determine which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1. After each access in the planar format, the address increments. The MPU uses ADDR, a binary address counter, to access the cursor RAM array (see Table 2). ADDR is the same binary counter used for RGB auto-incrementing. In the case of the 64 x 64 x 2 cursor RAM, command bits CR30 and CR31 are used as the extended bits (MSB) of the binary counter creating a 10-bit binary address counter.

Any write to ADDR after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until cursor RAM array has again been accessed. Cursor auto-incrementing will then begin from the address written. A read from the ADDR does not reset the cursor auto-incrementing logic. The color palette RAM and the cursor RAM share the same external address register. MPU addressing for this and all other registers is determined by the external register select lines RS[3:0] (see Table 1).

6-Bit / 8-Bit Operation

Bt485A can be configured to present 6 or 8 bits of color information to its digital-to-analog convertors. In an 8-bit operation, the MPU uses all of the 8 data lines (D[7:0]) to read or write color information. D[0] is the Least Significant Bit (LSB) and D[7] is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D[0] the LSB and D[5] the MSB of color data. When writing color data, D[6] and D[7] are ignored. During color read cycles, D[6] and D[7] are logical zeros.

The command bit CR01 is used to specify whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

In the 6-bit mode, the Bt485A's full-scale output current will be about 1.5 percent lower than when in the 8-bit mode. This is because the two LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Power-Down Mode

The Bt485A incorporates a power-down capability, controlled by command bit CR00. While CR00 is a logical zero, the Bt485A functions in the normal operating mode.

While CR00 is a logical one, the DACs and power to the RAM are turned off. Note that the RAM still retains the data. Also, the MPU may read or write to the RAM while the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. The DACs output no current, and the command registers may still be written to or read by the MPU. The output DACs require about one second to turn off (sleep mode) or turn on (normal), depending on the compensation capacitor used (see Video Generation in the Circuit Description section for further information).

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

Circuit Description *(continued)*

Frame Buffer Clocking

The video frame buffer Shift Clock (SCLK) is generated by the Bt485A (see Figure 2). SCLK is used for clocking the VRAMs serial outputs to provide pixel data to the RAMDAC. SCLK is 1/8, 1/4, or 1/2 the pixel clock rate, depending on which multiplexing mode is selected (see Table 3). SCLKs divide ratio is the same as the pixel data multiplexing ratio. In the 1:1/VGA mode, SCLK is equal to pixel clock rate. In the packed pixel mode, SCLK is not a true harmonic of the pixel clock (see Figure 4).

Clock inputs may be provided externally through pins CLK0 and CLK1. When CLK0 and CLK1 pins are used, there is an option of using two TTL clocks or using a differential ECL clock for high speeds. The 2x TTL clock multiplier may be used with the TTL clocks only.

Bt485A outputs SCLK to the graphics controller. In return, the graphics controller sends a Load Clock (LCLK) back to the RAMDAC which is generated based on the SCLK output. The pixel inputs to Bt485A P[0:7] (A–D) are always latched on the rising edge of LCLK. For the Bt485A to latch the correct pixel inputs, SCLK and LCLK must be phased appropriately. There is an invalid region where an LCLK rising should not occur with respect to an SCLK rising edge (see Figure 3a). However, this can be corrected by inverting the SCLK output so that the LCLK rising edge is not referenced to an SCLK falling edge. By setting CR26=1, the SCLK output is inverted internally, placing the invalid region in a different phase of SCLK. The LCLK rising edges, therefore, will occur outside of the invalid region (see Figure 3b).

SCLK is designed to drive only a single CMOS load. To ensure the integrity of the color palette, the device should be put in sleep mode before switching between 1:1/VGA and other MUX Modes.

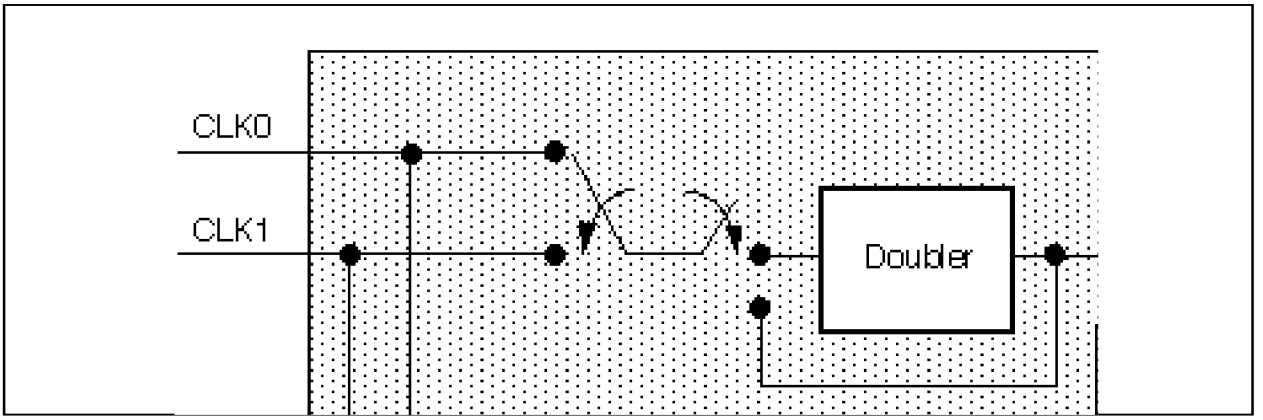


Figure 2. Bt485A Clocking.

MUX Ratio	SCLK/LCLK	VRAM = 32
8:1	Divide by 8	4 bpp
4:1	Divide by 4	8 bpp
2:1	Divide by 2	16 bpp 8 bpp
1:1	Divide by 1	16 bpp 24 bpp VGA
4/3:1	Figure 4	24-bit Packed Pixel

Table 3. Frame Buffer Clocking in Relation to Pixel Depth.

Circuit Description *(continued)*

Onboard 2x TTL Clock Multiplier

The Bt485A provides an on-board 2x TTL clock multiplier for high-speed operations. The clock multiplier can be enabled or disabled by programming bit CR33 in Command Register 3 (see Command Register 3 in the Internal Registers section). Upon applying a RESET signal, the clock multiplier is disabled until bit CR33 is written to a logical one. Either CLK0 or CLK1 can be doubled internally. For operation above 110 MHz, the clock multiplier must be used.

Differential Clock Inputs

For high-speed operations, an optional differential ECL clock input is specified. The CLK0 and CLK1 inputs can be used together as differential ECL inputs for external clock by setting CR34 = 1. If a differential ECL mode is used (CR34 = 1), then the state of bits CR33 and CR24 are ignored.

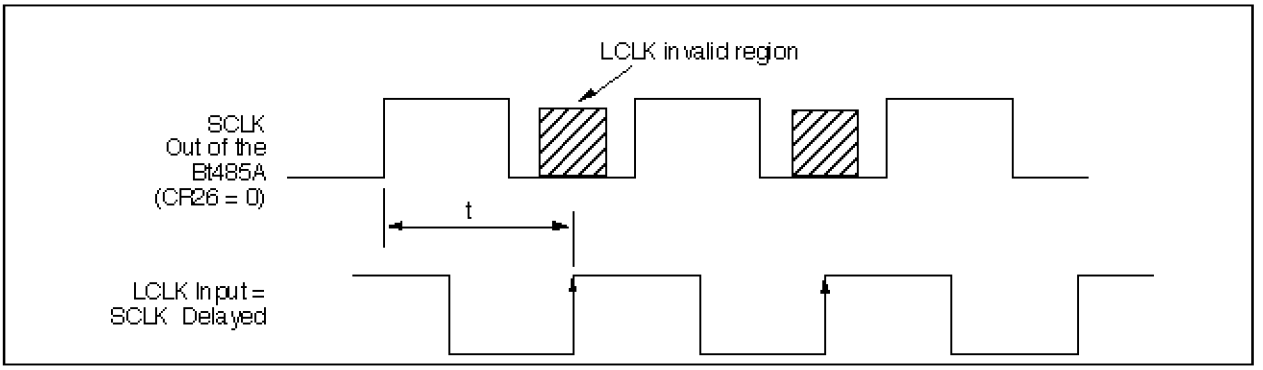


Figure 3(a). SCLK to LCLK Timing Restriction (CR26 = 0).

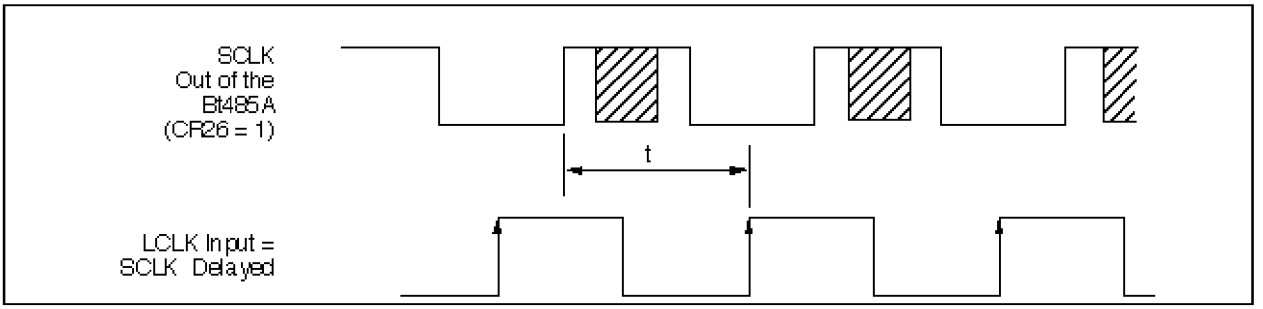


Figure 3(b). SCLK to LCLK Timing Restriction (CR26 = 1).

Circuit Description *(continued)*

Frame Buffer Pixel Port Interface

There are four 8-bit pixel ports, (A–D), used to interface to the frame buffer memory.

Video input data ports A–D are designated in this manner to represent the order of pixel data presentation. Port A always corresponds to the first pixel of the first line of the display. This is the first pixel fed to the analog outputs, followed by B, then C, and finally D, repeating the pattern ABCD until the first scan line is completely displayed.

Modes of Operation

4 Bits/Pixel Operation (8:1 MUX)

The 4-bit/pixel configuration may be achieved by multiplexing 32 input bits (A–D) in a ratio of 8:1. The 4-bit pixel ports are independent of one another and are configured as P[7:4] (A–D) and P[3:0] (A–D).

The pixel bits are latched on the rising edge of the LCLK. The 4 bits from each port select 1 of 16 locations (RAM address 0–15) in the palette in the order presented in Table 4.

8 Bits/Pixel Operation (4:1 and 2:1 MUX)

The 8 bit/pixel configuration may be achieved by multiplexing 32 input pins (A–D) in a ratio of 4:1, or alternatively multiplexing 16 input pins (A–B) in a 2:1 ratio. The 8-bit pixel ports are independent of one another and are configured as P[7:0] (A–D).

The pixel bits are latched on the rising edge of LCLK. The 8 bits from each port will select 1 of 256 locations in the palette as presented in Table 4.

16 Bits/Pixel Operation (2:1 and 1:1 MUX)

The 16 bits/pixel configuration may be achieved by multiplexing 32 input bits (A-D) in a ratio of 2:1. This results in two independent 16-bit pixel ports, (B–A) and (D–C).

Alternatively, a 16 bit/pixel mode may be achieved by dividing input bits (A–D) into two 16-bit ports (B–A) and (D–C) and selecting one in a 1:1 MUX ratio. Selection between the two 16-bit ports is made by bit CR10 in Command Register 1.

The pixel input bits are latched on the rising edge of LCLK. The pixel bits in these modes are in RGB color formats of 5:5:5 or 5:6:5. In the 2:1 MUX mode, P7D and P7B are ignored internally when the 5:5:5 color format is selected (see Tables 5 and 6). In the 1:1 MUX mode, however, P7D may be used instead of CR10 to switch between (B–A) and (D–C) multiplexed modes, when 5:5:5 color format is selected. This allows the (B–A) and (D–C) ports to be selected on a pixel-by-pixel basis in the 5:5:5 color format. The real-time switch enable bit must be set appropriately (CR11=1) for the above feature to be enabled. Real-time pixel port switching is not supported for 5:6:5 RGB color format.

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the correct color information is passed on to the respective DACs.

Bit CR22 in Command Register 2 determines whether palette addressing is sparse or contiguous. For sparse palette addressing, each color component of pixel data is mapped to the MSBs of the respective palette address; the LSBs are set to zero. For contiguous palette addressing, each color component of the pixel data is mapped to the LSBs of the respective palette address; the MSBs are set to zero. The color palette values indexed, for either sparse or contiguous addressing, are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32 K or 64 K simultaneous colors. The DACs can be configured for 6 or 8 bits of resolution in this mode.

24 Bits/Pixel Operation (1:1 MUX)

When multiplexing 1:1 in a 24-bits/pixel mode, pixel bits (C–A) are latched on the rising edge of LCLK, and pixel inputs D are ignored. The RGB color format in these modes is 8:8:8 (see Table 7).

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the independent RGB color values are passed on to the respective DACs. When 8:8:8 color format is selected, the display can contain 16.8 million simultaneous colors. The DACs should be configured for 8 bits of resolution in this mode (CR14=1 and CR01=1).

CR25	Portsel	CR11	CR10	P7D	CR12	CR13	CR16,15	CR17	CR36,35	Ports MUXed	MUX Rate	Operating Modes
X	0	X	X	X	X	X	XX	X	XX	VGA[P0]	1:1	VGA
0	X	X	X	X	X	X	XX	X	XX	VGA[P0]	1:1	VGA
1	1	X	X	Data	X	X	11	0	00	PT7-4[CA] PT3-0[CA] PT7-4[CB] PT3-0[CB] PT7-4[CC] PT3-0[CC] PT7-4[CD] PT3-0[CD]	8:1	4 Bits/Pixel (Big Endian)
1	1	X	X	Data	X	X	11	1	00	PT3-0[CA] PT7-4[CA] PT3-0[CB] PT7-4[CB] PT3-0[CC] PT7-4[CC] PT3-0[CD] PT7-4[CD]	8:1	4 Bits/Pixel (Little Endian)
1	1	X	X	Data	X	X	10	X	00	PT7-0[CA] PT7-0[CB] PT7-0[CC] PT7-0[CD]	4:1	8 Bits/Pixel
1	1	X	X	X	X	X	00	X	11	PT7-0[CA] PT7-0[CB]	2:1	8 Bits/Pixel
1	1	X	X	X	0	0	01	X	00	PT7-0[CB–A] PT7-0[CD–C]	2:1	16 Bits/Pixel (5:5:5) (See Table 5)
1	1	X	X	X	0	1	01	X	00	PT7-0[CB–A] PT7-0[CD–C]	2:1	16 Bits/Pixel (See SixSee Table 6)
1	1	0	0	X	1	0	01	X	00	PT7-0[CB–A]	1:1	16 Bits/Pixel (5:5:5) (See Table 5)
1	1	0	1	X	1	0	01	X	00	PT7-0[CD–C]	1:1	16 Bits/Pixel (5:5:5)
1	1	1	X	0	1	0	01	X	00	PT7-0[CB–A]	1:1	16 Bits/Pixel (5:5:5)
1	1	1	X	1	1	0	01	X	00	PT7-0[CD–C]	1:1	16 Bits/Pixel (5:5:5)
1	1	X	X	X	1	1	01	X	00	PT7-0[CB–A]	1:1	16 Bits/Pixel (5:6:5) (See Table 6)
1	1	X	X	X	X	X	00	X	00	PT7-0[CB–A]	1:1	24 Bits/Pixel (See Table 7)
1	1	X	X	X	X	X	10	X	01	PT7-0[D–A]	4:3:1	24 Bits/Packed Pixel (See Table 8)

Table 4. Modes of Operation (Pixel Port Configuration).

Circuit Description *(continued)*

BIT	MSB																			LSB
Format	S	R	R	R	R	R	G	G	G	G	G	G	G	G	G	B	B	B	B	B
Port 1	S	P0B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A	P7B	P6B	P5B	P4B
Port 2	S	P0D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C	P7D	P6D	P5D	P4D

NOTE: If bit CR11 in Command Register 1 is a logical zero, then S = CR10 bit. 16-bits/pixel port switch control (1:1 multiplexing, CR12 = 1).
If bit CR11 in Command Register 1 is a logical one, then S = P7D bit. real-time pixel port switch (1:1 multiplexing, CR12 = 1).

Table 5. 5:5:5 RGB Color Format for 2:1 and 1:1 Multiplexing Modes.

BIT	MSB																			LSB
Format	R	R	R	R	R	R	G	G	G	G	G	G	G	G	G	B	B	B	B	B
Port 1	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A	P7B	P6B	P5B	P4B
Port 2	P7D	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C	P7D	P6D	P5D	P4D

Table 6. 5:6:5 RGB Color Format for 2:1 and 1:1 Multiplexing Modes.

BIT	MSB																							LSB
Format	R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B
Port 1	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A

Table 7. 24-Bits/Pixel RGB Color Format for 1:1 Multiplexing Mode.

Circuit Description *(continued)*

24 Bit Packed-Pixel Operation (4/3:1 MUX)

This mode will also be referred to as the 24-bit true color packed-pixel format. It is selected through bits CR36, CR35=01 in Command Register 3 and multiplexes input data on P[7:0] (A–D) in a 4/3:1 ratio. Each 32-bit "packet" of data on P[7:0] (A–D) has more data than is required for one 24-bit RGB pixel. A sequence of three packets delivers 4 pixels worth of data.

In this mode, the Bt485A generates three SCLKs for every four pixel clocks (see Figure 4). The SCLK is intended to be used by the graphics controller as an input from which it generates a VRAM shift clock and an LCLK for the Bt485A. LCLK latches the pixel data on P[7:0] (A–D) into the device. The active video line length, horizontal interval, and vertical interval each must be an integral number of four pixel clocks or three SCLKs (see Table 8).

To generate four 24-bit pixels, the Bt485A requires three consecutive 32–bit packets of data to be loaded. The re-ordering of the bytes from a 32-bit format to a 24-bit format is automatically taken care of by the Bt485A. This re-ordering sequence repeats itself every four pixel clocks or three SCLKs.

For the Bt485A and the graphics controller to be in agreement about what any given packet of 32 bits represents, they must be synchronized to each other. The Bt485A assumes this responsibility and determines the phase of the controller by detecting the rising edge of the CDE signal generated by the controller (CDE should be tied to CBLANK* when overscan is not being used). The data latched by the first LCLK after CDE goes high should be the first packet of active video (B0, G0, R0, B1; see Figure 4). If the Bt485A is not expecting it (i.e. the controller and Bt485A are not synchronized) one less SCLK edge on that scan line is generated. This will shift the phase relationship of the controller CDE relative to the Bt485A SCLK sequence by 1 SCLK edge for the remainder of that scan line. The Bt485A will continue to do this on each rising edge of CDE (i.e. at the beginning of every scan line) until synchronization has been established. The Bt485A will not generate the correct colors on the display scan lines when it is not synchronized with the graphics controller.

Once synchronization has been established, it will persist since every rising edge of CDE will be a multiple of four pixel clocks (three SCLKs) apart. Therefore, synchronizing is only necessary at start-up or in the case of a random error such as a lost data packet.

Three different situations can exist after system start-up in this mode. They are illustrated as cases A, B, and C in Figure 4.

Case A shows a timing diagram with the Bt485A and graphics controller in synchronization. In case B, the Bt485A detects an unsynchronized condition when CDE is sampled high and drops one SCLK. This also occurs in case C. When the system starts up with the first scan line in case C, case B will occur on the second scan line and case A on the third scan line. Case A will always be followed by another scan line of case A; therefore, synchronization will at worst always be established by the third scan line.

Pixel Port	P[7:0] (A)	P[7:0] (B)	P[7:0] (C)	P[7:0] (D)
First 32-Bit Load	B0	G0	R0	B1
Second 32-Bit Load	G1	R1	B2	G2
Third 32-Bit Load	R2	B3	G3	R3

Table 8. 24 Bit Packed Pixel 4/3:1 MUX.

Circuit Description *(continued)*

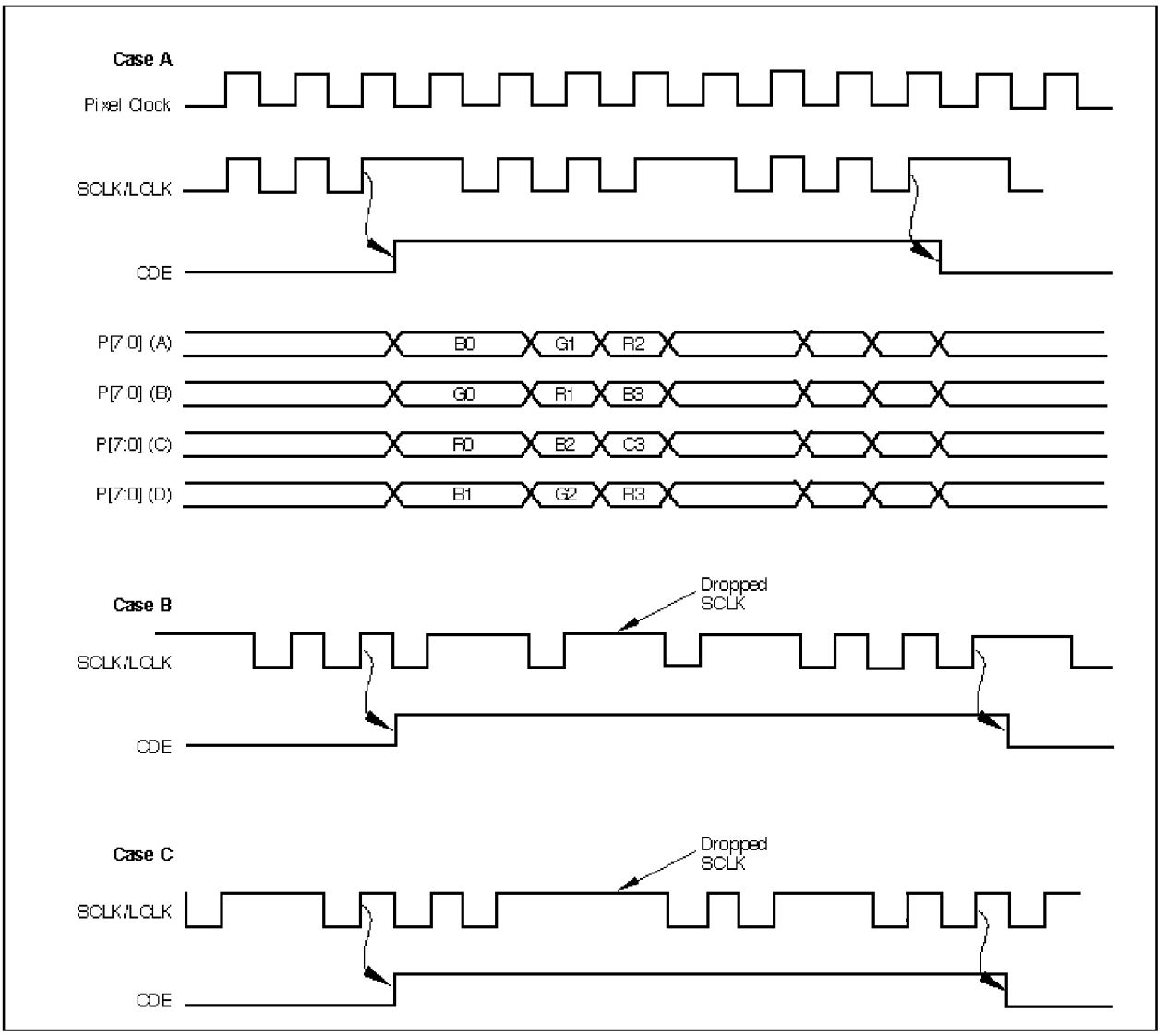


Figure 4. Pixel Data and Clock Format, 24-Bit Packed Pixel 4/3:1 MUX.

Circuit Description *(continued)*

By using 32 pixel inputs in the 24-bits/pixel mode, frame buffer memory may be used more efficiently. To support a 640 x 480 resolution with 24 bits of color information per pixel you need just under 1 Mbyte of frame buffer memory (640 x 480 x 3=921600 bytes).

If only 24 of the pixel inputs are used, 8 bits of the 32-bit memory will have to be ignored on every load cycle; therefore, greater than 1 Mbyte of memory would be needed to support 640 x 480 x 24. Figure 5a shows how the frame buffer can be formatted if 8 bits of the 32-bit word have to be ignored on every load cycle. Figure 5b shows how the frame buffer can be formatted if all 32 bits are used on every load cycle.

Bit CR14 in Command Register 1 enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the independent RGB color values are passed on to the respective DACs. When 8:8:8 color format is selected, the display can contain 16.8 million simultaneous colors. The DACs should be configured for 8 bits of resolution in this mode (CR14=1 and CR01=1).

The 2x Clock multiplier may not be used in Packed Pixel Mode.

	0–7	8–15	16–23	24–31
0	B0	G0	R0	X
1	B1	G1	R1	X
2	B2	G2	R2	X
3	B3	G3	R3	X
•				
•				
•				

Figure 5(a). Example of Frame Buffer Format Not Using All the Pixel Input Pins.

	0–7	8–15	16–23	24–31
0	B0	G0	R0	B1
1	G1	R1	B2	G2
2	R2	B3	G3	R3
3	B4	G4	R4	B5
•				
•				
•				

Figure 5(b). Example of Frame Buffer Format Using All the Pixel Input Pins.

Circuit Description *(continued)*

VGA Port

Bt485A provides an 8-bit input port to support VGA pixel data. The data on VGA[7:0] pins is latched on the rising edge of LCLK. The 8-bit VGA data forms an index into the color palette, selecting 1 of 256 colors. Upon power up, Bt485A is configured in the VGA mode.

Bt485A can select between the VGA port (VGA[7:0]) and the pixel port (P[7:0] (A–D)) using the PORTSEL input pin. A logical zero on the PORTSEL pin ensures that the VGA port is selected. A logical one on the PORTSEL pin selects the 32-bit pixel port.

The PORTSEL pin may be used to switch between the VGA and pixel ports on a pixel-by-pixel basis in the 1:1 MUX mode. Only CLK0 input must be used when switching between VGA and pixel ports on a pixel-by-pixel basis. The PORTSEL pin can also be used to switch between VGA and the pixel ports on a frame-by-frame basis in 2:1, 4:1, or 8:1 MUX modes. CLK1 should be used when switching between the VGA and pixel ports on a frame-by-frame basis.

Pixel Read Mask Register

The pixel data can be masked with the 8-bit pixel read mask register before being transferred to the color palette. The pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation, except when the true-color bypass is enabled.

Table 9 shows pixel index masking for different modes of operation. In the 15/16- and 24-bit true color modes, the same 8-bit pixel read mask register is ANDed with all three color components. In the 4-bits/pixel mode, each pixel is first unpacked and then ANDed with the 4 LSBs of the pixel read mask register.

The pixel read mask register is not initialized at the power-up/reset and must be initialized by the user to logical ones for proper operation.

	MSB							LSB	
Pixel Mask Register	7	6	5	4	3	2	1	0	Register Bits
VGA Data	7	6	5	4	3	2	1	0	Palette Index
4-Bits/Pixel	x	x	x	x	3	2	1	0	Palette Index
8-Bits/Pixel	7	6	5	4	3	2	1	0	Palette Index
16-Bits/Pixel 5:5:5 Format SPARSE	7 7 7	6 6 6	5 5 5	4 4 4	3 3 3	x x x	x x x	x x x	Red Palette Index Green Palette Index Blue Palette Index
16-Bits/Pixel 5:5:5 Format CONTIGUOUS	x x x	x x x	x x x	4 4 4	3 3 3	2 2 2	1 1 1	0 0 0	Red Palette Index Green Palette Index Blue Palette Index
16-Bits/Pixel 5:6:5 Format SPARSE	7 7 7	6 6 6	5 5 5	4 4 4	3 3 3	x 2 x	x x x	x x x	Red Palette Index Green Palette Index Blue Palette Index
16-Bits/Pixel 5:6:5 Format CONTIGUOUS	x x x	x x x	x 5 x	4 4 4	3 3 3	2 2 2	1 1 1	0 0 0	Red Palette Index Green Palette Index Blue Palette Index
24-Bits/Pixel 8:8:8 Format	7 7 7	6 6 6	5 5 5	4 4 4	3 3 3	2 2 2	1 1 1	0 0 0	Red Palette Index Green Palette Index Blue Palette Index

Table 9. Pixel Index Masking.

Circuit Description *(continued)*

Cursor Operation

The Bt485A has an on-chip, three-color, user-definable cursor. Upon power-up, Bt485A is in VGA mode and the cursor is disabled. A 64 x 64 x 2 or 32 x 32 x 2 cursor may be selected by writing bit CR32 in Command Register 3. The cursor can be used in both interlaced and noninterlaced systems.

The pattern for the cursor is stored in the cursor RAM, which may be accessed by the MPU at any time (see Accessing the Cursor RAM Array in the Circuit Description section). Three cursor color registers exist, each of which stores 24 bits of cursor color information. These registers may also be accessed by the MPU. Finally, Bt485A supports three cursor modes an shown in Table 10 (three-color cursor, PM/Window cursor, X-Windows cursor). Bits CR20 and CR21 in Command Register 2 determine which cursor mode is to be used.

The cursor position (Xp, Yp) is set through the cursor position registers. The cursor position is referenced to the lower right corner of the cursor (see Figure 6). A (0,0) written to the cursor position registers will place the cursor off the screen. A (1,1) written to the cursor position registers will place the lower right pixel of the cursor on the upper left corner of the screen. Refer to Cursor Registers in the Internal Registers section for more detail on cursor position coordinates.

Only one cursor pattern is displayed per frame at the specified location, regardless of the number of updates to (Xp, Yp) during that frame. The cursor's x- and y-position registers are loaded after the upper byte of Yp has been written. There are no restrictions on updating (Xp, Yp) other than both cursor position registers must be written when the cursor location is updated. The cursor position will remain at the same location if (Xp, Yp) values are not changed.

Figure 6 shows the cursor on a display with overscan boundary. As shown in this figure, cursor positioning is relative to the CDE signal, and is not dependent on the CBLANK* signal. If CBLANK* is deasserted but CDE is not yet asserted, overscan data is displayed. Only after CDE is asserted, is the cursor position determined. The cursor Xp position is relative to the first rising edge of LCLK when CDE is sampled at logical one after the CDE vertical blanking interval has been determined.

The Bt485A detects CDE vertical blanking by measuring the interval between CDE transitions. If a CDE transition from logical zero to logical one (as determined by LCLK) does not occur within 2,048 pixel clocks in the 1:1 MUX mode, then vertical blanking is asserted. The cursor timing is based on LCLK in the 1:1 MUX mode. In 8:1, 4:1, or 2:1 MUX modes, cursor timing is based on the Pixel Clock.

Bt485A's cursor can be used in both interlaced and noninterlaced systems. Bit CR23 allows the selection between interlaced and non-interlaced modes. In noninterlaced systems every scan line is displayed in consecutive order. In interlaced systems, each display scan displays either the odd or even field, depending on the state of the ODD/EVEN* pin.

The cursor pattern is held in the cursor RAM in the planar format. As shown in Figure 7, the first byte of the two planes combine to form the index to the cursor color register. In non-interlaced mode, every row of cursor RAM (plane 0, plane 1) is displayed consecutively, but in interlaced mode odd and even fields have to be assigned to rows of cursor RAM data.

When using the cursor in the interlaced mode, the first line displayed depends on the stage of the ODD/EVEN* pin. When the full length of the interlaced cursor is displayed, the first line displayed depends on the value of Yp as well as the state of the ODD/EVEN* pin.

The full length of the cursor is displayed on the screen when Yp is greater than or equal to 64 (32) and less than or equal to 4,095 for a 64 x 64 (32 x 32) cursor. If Yp is an even number, the data in row 0 of the cursor RAM will be displayed as the first scan line of the even field (ODD/EVEN*=0), and the data in row 1 of the cursor RAM will be displayed as the first scan line of the odd field (ODD/EVEN*=1). The subsequent odd or even scan lines will correspond to every alternate RAM location.

If Yp is an odd number, the data in row 0 of the cursor RAM will be displayed as the first scan line of the odd field (ODD/EVEN*=1), and the data in row 1 of the cursor RAM will be displayed as the first scan line of the even field (ODD/EVEN*=0). The subsequent odd or even scan lines will correspond to every alternate RAM location.

If the length of the cursor is only partially seen on the screen, then Yp is less than 64 (32). In this case, the interlaced cursor display does not depend on whether Yp is odd or even. The cursor RAM location corresponding to the first line of the partial cursor will be displayed as the first scan line of the even field (ODD/EVEN*=0). The cursor RAM location corresponding to the second line of the partial cursor will be displayed as the first scan line of the odd field (ODD/EVEN*=1). The subsequent odd or even scan lines will correspond to every alternate RAM location.

Circuit Description *(continued)*

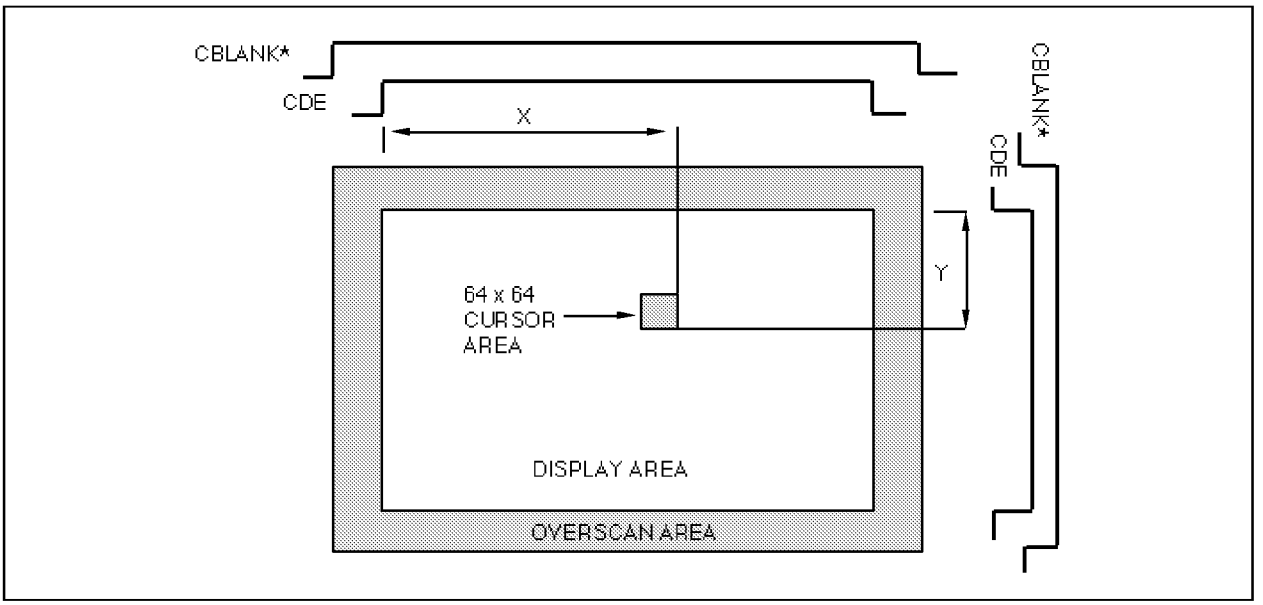


Figure 6. Cursor Positioning.

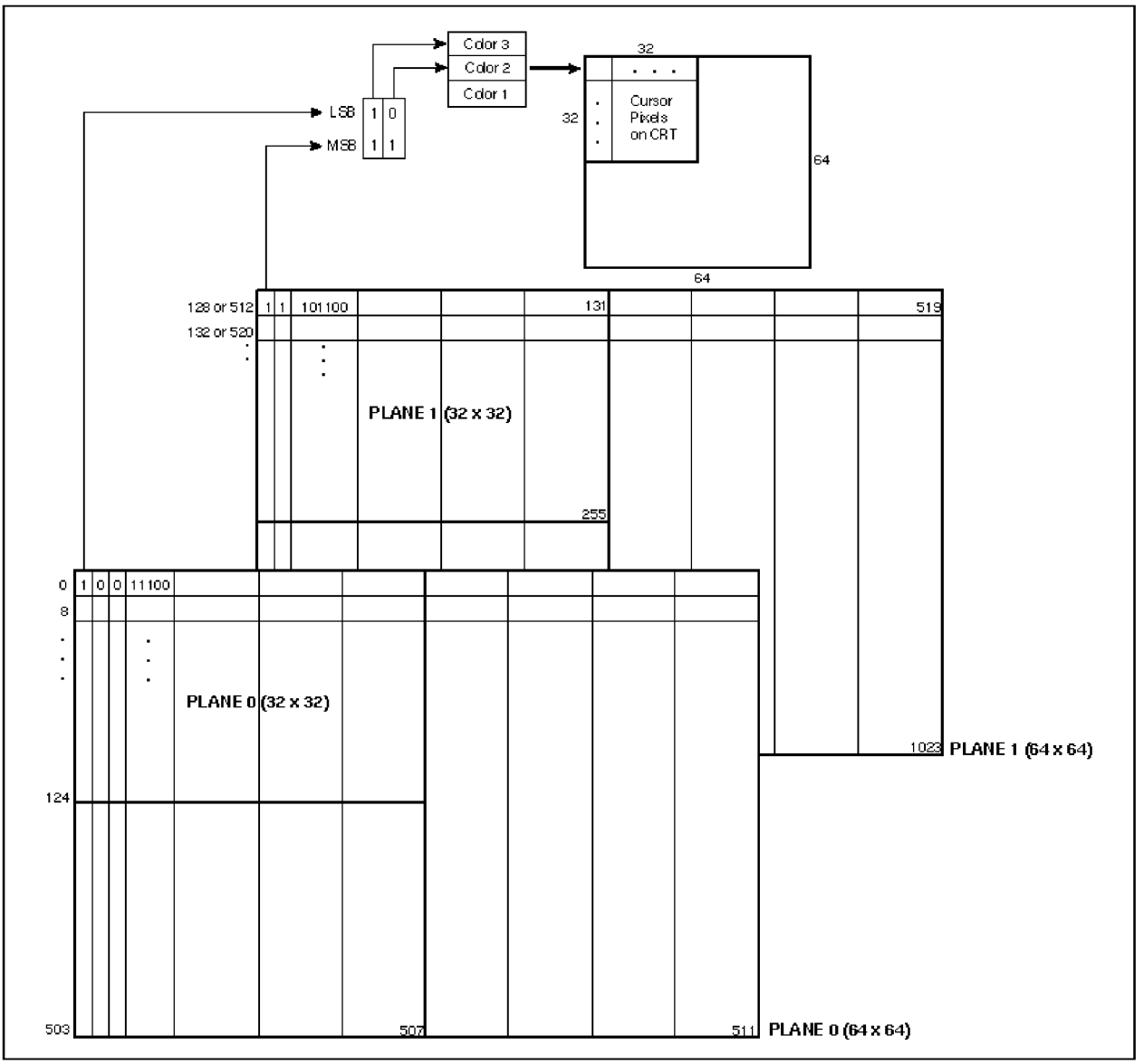


Figure 7. Planar Pixel Format and Cursor RAM Array Pixel Mapping for Both 32 x 32 and 64 x 64 Cursors.

Circuit Description *(continued)*

Cursor Color Support

The cursor has three modes for color selection. Bits CR21 and CR20 in Command Register 2 determine which cursor mode is to be used. Mode 1 is a three-color cursor, mode 2 is referred to as a PM/Window cursor, and mode 3 is referred to as an X-Windows cursor (see Table 10).

Highlight Logic

The highlight logic is enabled in Cursor Mode 2 when both plane data (plane 1 and plane 0) are logical ones (see Table 10). When the highlight logic is enabled, it ensures that the pixel highlighted has a unique color. This is because the highlight logic bit-wise complements the 24- or 18-bit palette or bypass data supplied to the DACs.

Video Generation

The CSYNC* and CBLANK* inputs are latched on the rising edge of LCLK to maintain synchronization with the color data. They add appropriately weighted currents to the analog outputs and produce the specific output levels required for video applications, as illustrated in Figures 10 and 11.Tables 11 and 12 detail how the CSYNC* and CBLANK* inputs modify the output levels.

The CR05 command bit is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. Command bits CR02, CR03, and CR04 specify whether the RGB outputs contain sync information.

SENSE* Output

The SENSE* output (and status bit SR3) determine the presence of a CRT monitor and, with diagnostic code, the difference between a loaded or an unloaded RGB line can be discerned. The reference voltage for the SENSE* circuitry is generated by dividing down the voltage reference on the VREFIN pin. If the DAC output level (IOR, IOG, and IOB) going to the comparator input is:

Iout *DAC load $\leq$ 230 mV	CRT present (SENSE* =1)
Iout *DAC load $\geq$ 410 mV	CRT not present (SENSE* =0)

The SENSE* output can drive only one CMOS load. For a given DAC output current, the DAC output voltage varies depending on the DAC load. Examples of two types of termination schemes are depicted in Figure 8. In Scheme A, the DAC output is tripled when the monitor is not present. In Scheme B, the DAC output is doubled when the monitor is not present.

For example, if termination scheme A is used, the DAC value should be selected such that it is less than 230 mV (terminated) and when tripled it is greater than 410 mV (unterminated). A DAC output value of 140 mV achieves just that.

Each step of DAC output = 17.62 mA* 50 Ohms/63
= 14 mV

Programming the outputs of the DAC to drive 140 mV on a 50 ohm termination means a DAC code of:

140 mV/14 mV = 10 = 0Ah

By programming 0Ah in the DAC, the SENSE* circuitry will detect a logical zero (CRT present) with a 50 ohm load (140 mV), and will detect a logical 1 (CRT not present) with a 150 ohm load (420 mV).

Alternatively, if termination scheme B is used, the DAC value should be selected such that it is less than 230 mV (terminated) and when doubled it is greater than 410 mV (unterminated). A DAC output value of 210 mV achieves that.

Each step of DAC output = 17.62 mA* 37.5 Ohms/63
= 10.5 mV

Programming the outputs of the DAC to drive 224mV on a 37.5 ohm termination means a DAC code of:

210 mV/10.5 mV = 20 = 14h

By programming 10h in the DAC, the SENSE* circuitry will detect a logical zero (CRT present) with a 37.5 ohm load (224 mV), and will detect a logical 1 (CRT not present) with a 75 ohm load (448 mV).

PLANE 1	PLANE 0	MODE 1 (Three Color)	MODE 2 (PM/Windows)	MODE 3 (X-Windows)
0	0	Palette Data	Cursor Color 1	Palette Data
0	1	Cursor Color 1	Cursor Color 2	Palette Data
1	0	Cursor Color 2	Palette Data	Cursor Color 1
1	1	Cursor Color 3	Palette Data Complement	Cursor Color 2

Table 10. Overlay Color Modes.

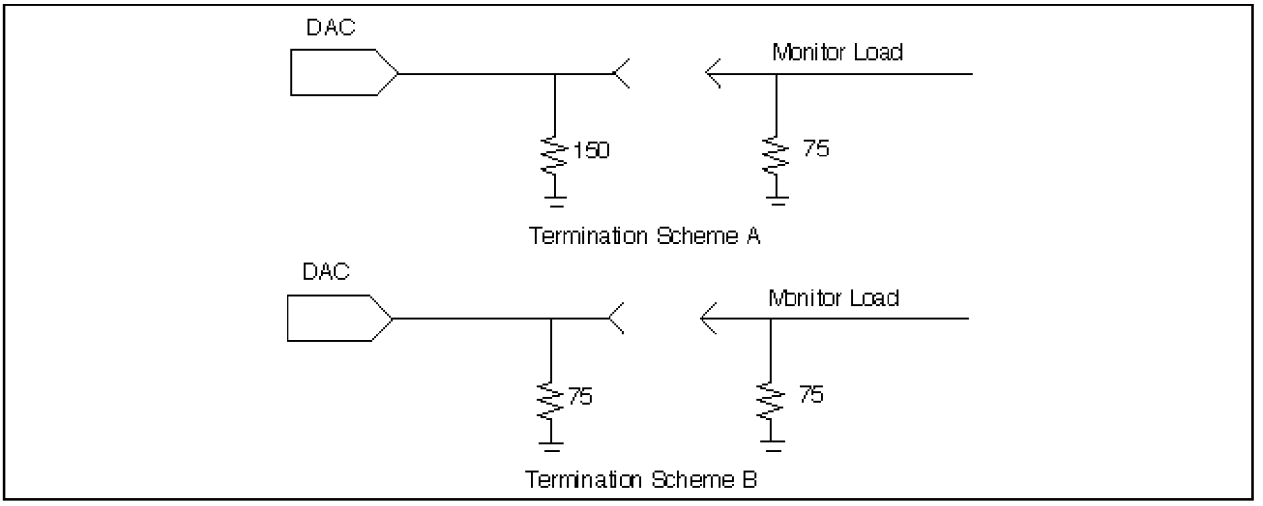


Figure 8. Examples of Monitor Termination Schemes.

Circuit Description *(continued)*

Signature Analysis Register

The Bt485A includes dedicated test registers that assist the user in evaluating the performance and functionality of the device. This section explains the operating use of these test features.

Signature Mode

The signature register, in active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color. They are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as to the three on-chip DACs.

The SARs act as a 24-bit wide linear feedback shift register. For complete test coverage the user needs to capture the signature four times by changing CR4[1:0] bits from 0, 1, 2, and 3. The Bt485A will only generate pixels while it is in "active-display" (CBLANK* negated) mode. The SARs are available for reading and writing via the MPU port when the Bt485A is in a blanking state (CBLANK* asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one scan line or one frame buffer of pixels, will be input to the chip. At the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, cursor validity is also tested with the signature registers. The above process would be repeated with all different pixel phases (A, B, C, D, etc.)

The linear feedback configuration is shown in Figure 9. Each register internally uses XORs at each input bit (D_n) with the output by 1 least significant bit (Qn-1).

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can be used as the seed for the succeeding steam to be tested.Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

Data Strobe Mode

Setting Command Register bit CR42 to "1" puts the SARs into data-strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the generation of signatures by the SARs. Instead, the SARs capture and hold the respective pixel phase that is selected.

In the data strobe mode, any MPU data written to the SARs is ignored. However, each pixel color value that is strobed into the SARs can be directly checked. To read out a captured color in the middle of a pixel stream, the user should first freeze all inputs to the Bt485A. Then, the user may read out the pixel color by doing three successive MPU reads from the read, green, and blue SAR registers, respectively.

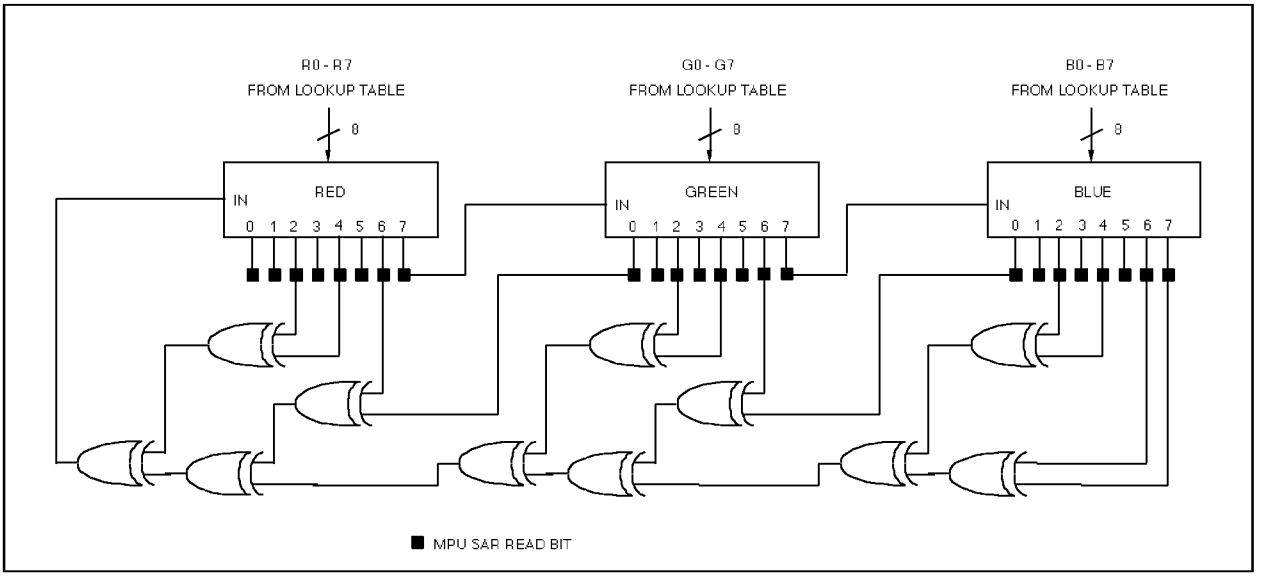
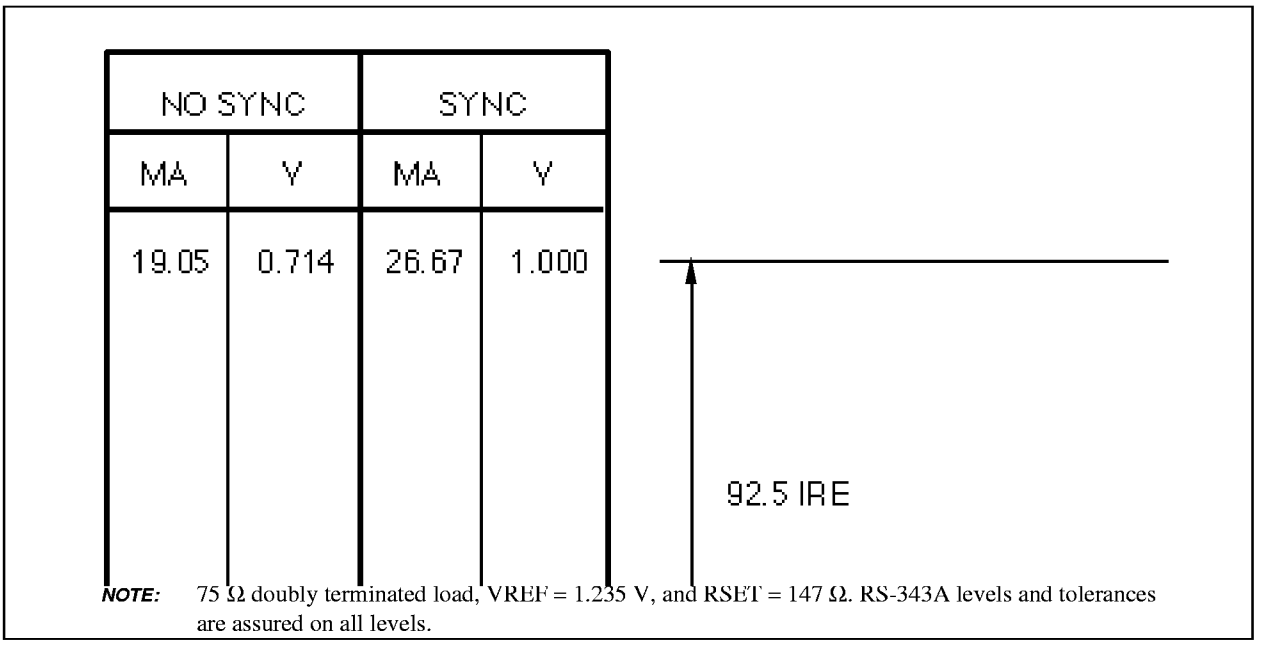


Figure 9. Signature Analysis Register Circuit.



NOTE: 75 Ω doubly terminated load, VREF = 1.235 V, and RSET = 147 Ω. RS-343A levels and tolerances are assured on all levels.

Figure 10. Composite Video Output Waveforms (SETUP = 7.5 IRE).

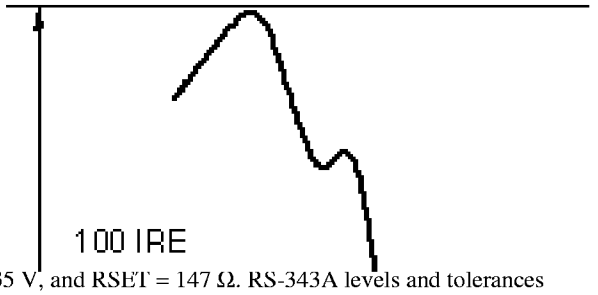
Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
White	19.05	26.67	1	1	$FF
Data	Data + 1.44	Data + 9.05	1	1	Data
Data - Sync	Data + 1.44	Data + 1.44	0	1	Data
Black	1.44	9.05	1	1	$00
Black - Sync	1.44	1.44	0	1	$00
Blank	0	7.62	1	0	$xx
Sync	0	0	0	0	$xx

NOTE: 75 Ω doubly terminated load, VREF = 1.235 V, and RSET = 147 Ω.

Table 11. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950



NOTE: 75 Ω doubly terminated load, VREF = 1.235 V, and RSET = 147 Ω. RS-343A levels and tolerances are assured on all levels.

Figure 11. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
White	17.62	25.24	1	1	$FF
Data	Data	Data + 7.62	1	1	Data
Data - Sync	Data	Data	0	1	Data
Black	0	7.62	1	1	$00
Black - Sync	0	0	0	1	$00
Blank	0	7.62	1	0	$xx
Sync	0	0	0	0	$xx

NOTE: 75 Ω doubly terminated load, VREF = 1.235 V, and RSET = 147 Ω.

Table 12. Video Output Truth Table (SETUP = 0 IRE).

Register Set

Bt485A's internal registers are programmed to enable the various functionalities of the device. Most of these registers can be addressed directly by the MPU (see Table 1). However, since the number of Register Select inputs (RS[0:3]) is limited, the extended registers must be accessed through the status register.

	Value	RS3	RS2	RS1	RS0	Extended Register
ADDR0–7 (counts binary)	0000 0000	1	0	1	0	Status Register
	0000 0001	1	0	1	0	Command Register 3
	0000 0010	1	0	1	0	Command Register 4
	0010 0000	1	0	1	0	Red Signature Analysis Register
	0010 0001	1	0	1	0	Green Signature Analysis Register
	0010 0010	1	0	1	0	Blue Signature Analysis Register

Table 12. Indirect Addressing of the Extended Register.

Please note that when RS[3:0] = 1010 and CR07 = 0, the Status Register is accessed directly and is in the read only mode. However, when RS[3:0] = 1010 and CR07 = 1, the Extended Register can be accessed (read or write) instead.

As an example, the following sequence of operations explains indirect access of Command Register 3 through the status register:

1. Set RS[3:0] = 0110 to access Command Register 0.
2. Write a logical one to Command Register bit CR07.
3. Set RS[3:0] = 0000, for Address Register write mode.
4. Write address register to 0000 0001 for Command Register 3.
5. Set RS[3:0] = 1010 for Command Register 3.
6. Read or write Command Register 3.

Internal Registers *(continued)*

Command Register 0 (RS Value = 0110)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR00 corresponds to data bus bit D[0], the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR07	(0) Extended Registers Cannot Be Addressed (1) Extended Registers Can Be Addressed	A logical one written to this bit allows the user to indirectly access the extended registers.
CR06	Clock Disable ANDed with CR00 (0) Normal Operation (1) Disable Internal Clocking	When this bit *and* CR00 are a logical one, the pixel clock is disabled to further conserve power when in power-down mode. The RAM still retains the data, and MPU reads and writes can occur without loss of data. When this bit is a logical zero, internal clocking enabled.
CR05	Setup Enable (0) Disable SETUP (0 IRE) (1) Enable SETUP (7.5 IRE)	This bit determines the video blanking pedestal. A logical zero sets a 0 IRE blanking pedestal, and a logical one sets 7.5 IRE.
CR04 CR03 CR02	Blue Sync Enable Green Sync Enable Red Sync Enable (0) Disable Sync (1) Enable Sync	These bits specify whether the respective IOB, IOG, or IOR outputs are to contain sync information. The sync currents enabled by these bits are controlled by CSYNC* input pin.
CR01	DAC 6/8-Bit Resolution (0) 6-Bit Operation (1) 8-Bit Operation	This bit specifies whether the MPU is reading and writing 8 bits (16M colors) or 6 bits (256K colors) during each cycle.
CR00	Power-Down Enable (0) Normal Operation (1) Power-Down Operation	While this bit is a logical zero, the device operates normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data, and CPU reads and writes can occur with no loss of data. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used.

Internal Registers *(continued)*

Command Register 1 (RS Value = 1000)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR10 corresponds to data bus bit D[0], the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR17	Nibble Swap Select (0) 4 Bit Per Pixel Big Endian (1) 4 Bit Per Pixel Little Endian	This bit determines whether the 4 bits/pixel mode is presented as Big Endian or Little Endian (refer to Table 4).
CR16,15	Bit/Pixel Select (00) One 24-Bit Pixel (01) One or Two 16-Bit Pixel(s) (10) Four 8-Bit Pixels (11) Eight 4-Bit Pixels	These bits select the pixel size depth and determine the multiplexing rates. The 16 bits/pixel multiplexing rate is set by the state of CR12. If bits CR36, 35 are used for selecting the MUX mode, bits CR16,15 should be set to zero.
CR14	True-Color Bypass Enable (0) Pixel Address Palette (1) Pixel Bypass Palette	When this bit is a logical zero, the color RAM is addressed by the pixel data. In this case, the value in the color RAMs may be the gamma-corrected color. When this bit is a logical one, the RGB pixel data bypasses the color palette and drives the DACs directly. True-color bypassing is available only for pixel sizes of 16 and 24 bits.
CR13	16-Bit RGB Color Format (0) 5:5:5 RGB Color Format (1) 5:6:5 RGB Color Format	This bit selects the RGB color format for 16 bits/pixel operation.
CR12	16-Bit Multiplexing Rate (0) 2:1 Multiplexing (1) 1:1 Multiplexing	When this bit is a logical zero and CR16 and 15 are set to 01, two 16-bit values are latched in during every LCLK cycle. When this bit is a logical one and CR16 and 15 are set to 01, one 16-bit value is output during every LCLK cycle. This bit is ignored if CR16/CR15 specify 4, 8, or 24-bit/pixel operation.
CR11	16-Bit Real-Time Switch Enable (0) CR10 Control Selection (non-real time) (1) P7D Control Selection (non-real time)	When this bit is a logical zero, CR10 switches the ports multiplexed. When this bit is a logical one, pixel port bit P7D switches the ports multiplexed. This bit is ignored when 5:6:5 RGB color format is selected (when bit CR13 is a logical one).
CR10	16 Bits/Pixel Port Switch Control (0) Multiplex Port [B–A] (1) Multiplex Port [D–C]	This bit specifies which 16-bit word is selected for either 5:5:5 (CR13 = 0) or 5:6:5 (CR13 = 1) modes. In order for this bit to control which 16-bit port is selected, CR12 must be a logical one (16-bit 1:1 multiplexing). This bit is ignored when real-time port switching is enabled (CR11 = 1).

Internal Registers *(continued)*

Command Register 2 (RS value = 1001)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR20 corresponds to data bus bit D[0], the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR27	SCLK Disabled (0) SCLK Enabled (1) SCLK Disabled	A logical zero must be written to this bit to enable SCLK to be output. A logical one written to this bit three-states the SCLK output.
CR26	Inverted SCLK Enable (0) Normal SCLK Output (1) Inverted SCLK Output	By setting CR26 = 1, SCLK output will be inverted; thereby placing the invalid region (where an LCLK rising edge should not occur) at a different phase of SCLK, i.e., in reference to a falling edge. The LCLK rising edges therefore, will occur outside of the invalid region (refer to Frame Buffer Clocking in the Circuit Description section).
CR25	PORTSEL Mask (0) Masked (1) Nonmasked	This bit determines the selection of the input port. It is logically ANDed with the PORTSEL pin. A logical zero selects the VGA port. When this bit is a logical one, the PORTSEL pin selects either the VGA or pixel port.
CR24	CLKSEL (0) CLK0 Selected (1) CLK1 Selected	When this bit is a logical zero, CLK0 is selected. When this bit is a logical one, CLK1 is selected. Please note that CR34 must be set to a logical zero when TTL clocks are being used. To eliminate glitches on the SCLK output, switching between CLKs should occur only when the multiplexing rate is 8:1 or 4:1. To ensure the integrity of the palette, the device should be put in sleep mode before switching clocks.
CR23	Display Mode Select (0) Noninterlaced (1) Interlaced	When this bit is a logical zero, the display format is noninterlaced. When the bit is a logical one, the display format is interlaced. The mode must be set properly to ensure proper operation of the internal cursor.
CR22	16 Bits/Pixel Palette Index Select (0) Sparse Indexing (1) Contiguous Indexing	When this bit is a logical zero, palette addressing is sparse. The RGB color component pixel data is mapped to the most significant bits of the RGB palette address. The least significant of the palette address bits are set to zero. When this bit is a logical one, palette addressing is contiguous. The RGB color component pixel data is mapped to the least significant bits of the palette address. The most significant bits of the address are set to zero.
CR21,20	Cursor Mode Select (00) Cursor Disabled (01) Three-Color Cursor (10) Two-Color/Highlight Cursor (11) Two-Color/X-Windows Cursor	These bits determine the functionality of the onboard 64 x 64 x 2 or the 32 x 32 x 2 hardware cursor.

Internal Registers *(continued)*

Command Register 3 (RS Value = 1010, Address = 0X01, Bit CR07 in Command Register 0 Set to Logical One)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR30 corresponds to data bus bit D[0], the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR37	Reserved (Logical Zero)	
CR36,35	Additional MUX Modes (00) MUX Mode Determined by Other Command Register Bits (01) 24-Bit Packed-Pixel Format 4/3:1 MUX Mode (10) Reserved (11) 8 Bits/Pixel 2:1 MUX Mode	These bits select the pixel port multiplexing modes. If bits CR15, 16, or CR12 are used for selecting the MUX mode, bits CR36, 35 should be set to zero.
CR34	Differential Clock Enable (0) Either CLK0, CLK1 or Clock Multiplier Can Be Selected (1) Differential Clock Inputs Selected	This bit enables the user to select the differential clock inputs. A logical one written to this bit enables the differential ECL clock input buffer using CLK0 and CLK1 as inputs. A logical zero written to this bit enables the user to choose between CLK0, CLK1, or the 2x multiplier. If a logical one is written to this bit, then the clock multiplier and TTL clock selections are overridden.
CR33	2x TTL Clock Multiplier (0) 2x Clock Multiplier Disabled (1) 2x Clock Multiplier Enabled	This bit enables or disables the 2x multiplier. A logical one written to this bit enables the 2x on-chip TTL clock multiplier for high-speed operation. A logical zero written to CR33 will disable the clock multiplier and will allow the external clock source to directly drive the logic.
CR32	Cursor Select (0) 32 x 32 x 2 Cursor (1) 64 x 64 x 2 Cursor	This bit selects either a 64 x 64 or a 32 x 32 hardware cursor. A logical zero written to this bit will select the 32 x 32 cursor size, and a logical one will select the 64 x 64 cursor size.
CR31,30	MSBs for 10-Bit Address Counter CR31 = A9 CR30 = A8	These bits are the load inputs to the two MSBs of the 10-bit address counter. The 10-bit address counter can be set to access any particular location in the 64 x 64 x 2 cursor RAM array.

Internal Registers *(continued)*

Command Register 4 (RS Value = 1010, Address = 0X02, Bit CR07 in Command Register 0 Set to Logical One)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR40 corresponds to data bus bit D[0], the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR47 Reserved (Logical Zero)

CR46 Reserved (Logical Zero)

CR45 Reserved (Logical Zero)

CR44 Reserved (Logical Zero)

CR43 Reserved (Logical Zero)

CR42 SAR Mode of Operation

- (0) Signature Operation
- (1) Data Strobe Testing

CR41,40 SAR Pixel Data Strobe

- (00) Pixel A
- (01) Pixel B
- (02) Pixel C
- (03) Pixel D

Internal Registers *(continued)*

Pixel Read Mask Register (RS Value = 0010)

The 8-bit pixel read mask register can be written to or read by the MPU at any time, and is not initialized at power-up. D[0] is the least significant bit. The contents of this register are bit-wise ANDed with the pixel data prior to addressing the color palette RAM. The pixel read mask register must be initialized by the user to logical ones for proper operation. (See Pixel Read Mask Register section).

Status Register (RS Value = 1010)

The 8-bit status register monitors certain device states and identifies devices. It may be read by the MPU at any time. MPU write cycles to this register are ignored. D[0] is the least significant bit corresponding to SR[0]. This register is not reset during power-up/reset.

SR7,6	Identification Bits SR7 = 0 SR6 = 0	These bits determine the type of RAMDAC being used in the system. The value is different for each RAMDAC.
SR5,4	Revision Bits SR5 = 1 SR4 = 0	These bits determine the revision of the Bt485A.
SR3	Sense* (0) CRT not present (1) CRT present	This bit is used to determine the presence of a CRT monitor. When this bit is a logical zero, one or more of IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (see SENSE* Output Description in the Pin Description section).
SR2	Read/Write Status (0) Write Operation (1) Read Operation	This bit provides RD/WR access status when the register select bits equal to $0, $3, $4, or $7. If RS[3:0] equal $0 or $4, the MPU is accessing the address register for a write operation. If RS[3:0] equal $3 or $7, the MPU is accessing the address register for a read operation.
SR1,0	ADDR [a,b] (00) Red Color Component (01) Green Color Component (10) Blue Color Component	These bits reflect the color component address for the next RD/WR cycle when the palette, cursor color registers, or overscan register is accessed.

Internal Registers *(continued)*

Red, Green, and Blue Signature Analysis Registers (RS Value = 1010, Bit CR07 in Command Register 0 Set to Logical One)

Signature Operation

These three 8-bit signature registers (one each for read, green, and blue) may be read by the MPU while CBLANK* is a logical zero. While CBLANK* is a logical one, the three registers are concatenated and a 24-bit signature is acquired. The MPU may read from or write to the signature registers while CBLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly.

Data Strobe Operation

If Command Register bit CR42 selects data strobe testing (CR42=1), the operation of the signature registers changes. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

During each LCLK cycle, the three signature registers capture the color values being presented to the DACs. Because only one of the A-D pixels can be captured during each LCLK cycle, Command Register bits CR40 and CR41 are used to specify which pixel (A-D) is to be captured.

Internal Registers *(continued)*

Cursor (x,y) Registers (RS values: CXLR = 1100, CXHR = 1101, CYLR = 1110, and CYHR = 1111)

These registers are used to specify the (x,y) coordinate of a 32 x 32 x 2 or a 64 x 64 x 2 hardware cursor. The cursor (x) register contains the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register contains the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros but are ignored internally by Bt485A.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CXHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as listed below:

For a 32 x 32 x 2 cursor — Xp = desired display screen (x) position + 32 (or $0020)
For a 64 x 64 x 2 cursor — Xp = desired display screen (x) position + 64 (or $0040)

where the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (x) register. If Xp is equal to 0, the cursor will be offscreen (see Cursor Operation in the Circuit Description section).

The cursor (y) value to be written is calculated as listed below:

For a 32 x 32 x 2 cursor — Yp = desired display screen (y) position + 32 (or $0020)
For a 64 x 64 x 2 cursor — Yp = desired display screen (y) position + 64 (or $0040)

where the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to 0, the cursor will be entirely offscreen (see Cursor Operation in the Circuit Description section).

When a 64 x 64 x 2 cursor is selected (CR32 = 1), CR31 and CR30 must be written to use a 10-bit counter to address the larger RAM array. CR31 and CR30 become the load inputs to the two MSBs of the 10-bit address counter. Therefore, to set this counter to access a particular location in the 64 x 64 x 2 cursor RAM array, these two bits must be written to Command Register 3 before the lower 8 bits are written to the address counter through the MPU port. As the 10-bit address counter auto-increments, the new values of this counter can be read back through CR31 and CR30. The contents of this register will be reset with the assertion of the external RESET* pin.

Pin Information

Pin Name	Pin Count	Description
		Video Data and Control Inputs
CBLANK*	1	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Tables 11 and 12. CBLANK* is latched on the rising edge of LCLK. When CBLANK* is a logical zero the pixel inputs are ignored. The falling edge of this signal determines the polarity of the CSYNC* input pin. The onboard cursor positioning counters are referenced to this signal.
CSYNC*	1	Composite sync control input (TTL compatible). The polarity of this pin is determined on the last rising LCLK edge before the falling edge of CBLANK*. CSYNC* does not override any other control or data input, as shown in Tables 11 and 12; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LCLK. Bits CR04–CR02 in Command Register 0 can permanently disable sync on the IOR, IOG, or IOB output.
CDE	1	Composite display enable control input (TTL compatible). The state of this signal and CBLANK* determines whether the analog outputs are blanked or contain cursor color, pixel, or overscan data. This signal is latched on the rising edge of LCLK. If overscanning is not used, this pin should be tied to CBLANK*. The following is a list of combinations of CDE and CBLANK*: PORTSEL CDE CLBANK* x x 0 Video Blanking 0 0 1 VGA Pixel Data 0 1 1 Cursor Color or VGA Data 1 0 1 Overscan Data 1 1 1 Cursor Color or Pixel Data
P[7:0] (A–D)	32	Pixel port inputs (TTL compatible). This port is selected if PORTSEL is a logical one and PORTSEL is not masked by CR25. The appropriate pins on this port are multiplexed at selected rates. The data on this port is latched on the rising edge of LCLK. P[0] is the LSB. Unused inputs should be connected to GND.
VGA[7:0]	8	VGA port inputs (TTL compatible). This port is selected if PORTSEL is a logical zero. The data on this port is multiplexed 1:1, and is latched on the rising edge of LCLK. VGA[0] is the LSB. Unused inputs should be connected to GND.
PORTSEL	1	VGA/pixel port select input (TTL compatible). This pin is ANDed with control register bit CR25 to determine whether the pixel port or VGA port is selected. A logical zero on this pin selects the VGA port regardless of the state of CR25. A logical one selects the pixel port if CR25 = 1. This pin may be used in 1:1 mode to switch between the pixel and VGA ports on a pixel-by-pixel basis. This pin may also be used to switch between the VGA and pixel ports in 2:1, 4:1 or 8:1 MUX modes on a frame-by-frame basis. This pin should not be left floating.

Pin Information *(continued)*

Pin Name	Pin Count	Description
Clocks and Clock Controls		
CLK0 (OSC)	1	Clock 0 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical zero. In VGA mode, CLK0 should be used. This clock should be specified when switching between the pixel and VGA ports on a pixel-by-pixel basis (in 1:1 mode, only). This input pin may also be used as a differential clock input pin by setting CR34 to 1. It is recommended that all clock inputs be driven by a dedicated buffer to avoid reflection-induced jitter.
CLK1 (OSC*)	1	Clock 1 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical one. This input pin may also be used as a differential clock input pin by setting CR34 to 1. The signal on this pin is typically the high-speed pixel clock used during multiplexed operation of the pixel port.
SCLK	1	VRAM shift clock output (TTL compatible). The signal on this pin is equal to the selected pixel clock divided by 8, 4, 2, or 1 depending on the operating mode selected. If 2x clock multiplier is selected (CR33 = 1), then the SCLK output is equal to either CLK0 or CLK1 divided by 4, 2, or 1, or pixel clock multiplied by 2 in 8:1, 4:1, 2:1, or 1:1 modes, respectively.
LCLK	1	Latch Clock input (TTL compatible). The rising edge of this signal latches P[7:0] (A–D) or VGA[7:0], and CBLANK*, CDE, CSYNC*, and PORTSEL. The information latched by this signal is synchronized internally with SCLK. Because of this synchronization process, there is a timing window on both sides of SCLK where LCLK must not rise (see AC Characteristics section). This timing window is necessary so that data latched by LCLK does not interfere with the setup and hold times required by the internal synchronizing latch. Data is synchronized with the selected pixel clock after being internally latched with SCLK. When the multiplexing rate is 8:1, 4:1, 2:1, or 1:1, this signal is equal to the selected pixel clock divided by 8, 4, 2, or 1, respectively.
Video Outputs		
IOR,IOG,IOB	3	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly terminated 75 Ω coaxial cable. The PC Board Layout Considerations section contains further information.

Pin Information *(continued)*

<table>
<tr><th>Pin Name</th><th>Pin Count</th><th>Description</th></tr>
<tr><td colspan="3">DAC Support</td></tr>
<tr><td>FSADJ</td><td>1</td><td>Full-scale adjust control. The IRE relationships in Figures 10 and 11 are maintained, regardless of the full-scale output current.

When an external voltage reference (Figure 13 in the PC Board Layout Considerations section) is used, a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

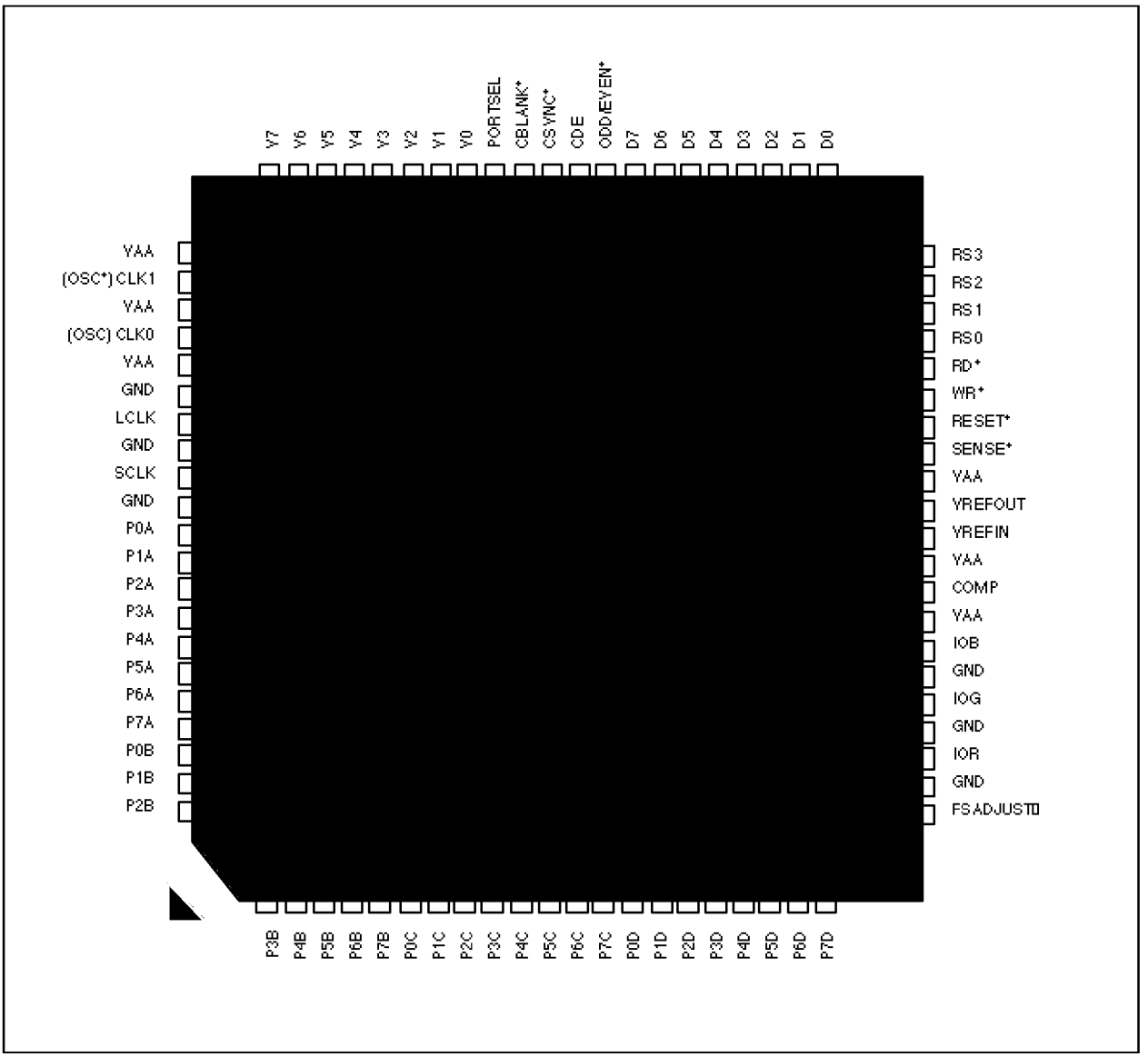
K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly terminated 75 Ω loads (i.e., RS-343A applications).

<table>
<tr><th></th><th colspan="2">Sync Enabled</th><th colspan="2">Sync Disabled</th></tr>
<tr><th>Setup</th><td>0 IRE</td><td>7.5 IRE</td><td>0 IRE</td><td>7.5 IRE</td></tr>
<tr><th>K (8 bits)</th><td>3.058</td><td>3.226</td><td>2.145</td><td>2.314</td></tr>
<tr><th>K (6 bits)</th><td>3.012</td><td>3.178</td><td>2.113</td><td>2.279</td></tr>
</table>
</td></tr>
<tr><td>VREF OUT</td><td>1</td><td>Voltage reference Output. This output provides an internal voltage reference and may be connected directly to VREF IN Pin. If the on-chip reference is not used, this pin may be left floating (see Figure 12). Up to four 485As can be driven by this output.</td></tr>
<tr><td>VREF IN</td><td>1</td><td>Voltage reference input. If an external voltage reference is used (Figure 13), it must supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry except the decoupling capacitor.</td></tr>
<tr><td colspan="3">Microprocessor Interface</td></tr>
<tr><td>WR*</td><td>1</td><td>Write control input (TTL compatible). D[0:7] data is latched on the rising edge of WR*, and RS[0:3] are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.</td></tr>
<tr><td>RD*</td><td>1</td><td>Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS[0:3] are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.</td></tr>
<tr><td>RS[0:3]</td><td>4</td><td>Register select inputs (TTL compatible). RS[0:3] specify the type of read or write operation being performed, as shown in Tables 1 and 2.</td></tr>
</table>

Pin Information *(continued)*

Pin Name	Pin Count	Description
D[0:7]	8	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D[0] is the least significant bit.
Misc.		
RESET*	1	Reset input (TTL compatible). When this signal is low, all command register bits are set to zero, and the device is in VGA mode. The pixel read mask register is not initialized on reset and must be initialized by the user to logical ones for proper operation (see Pixel Read Mask Register in the Circuit Description section).
ODD/EVEN*	1	Odd/even field input (TTL compatible). This signal should be changed only during vertical blank. This input is used to ensure proper operation of the onboard cursor when interlaced operation (command bit CR23=1) is selected. When this signal is a logical zero, an even field is specified. When this signal is a logical one, an odd field is specified. This input is ignored if noninterlaced operation (command bit CR23=0) is selected.
SENSE*	1	Comparator sense output (CMOS compatible). This pin will be low if one or more of the IOR, IOG, and IOB analog output levels exceed the internal comparator reference levels. The sense output can drive only one CMOS load.
COMP	1	Compensation pin. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
Power and Ground		
VAA	6	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	6	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.

Pin Information *(continued)*



Pin Information *(continued)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
CBLANK*	65	V[0]	67	RESET*	47
CSYNC*	64	V[1]	68		
CDE	63	V[2]	69	ODD/EVEN*	62
		V[3]	70		
P0A	1	V[4]	71	SENSE*	46
P1A	2	V[5]	72		
P2A	3	V[6]	73	COMP	41
P3A	4	V[7]	74		
P4A	5			VAA	40, 42, 45, 75, 77,
P5A	6	PORTSEL	66		79
P6A	7				
P7A	8	CLK0 (OSC)	78	GND	34,36,38,80,82,84
		CLK1 (OSC*)	76		
P0B	9	SCLK	83		
P1B	10	LCLK	81		
P2B	11				
P3B	12	IOR	35		
P4B	13	IOG	37		
P5B	14	IOB	39		
P6B	15				
P7B	16	VREFIN	43		
		VREFOUT	44		
P0C	17				
P1C	18	FSADJ	33		
P2C	19				
P3C	20	WR*	48		
P4C	21	RD*	49		
P5C	22				
P6C	23	RS[0]	50		
P7C	24	RS[1]	51		
		RS[2]	52		
P0D	25	RS[3]	53		
P1D	26				
P2D	27	D[0]	54		
P3D	28	D[1]	55		
P4D	29	D[2]	56		
P5D	30	D[3]	57		
P6D	31	D[4]	58		
P7D	32	D[5]	59		
		D[6]	60		
		D[7]	61		

PC Board Layout

PC Board Considerations

For optimum performance of the Bt485A, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun.

The layout should be optimized for lowest noise on the Bt485A power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt485A to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all analog power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 12 and 13. This bead should be located within 3 inches of the Bt485A. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 12 and 13 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

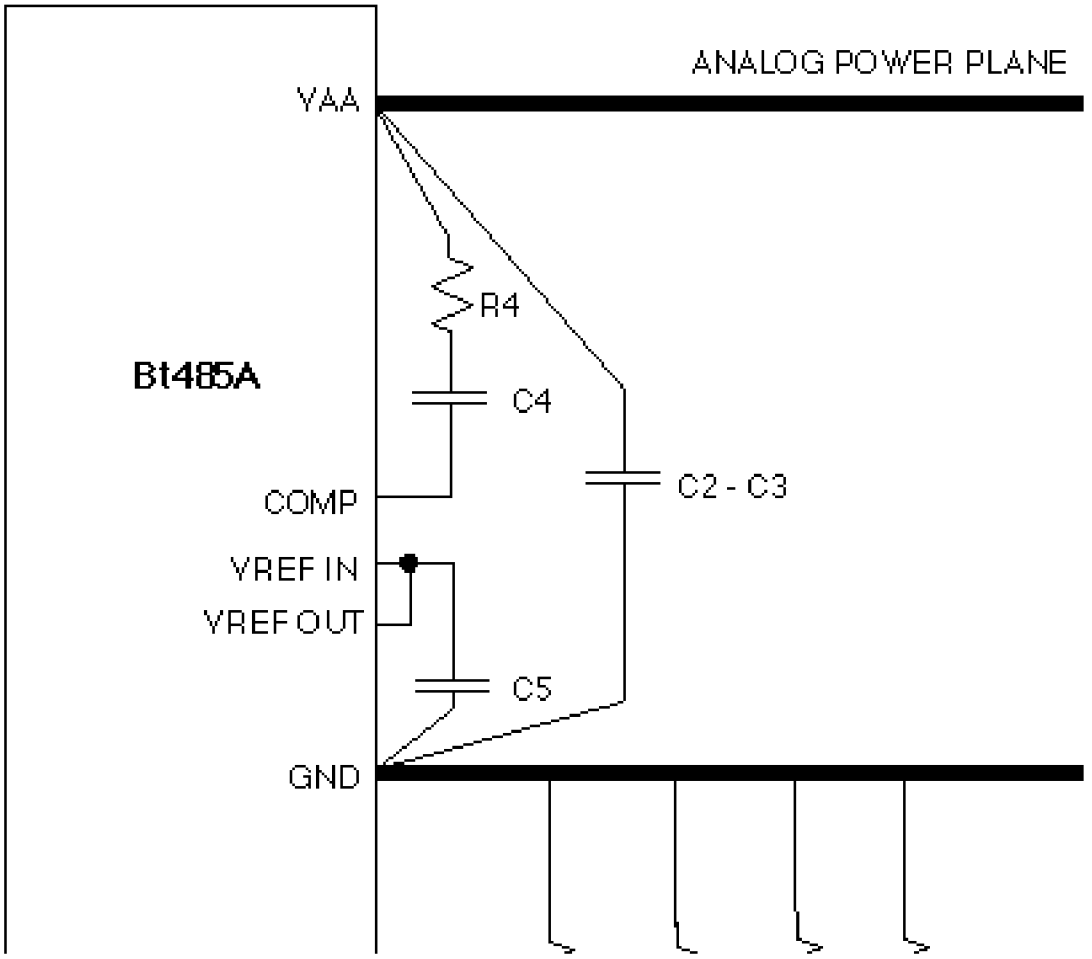
The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout *(continued)*



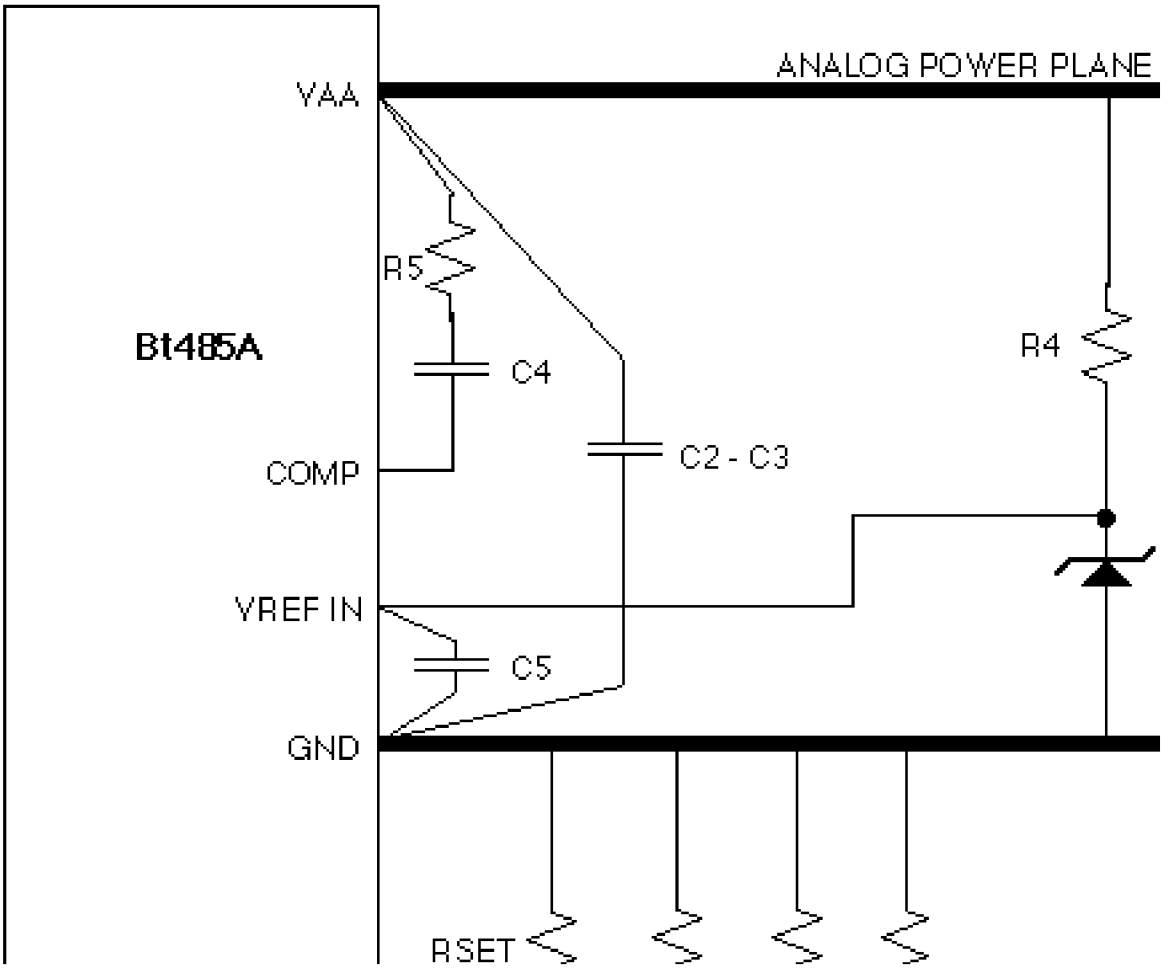
NOTE: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	TDK BF45-4001
R1–R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	1% Metal Film Resistor	Dale CMF-55C
R4	15 Ω 1% Metal Film Resistor	Dale CMF-55C

NOTE: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt485A.

Figure 12. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout *(continued)*



NOTE: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	TDK BF45-4001
R1–R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
R4	1 kΩ 5% Resistor	
RSET	147 Ω 1% Metal Film Resistor	Dale CMF-55C
Z1	1.2 V Voltage Reference	National Semiconductor LM385BZ-1.2
R5	15 Ω 1% Metal Film Resistor	Dale CMF-55C

NOTE: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt485A.

Figure 13. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt485A should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one-fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90° angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

TTL Clock Interfacing

The Bt485A requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

Differential Clock Interfacing

Termination requirements for differential ECL clock sources will vary depending on the particular clock generator used. Illustrated in Figure 14 are two examples with termination schemes recommended by the vendors.

MPU Control Signal Interfacing

The Bt485A uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

PC Board Layout *(continued)*

Analog Signal Interconnect

The Bt485A should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt485A to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt485A analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot switching AC-coupled monitors.

The diode protection circuit shown in Figures 12 and 13 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout *(continued)*

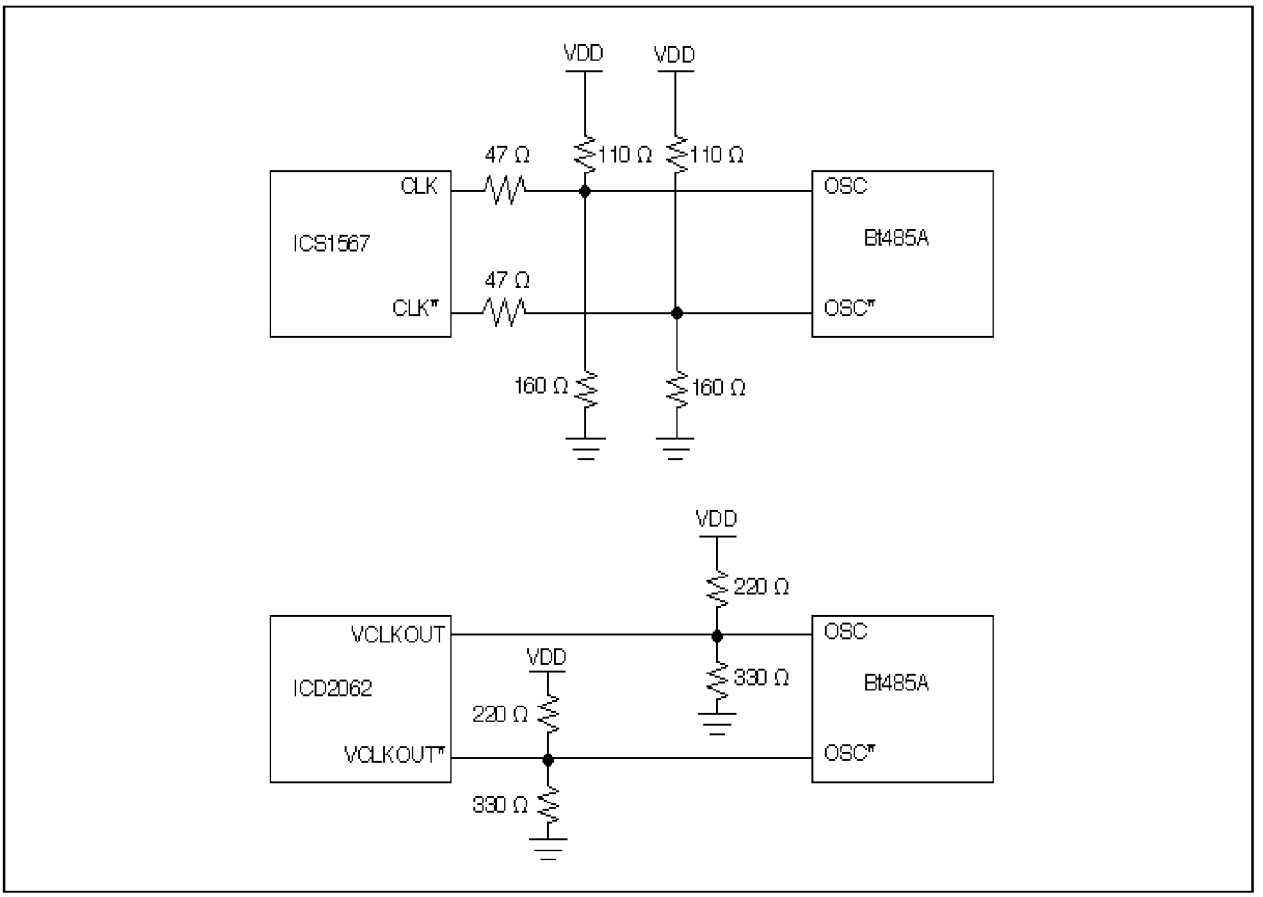


Figure 14. Differential Clock Input Interface.

Application Information

Using Multiple Devices

When multiple Bt485As are used, each Bt485A should have its own power plane ferrite bead. If the internal reference is used, each Bt485A should use its own internal reference.

Although the multiple Bt485As may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt485A must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about 10 times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

Electrical Specifications

Recommended Operating Conditions

Parameter	Symbol	MIN	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
DAC Output Load	RL		37.5		Ω
Voltage Reference Input	VREF IN		1.235		V

Absolute Maximum Ratings

Parameter	Symbol	MIN	Typ	Max	Units
VAA (measured GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		Indefinite		
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Tjx is measured with devices surface mounted on a four layer board, 1 ounce copper plating, at 0 air flow. Tjx = 20.6°C/w (KHJ Package) and 34.2 °C/w (KPJ Package).

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Electrical Specifications *(continued)*

DC Characteristics

Parameter	Symbol	MIN	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	%Gray Scale
Monotonicity			Guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND-0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Clock Inputs (OSC, OSC*)					
Differential Input Voltage (VIN = 4.0 V)	ΔVIN	0.6			V
Input High Voltage	VIH			VDD-0.8	V
Input Low Voltage	VIL	VDD-3			V
Input High Current (VIN = 4.0 V)	IKIH			1	µA
Input Low Current (VIN = 0.8 V)	IKIL			–1	µA
Input Capacitance (f=1 MHz, VIN = 4.0 V)	CKIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
SCLK Output High Voltage (IOH = –10 mA)		2.4			V
SCLK Output Low Voltage (IOL = +10 mA)				0.4	V
Three-state Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

Electrical Specifications *(continued)*

DC Characteristics (continued)

Parameter	Symbol	MIN	Typ	Max	Units
Analog Outputs					
Gray-Scale Current Range				20	mA
Output Current (Standard RS-343A) (Note 1)					
White Level Relative to Black					
Using Internal V ref, Rset = 147Ω		16.74	17.62	18.50	mA
Using External V ref, Rset = 147Ω		17.24	17.87	18.50	mA
Using External V ref, Rset = 149Ω		16.99	17.62	18.25	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance		–0.2		+1.5	V
Output Impedance	VOC		10		kΩ
Output Capacitance	RAOUT			30	pF
(f = 1 MHz, IOUT = 0 mA)	CAOUT				
Voltage Reference Input Current	IVREFIN		0.5		mA
Power Supply rejection Ratio (Note 2) (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, RSET = 147 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

NOTE 1: When the Bt485A is in the 6-bit mode, the output levels are approximately 1.5 percent lower than these values.

NOTE 2: Guaranteed by characterization, not tested.

Electrical Specifications *(continued)*

AC Characteristics

Parameter	Symbol	170 MHz Devices Min	170 MHz Devices Typ	170 MHz Devices Max	150 MHz Devices Min	150 MHz Devices Typ	150 MHz Devices Max	Units
CLK 0, CLK 1 (Note 1)	Fmax							
2 x TTL Clock Multiplier Not Activated								
2:1, 4:1, 8:1 MUX Modes				110			110	MHz
1:1 MUX or VGA				110			110	MHz
4/3:1 MUX Packed Pixel				85			85	MHz
2 x TTL Clock Multiplier Activated								
8:1 MUX				85			75	MHz
4:1 MUX				85			75	MHz
2:1 MUX				67.5			67.5	MHz
OSC, OSC* All MUX Modes (Note 1)				170			150	MHz
RS[0:3] Setup Time (Figure 15)	1	10			10			ns
RS[0:3] Hold Time	2	10			10			ns
RD* Asserted to D[0:7] Driven	3	2			2			ns
RD* Asserted to D[0:7] Valid	4			40			40	ns
RD* Negated to D[0:7] Three-Stated	5			20			20	ns
Read D[0:7] Hold Time	6	2			2			ns
Write D[0:7] Setup Time	7	10			10			ns
Write D[0:7] Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			
RD*, WR* Pulse Width High	10	6*PCLK			6*PCLK			
LCLK Rates	Lmax							
8:1 Multiplexing				21.3			18.7	MHz
4:1 Multiplexing				42.5			37.5	MHz
2:1 Multiplexing				67.5			67.5	MHz
4/3:1 Multiplexing 24-bit mode (Note 1)				85			85	MHz
1:1 Multiplexing or VGA (Note 1)				110			110	MHz
SCLK Rate	Smax							
8:1 Multiplexing				21.3			18.7	MHz
4:1 Multiplexing				42.5			37.5	MHz
2:1 Multiplexing				67.5			67.5	MHz
4/3:1 Multiplexing 24-bit Mode (Note 1)				85			85	MHz
1:1 Multiplexing or VGA (Note 1)				110			110	MHz
OSC, OSC* Cycle Time (Note 1) All MUX Rates		5.9			6.6			ns

Electrical Specifications *(continued)*

AC Characteristics (continued)

Parameter	Symbol	170 MHz Devices Min	170 MHz Devices Typ	170 MHz Devices Max	150 MHz Devices Min	150 MHz Devices Typ	150 MHz Devices Max	Units
CLK 0, CLK 1 Cycle Time (Note 1)	11							
2 x TTL Clock Multiplier Not Activated								
2:1, 4:1, 8:1 MUX Modes		9.1			9.1			ns
1:1 MUX or VGA		9.1			9.1			ns
4/3:1 MUX Packed Pixel		11.8			11.8			ns
2 x TTL Clock Multiplier Activated								
8:1 MUX		11.8			13.3			ns
4:1 MUX		11.8			13.3			ns
2:1 MUX		14.8			14.8			ns
Duty Cycle x 2 TTL Clock Multiplier	12	44		52	44		52	%
(if activated)	13	48		56	48		56	%
LCLK Cycle Time	14							
8:1 Multiplexing		47.1			53.4			ns
4:1 Multiplexing		23.5			26.7			ns
2:1 Multiplexing		14.8			14.8			ns
4/3:1 Multiplexing 24-bit Mode (Note 1)		11.8			11.8			ns
1:1 Multiplexing or VGA (Note 1)		9.1			9.1			ns
LCLK Pulse Width High	15	4			4			ns
All Modes								
LCLK Pulse Width Low	16	4			4			ns
All Modes								
SCLK Cycle Time	17							
8:1 Multiplexing		47.1			53.4			ns
4:1 Multiplexing		23.5			26.7			ns
2:1 Multiplexing		14.8			14.8			ns
4/3:1 Multiplexing 24-bit mode (Note 1)		11.8			11.8			ns
1:1 Multiplexing or VGA (Note 1)		9.1			9.1			ns
Data Setup to LCLK	18	1			1			ns
P[7:0] (A–D)								
Data Hold from LCLK	19	5			5			ns
P[7:0] (A–D)								
Data Setup and Hold to LCLK	20	3			3			ns
VGA[7:0], CDE, CBLANK*								
CSYNC*, PORTSEL								
LCLK Valid Skew with Respect to SCLK	21							
(Note 2)								
2:1, 4:1, 8:1 MUX Modes		–1		T-8	–1		T-8	ns
4/3:1 Multiplexing 24-bit Mode		0		T-7	0		T-7	ns

Electrical Specifications *(continued)*

AC Characteristics (continued)

Parameter	Symbol	170 MHz Devices			150 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
SCLK Output Delay (1:1 mode)	22		6	9		6	9	ns
SCLK Output Delay (MUX mode)			10	15		10	15	ns
Analog Output Delay				30			30	ns
Analog Output Rise/Fall Time	23		3			3		ns
Analog Output Settling Time (Note 3)	24		13			13		ns
Clock and Data Feedthrough (Note 3)	25		–30			–30		dB
Glitch Impulse (Note 3)			75			75		pV- sec
SENSE* Output Delay	26		1			1		µs
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
VAA Supply Current (Note 4)	IAA							
Normal Operation			460	500		435	480	mA
Sleep Mode (Note 5)				5			5	mA

Electrical Specifications *(continued)*

AC Characteristics (continued)

Parameter	Symbol	135 MHz Devices Min	135 MHz Devices Typ	135 MHz Devices Max	110 MHz Devices Min	110 MHz Devices Typ	110 MHz Devices Max	Units
CLK 0, CLK 1 (Note 1)	Fmax							
2 x TTL Clock Multiplier Not Activated								
2:1, 4:1, 8:1 MUX Modes				110			110	MHz
1:1 MUX or VGA				110			110	MHz
4/3:1 MUX Packed Pixel				85			85	MHz
2 x TTL Clock Multiplier Activated								MHz
8:1 MUX				67.5			55	MHz
4:1 MUX				67.5			55	MHz
2:1 MUX				67.5			55	MHz
OSC, OSC* All MUX Modes (Note 1)				135			110	MHz
RS[0:3] Setup Time (Figure 15)	1	10			10			ns
RS[0:3] Hold Time	2	10			10			ns
RD* Asserted to D[0:7] Driven	3	2			2			ns
RD* Asserted to D[0:7] Valid	4			40			40	ns
RD* Negated to D[0:7] Three Stated	5			20			20	ns
Read D[0:7] Hold Time	6	2			2			ns
Write D[0:7] Setup Time	7	10			10			ns
Write D[0:7] Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*PCLK			6*PCLK			
LCLK Rates	Lmax							
8:1 Multiplexing				16.9			13.8	MHz
4:1 Multiplexing				33.8			27.5	MHz
2:1 Multiplexing				67.5			55	MHz
4/3:1 Multiplexing 24-bit Mode (Note 1)				85			85	MHz
1:1 Multiplexing or VGA				110			110	MHz
SCLK Rate	Smax							
8:1 Multiplexing				16.9			13.8	MHz
4:1 Multiplexing				33.8			27.5	MHz
2:1 Multiplexing				67.5			55	MHz
4/3:1 Multiplexing 24-bit Mode (Note 1)				85			85	MHz
1:1 Multiplexing or VGA (Note 1)				110			110	MHz

Electrical Specifications *(continued)*

AC Characteristics (continued)

Parameter	Symbol	135 MHz Devices Min	135 MHz Devices Typ	135 MHz Devices Max	110 MHz Devices Min	110 MHz Devices Typ	110 MHz Devices Max	Units
CLK 0, CLK 1 Cycle Time (Note 1)	11							
2 x TTL Clock Multiplier Not Activated								
2:1, 4:1, 8:1 MUX Modes		9.1			9.1			ns
1:1 MUX or VGA		9.1			9.1			ns
4/3:1 MUX Packed Pixel		11.8			11.8			ns
2 x TTL Clock Multiplier Activated								
8:1 MUX		14.8			18.2			ns
4:1 MUX		14.8			18.2			ns
2:1 MUX		14.8			18.2			ns
Duty Cycle 2 x TTL Clock Multiplier (if activated)	12,13	45		55	40		60	%
LCLK Cycle Time	14							
8:1 Multiplexing		59.2			72.5			ns
4:1 Multiplexing		29.6			36.4			ns
2:1 Multiplexing		14.8			18.2			ns
4/3:1 Multiplexing 24-bit Mode (Note 1)		11.8			11.8			ns
1:1 Multiplexing or VGA (Note 1)		9.1			9.1			ns
LCLK Pulse Width High	15	4			4			ns
All modes								
LCLK Pulse Width Low	16	4			4			ns
All modes								
SCLK Cycle Time	17							
8:1 Multiplexing		59.2			72.5			ns
4:1 Multiplexing		29.6			36.4			ns
2:1 Multiplexing		14.8			18.2			ns
4/3:1 Multiplexing 24-bit Mode (Note 1)		11.8			11.8			ns
1:1 Multiplexing or VGA (Note 1)		9.1			9.1			ns
Data Setup to LCLK P[7:0] (A–D)	18	1			1			ns
Data Hold from LCLK P[7:0] (A–D)	19	5			5			ns
Data Setup and Hold to LCLK VGA[7:0], CDE, CBLANK* CSYNC*, PORTSEL	20	3			3			ns
LCLK Valid Skew with Respect to SCLK (Note 2)	21							
2:1, 4:1, 8:1 MUX Modes		–1		T-8	–1		T-8	ns
4/3:1 Multiplexing 24-bit Mode		0		T-7	0		T-7	ns

Electrical Specifications *(continued)*

AC Characteristics (continued)

Parameter	Symbol	135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
SCLK Output Delay (1:1 mode)	22		6	9		6	9	ns
SCLK Output Delay (MUX mode)			10	15		10	15	ns
Analog Output Delay				30			30	ns
Analog Output Rise/Fall Time	23		3			3		ns
Analog Output Settling Time (Note 3)	24		13			13		ns
Clock and Data Feedthrough (Note 3)	25		–30			–30		ns
Glitch Impulse (Note 3)			75			75		pV-
SENSE* Output Delay	26		1			1		sec
DAC-to-DAC Crosstalk			–23			–23		µs
Analog Output Skew				2			2	dB
								ns
VAA Supply Current (Note 4)	IAA							
Normal Operation			360	390		330	360	mA
Sleep Mode (Note 5)				5			5	mA

Electrical Specifications *(continued)*

Pipeline Delay	MIN	MAX
1:1/VGA Mode	9 LCLKs	9 LCLKs
2:1 Mode (15/16 bpp)	1 LCLK + 8 PCLKs	1 LCLK + 9 PCLKs
2:1 Mode (8 bpp)	1 LCLK + 8 PCLKs	1 LCLK + 9 PCLKs
4:1 Mode (8 bpp)	1 LCLK + 8 PCLKs	1 LCLK + 11 PCLKs
8:1 Mode (4 bpp)	1 LCLK + 8 PCLKs	1 LCLK + 15 PCLKs
4/3:1 24-bit Mode	1 LCLK + 8 PCLKs	1 LCLK + 11 PCLKs (Note 6)

Pipeline delay (MIN) is the minimum number of clocks required to output 1 pixel after all pixels have been latched. Pipeline delay (MAX) is the maximum number of clocks required to output all pixels after all pixels have been latched. In the 1:1/VGA modes, LCLK is the primary clock latching and pipelining for the pixels.

Test conditions unless otherwise specified: "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 147 Ω. TTL input values are 0–3 V with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF; SENSE* and D0–D7 output load ≤50 pF. SCLK output load = 25 pF. See timing notes in Figures 15–18. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

NOTE 1: To pipeline data above 110 MHz, the 2x clock multiplier or differential ECL clock inputs must be activated. ECL clock inputs are recommended for operation above 135 MHz.

NOTE 2: T = SCLK cycle time.

NOTE 3: Clock and data feedthrough are a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

NOTE 4: IAA (typ) at VAA = 5.0 V, 25°C. IAA (max) at VAA = 5.25 V, 0° C.

NOTE 5: External voltage reference is disabled during sleep mode, all inputs are low, and clock is held high.

NOTE 6: In the 4/3:1 Packed Pixel mode, 4 24-bit pixels are piped within 3 load clock cycles. Therefore, the maximum pipeline delay as specified is for 4 24-bit pixels.

Timing Waveforms

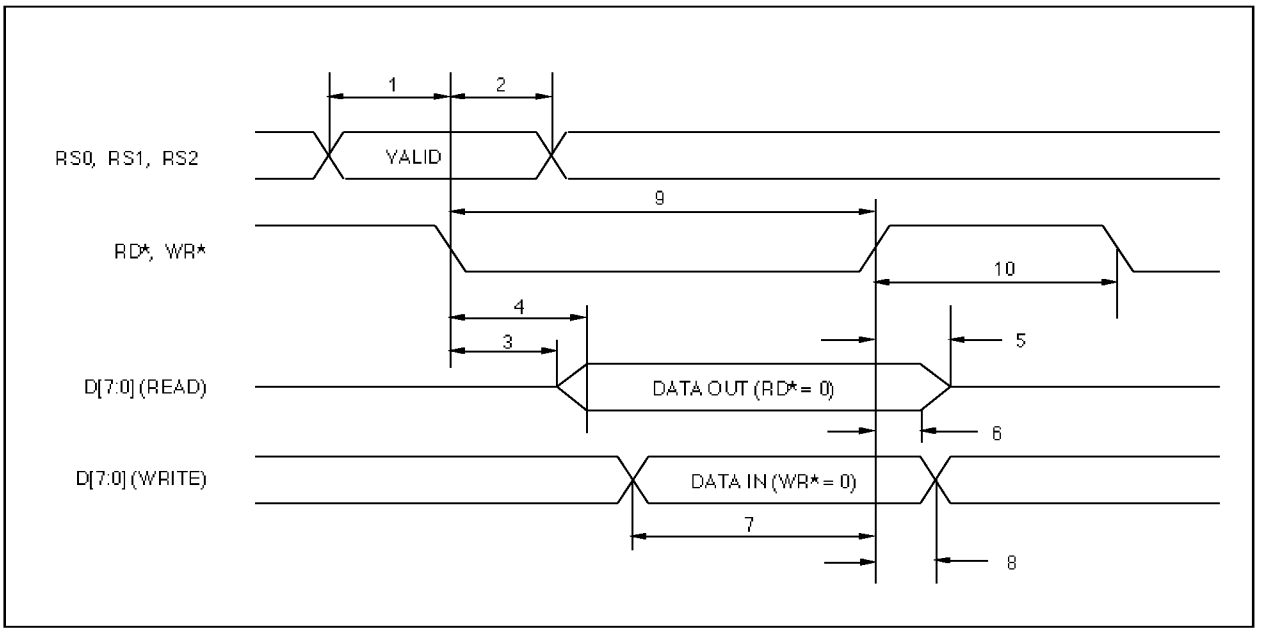
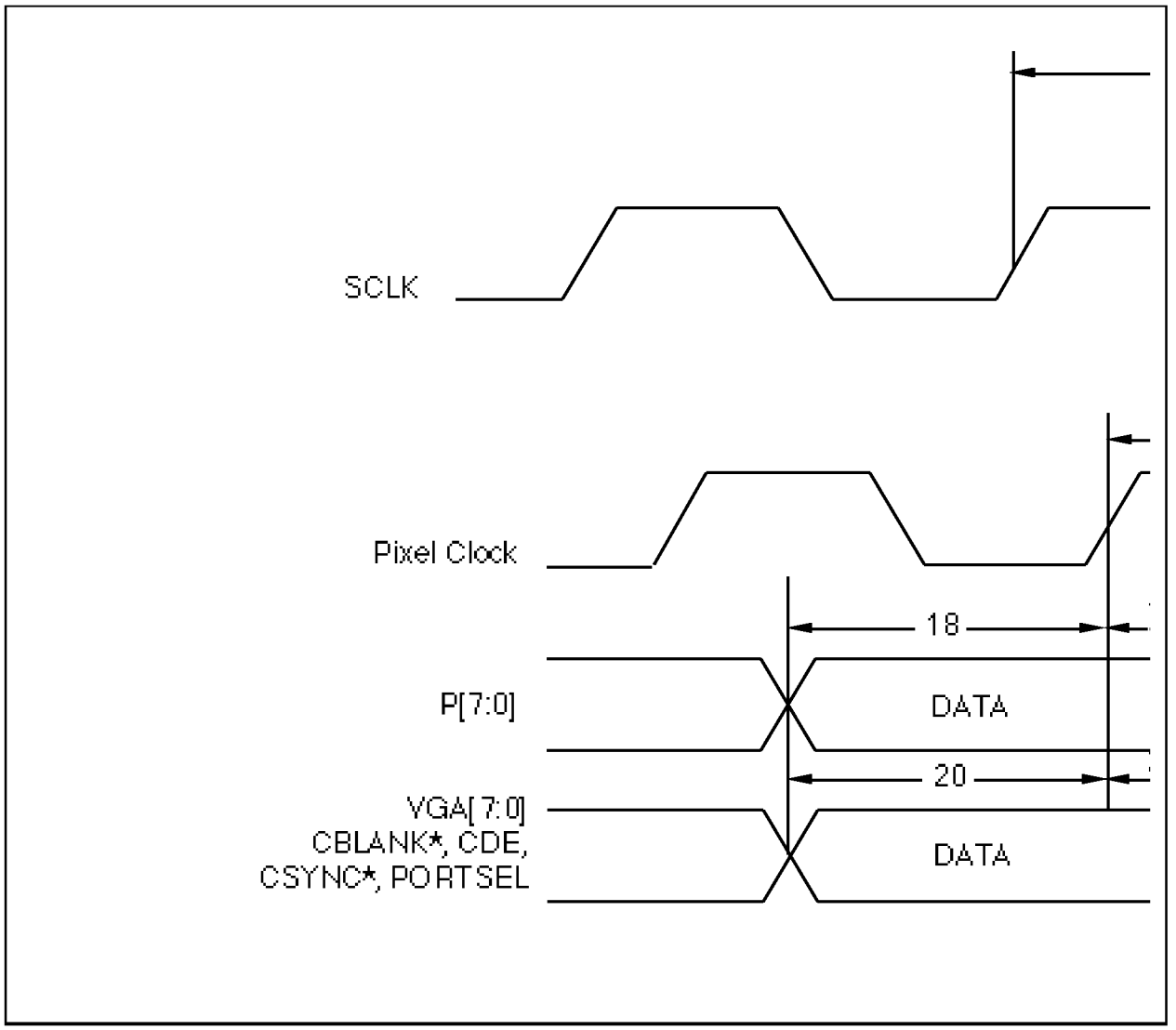


Figure 15. MPU Read/Write Timing.

Timing Waveforms *(continued)*



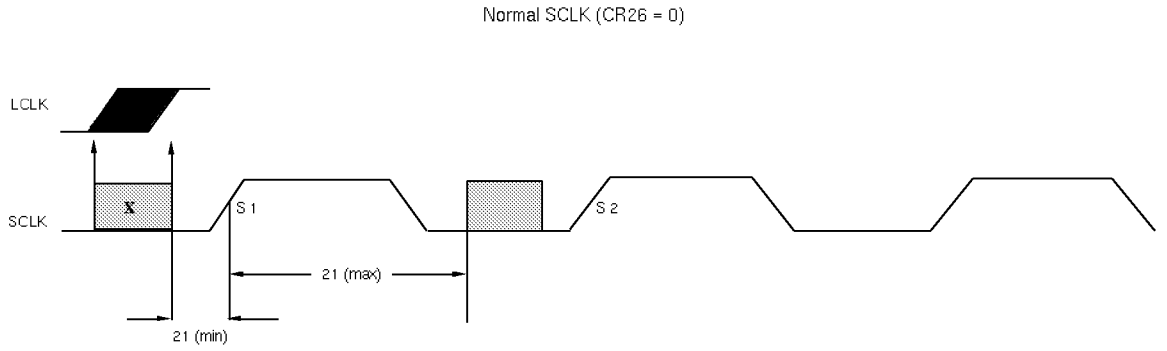
NOTE 1: Output delay is measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

NOTE 2: Settling time is measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

NOTE 3: Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

Figure 16. Video Input/Output Timing (Non-1:1).

Timing Waveforms *(continued)*



L = LCLK rising edges
S1 = First SCLK rising edge
S2 = Second SK rising edge

In order for the pixel data latched by LCLK to be synchronized correctly with the internal pixel clock, an LCLK rising edge cannot occur in an invalid window, as illustrated above.

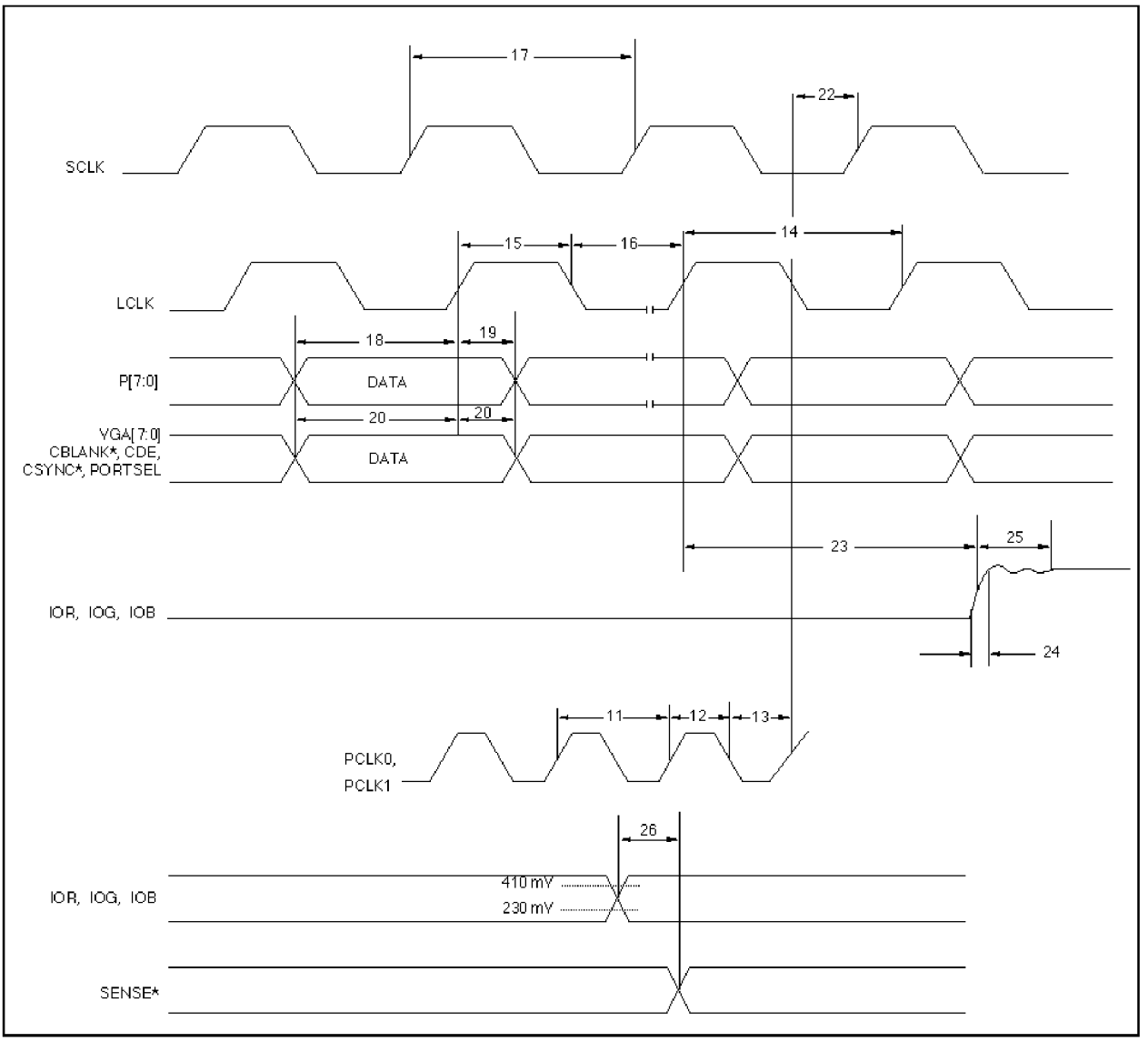
If L occurs within the invalid region (X), it is not guaranteed on which rising edge of SCLK (S1 or S2) the data will be synchronized. If L occurs before the invalid region (X), then the data is guaranteed to by synchronized on S1. If L occurs after the invalid region (X), then the data will not be synchronized on S1 and is guaranteed to be synchronized on S2.

Inverted SC

LCLK valid skew with respect to SCLK is referenced to an SCLK falling edge when SK is inverted through setting CR26 = 1.

Figure 17. SCLK to LCLK Timing (Non-1:1).

Timing Waveforms *(continued)*



NOTE 1: Output delay is measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

NOTE 2: Settling time is measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

NOTE 3: Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

Figure 18. Video Input/Output Timing (1:1 MUX Rates).

Ordering/Revision History

Ordering Information

Model Number	Speed (MHz)	Package	Ambient Temperature Range
Bt485AKHJ170	170 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt485AKHJ150	150 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt485AKPJ135	135 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt485AKPJ110	110 MHz	84-Pin Plastic J-Lead	0° to +70° C

Revision History

Revision	Change from Previous Revision
A	Initial Release.
B	Incorporated characterization information to bring datasheet to Final status.