

To all our customers

---

## **Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.**

---

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

## Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

---

# HM62V16256CBP Series

4 M SRAM (256-kword × 16-bit)



ADE-203-1259 (Z)  
Preliminary  
Rev. 0.0  
Mar. 21, 2001

---

## Description

The Hitachi HM62V16256CBP Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62V16256CBP Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48 bumps chip size package with 0.75 mm bump pitch for high density surface mounting.

## Features

- Single 2.5 V and 3.0 V supply: 2.2 V to 3.6 V
- Fast access time: 55 ns/70 ns (max)
- Power dissipation:
  - Active: 5.0 mW/MHz (typ)( $V_{CC} = 2.5$  V)  
: 6.0 mW/MHz (typ) ( $V_{CC} = 3.0$  V)
  - Standby: 2  $\mu$ W (typ) ( $V_{CC} = 2.5$  V)  
: 2.4  $\mu$ W (typ) ( $V_{CC} = 3.0$  V)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup

Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

---

## HM62V16256CBP Series

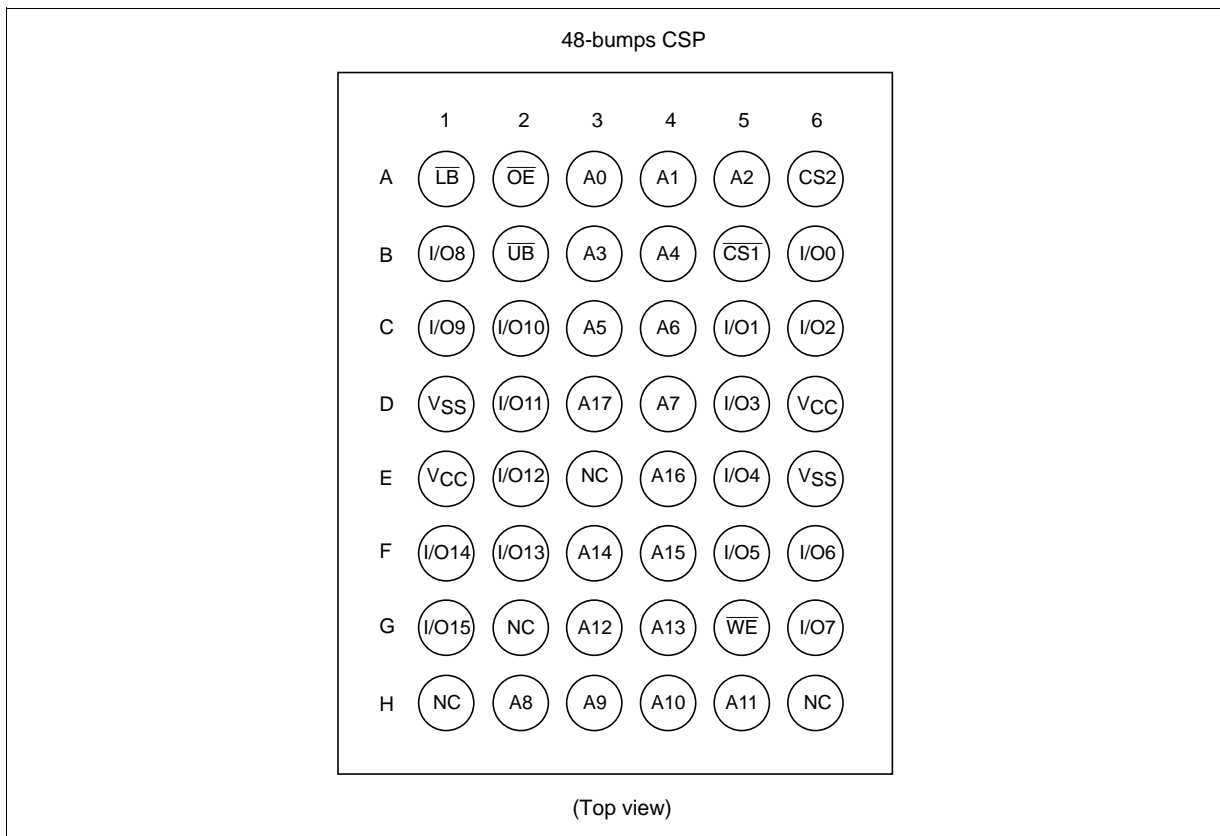
---

### Ordering Information

Type No.	Access time	Package
HM62V16256CLBP-5	55 ns	48-bumps CSP with 0.75 mm bump pitch (TBP-48)
HM62V16256CLBP-7	70 ns	
HM62V16256CLBP-5SL	55 ns	
HM62V16256CLBP-7SL	70 ns	

---

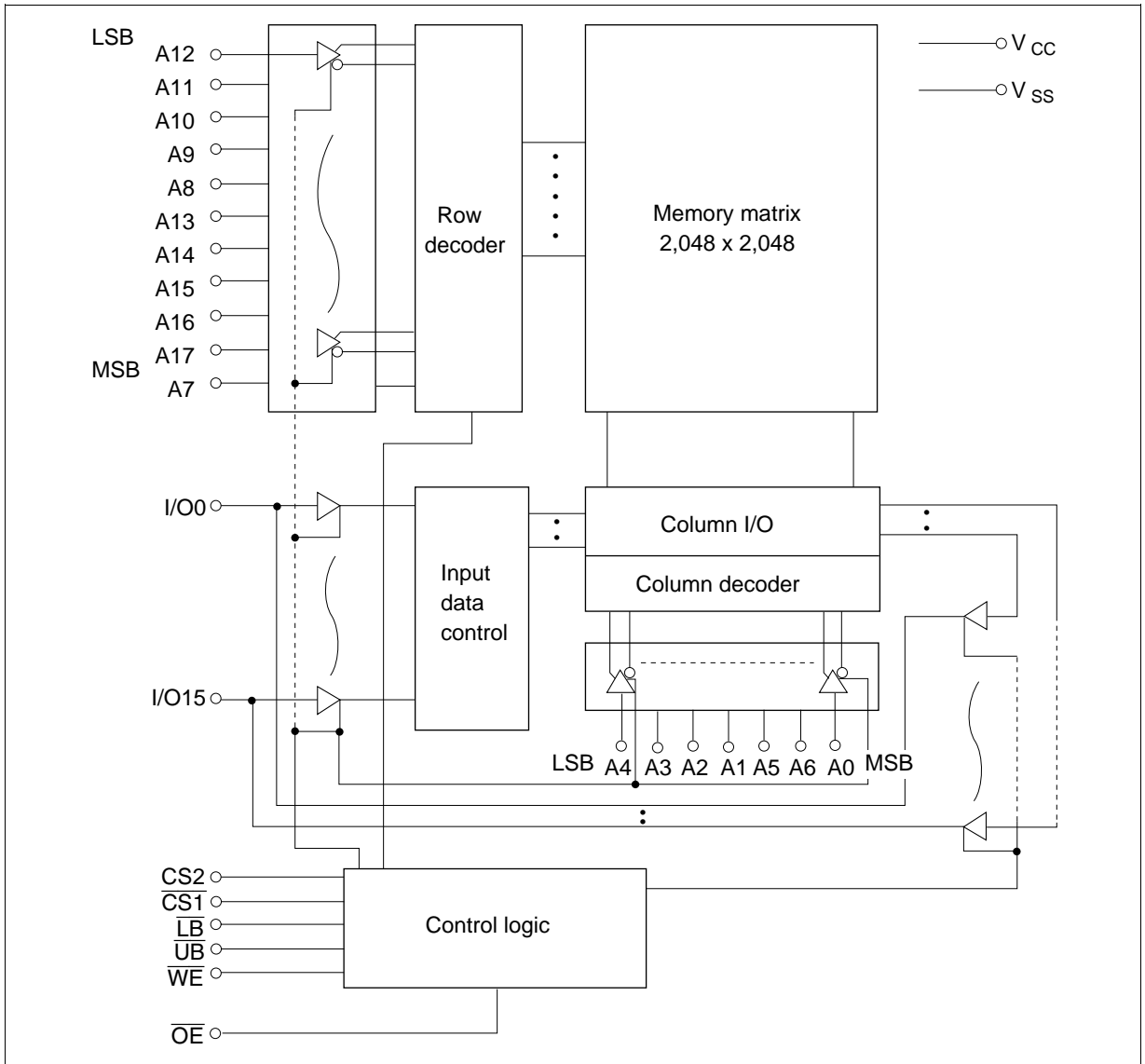
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
$V_{CC}$	Power supply
$V_{SS}$	Ground
NC	No connection

## Block Diagram



**Operation Table**

$\overline{CS1}$	$CS2$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Storage temperature range	$T_{stg}$	-55 to +125	°C
Storage temperature range under bias	$T_{bias}$	-20 to +85	°C

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width  $\leq$  30 ns.  
 2. Maximum voltage is +4.6 V.

**DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	2.2	2.5/3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{CC} = 2.2$ V to 2.7 V $V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	
	$V_{CC} = 2.7$ V to 3.6 V $V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{CC} = 2.2$ V to 2.7 V $V_{IL}$	-0.2	—	0.4	V	1
	$V_{CC} = 2.7$ V to 3.6 V $V_{IL}$	-0.3	—	0.6	V	1
Ambient temperature range	$T_a$	-20	—	70	°C	

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width  $\leq$  30 ns.

## DC Characteristics

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	$\mu\text{A}$	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$ , $V_{IO} = V_{SS} \text{ to } V_{CC}$
Operating current	$I_{CC}$	—	5	20	$\text{mA}$	$\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0 \text{ mA}$
Average operating current	$I_{CC1}$	—	18	25	$\text{mA}$	Min. cycle, duty = 100%, $I_{IO} = 0 \text{ mA}$ , $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$
	$I_{CC2}$	—	2	5	$\text{mA}$	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{IO} = 0 \text{ mA}$ , $\overline{CS1} \leq 0.2 \text{ V}$ , $CS2 \geq V_{CC} - 0.2 \text{ V}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$
Standby current	$I_{SB}$	—	0.1	0.3	$\text{mA}$	$CS2 = V_{IL}$
Standby current	$I_{SB1}^{*2}$	—	0.8	20	$\mu\text{A}$	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$ , $CS2 \geq V_{CC} - 0.2 \text{ V}$ or (3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 \text{ V}$ $CS2 \geq V_{CC} - 0.2 \text{ V}$ $\overline{CS1} \leq 0.2 \text{ V}$
	$I_{SB1}^{*3}$	—	0.8	10	$\mu\text{A}$	
Output high voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$	$V_{OH}$	2.0	—	$\text{V}$	$I_{OH} = -0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	$V_{OH}$	2.4	—	$\text{V}$	$I_{OH} = -1 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$	$V_{OH}$	$V_{CC} - 0.2$	—	$\text{V}$	$I_{OH} = -100 \mu\text{A}$
Output low voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$	$V_{OL}$	—	0.4	$\text{V}$	$I_{OL} = 0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	$V_{OL}$	—	0.4	$\text{V}$	$I_{OL} = 2 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$	$V_{OL}$	—	0.2	$\text{V}$	$I_{OL} = 100 \mu\text{A}$

Notes: 1. Typical values are at  $V_{CC} = 2.5 \text{ V}/3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.



**Capacitance** ( $T_a = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

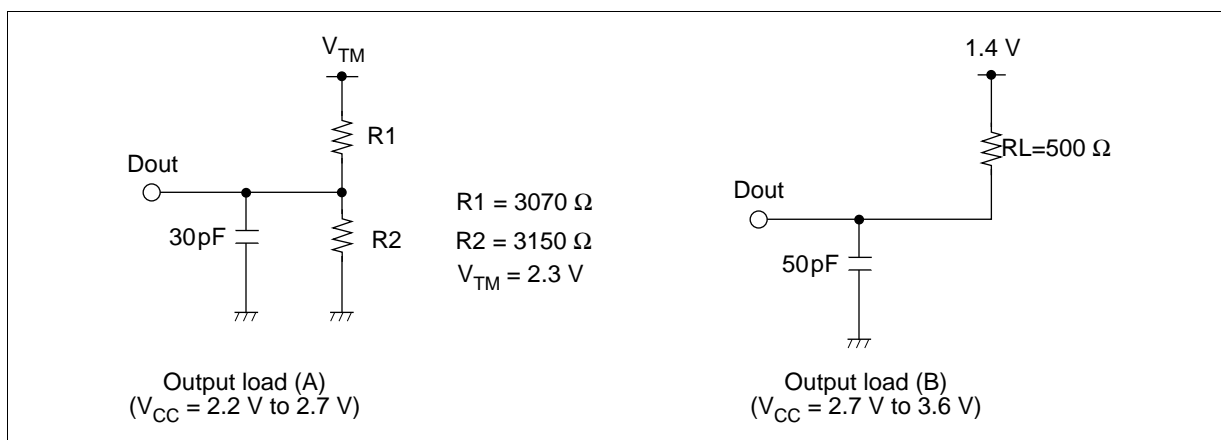
<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test conditions</b>	<b>Note</b>
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0\text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0\text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics (Ta = -20 to +70°C, V<sub>CC</sub> = 2.2 V to 3.6 V, unless otherwise noted.)

### Test Conditions

- Input pulse levels: V<sub>IL</sub> = 0.4 V, V<sub>IH</sub> = 2.0 V (V<sub>CC</sub> = 2.2 V to 2.7 V)  
V<sub>IL</sub> = 0.4 V, V<sub>IH</sub> = 2.2 V (V<sub>CC</sub> = 2.7 V to 3.6 V)
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.1 V (V<sub>CC</sub> = 2.2 V to 2.7 V)
- Output timing reference levels: 1.1 V (V<sub>CC</sub> = 2.2 V to 2.7 V)
- Input timing reference levels: 1.4 V (V<sub>CC</sub> = 2.7 V to 3.6 V)
- Output timing reference levels: 1.4 V (HM62V16256CBP-5, V<sub>CC</sub> = 2.7 V to 3.6 V)  
: 2.0 V/0.8 V (HM62V16256CBP-7, V<sub>CC</sub> = 2.7 V to 3.6 V)
- Output load: See figures (Including scope and jig)



**Read Cycle**

Parameter	Symbol	HM62V16256CBP				Unit	Notes
		-5		-7			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	55	—	70	—	ns	
Address access time	$t_{AA}$	—	55	—	70	ns	
Chip select access time	$t_{ACS1}$	—	55	—	70	ns	
	$t_{ACS2}$	—	55	—	70	ns	
Output enable to output valid	$t_{OE}$	—	35	—	40	ns	
Output hold from address change	$t_{OH}$	10	—	10	—	ns	
$\overline{LB}$ , $\overline{UB}$ access time	$t_{BA}$	—	55	—	70	ns	
Chip select to output in low-Z	$t_{CLZ1}$	10	—	10	—	ns	2, 3
	$t_{CLZ2}$	10	—	10	—	ns	2, 3
$\overline{LB}$ , $\overline{UB}$ enable to low-z	$t_{BLZ}$	5	—	5	—	ns	2, 3
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	$t_{CHZ1}$	0	20	0	25	ns	1, 2, 3
	$t_{CHZ2}$	0	20	0	25	ns	1, 2, 3
$\overline{LB}$ , $\overline{UB}$ disable to high-Z	$t_{BHZ}$	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2, 3

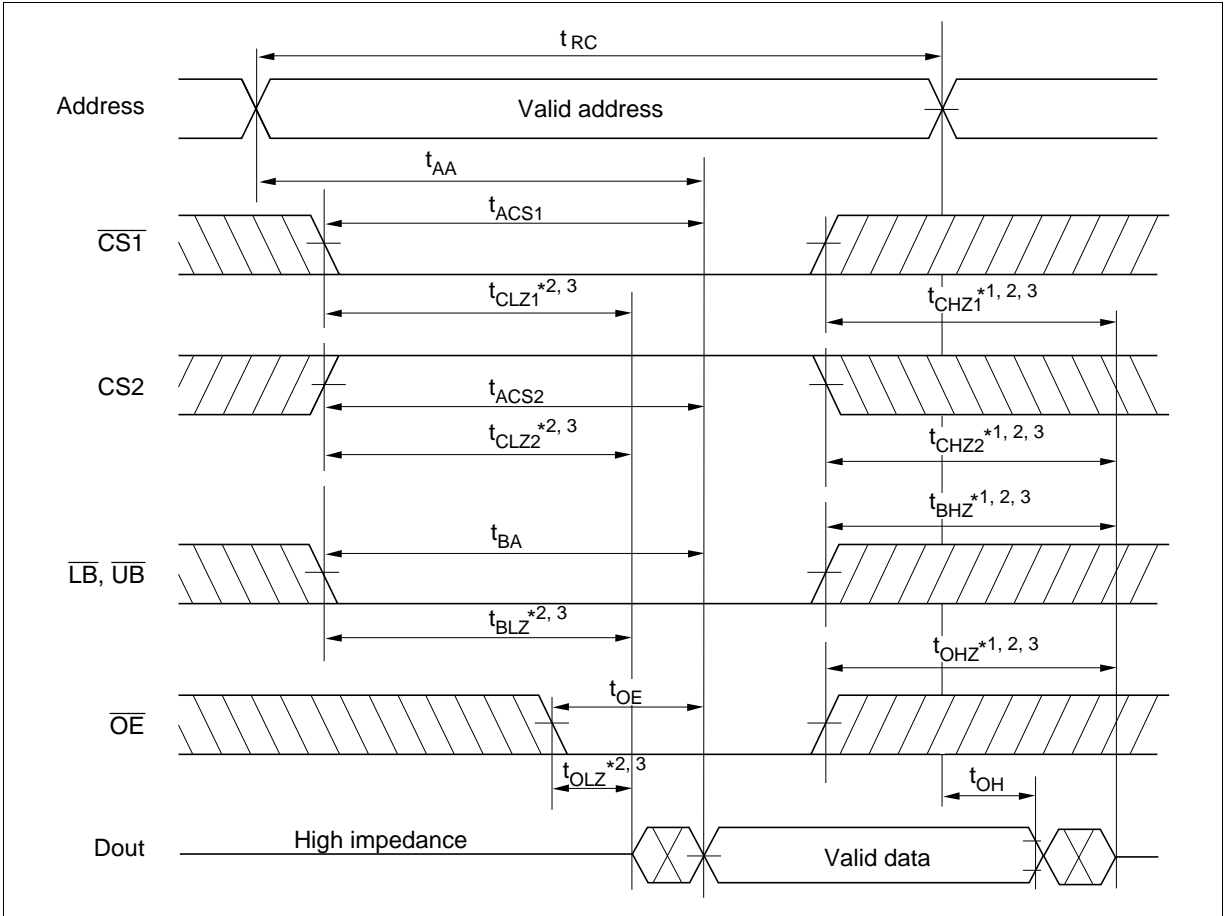
## Write Cycle

Parameter	Symbol	HM62V16256CBP				Unit	Notes
		-5		-7			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	55	—	70	—	ns	
Address valid to end of write	$t_{AW}$	50	—	60	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	60	—	ns	5
Write pulse width	$t_{WP}$	40	—	50	—	ns	4
$\overline{LB}$ , $\overline{UB}$ valid to end of write	$t_{BW}$	50	—	55	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	0	—	ns	7
Data to write time overlap	$t_{DW}$	25	—	30	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in High-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2
Write to output in high-Z	$t_{WHZ}$	0	20	0	25	ns	1, 2

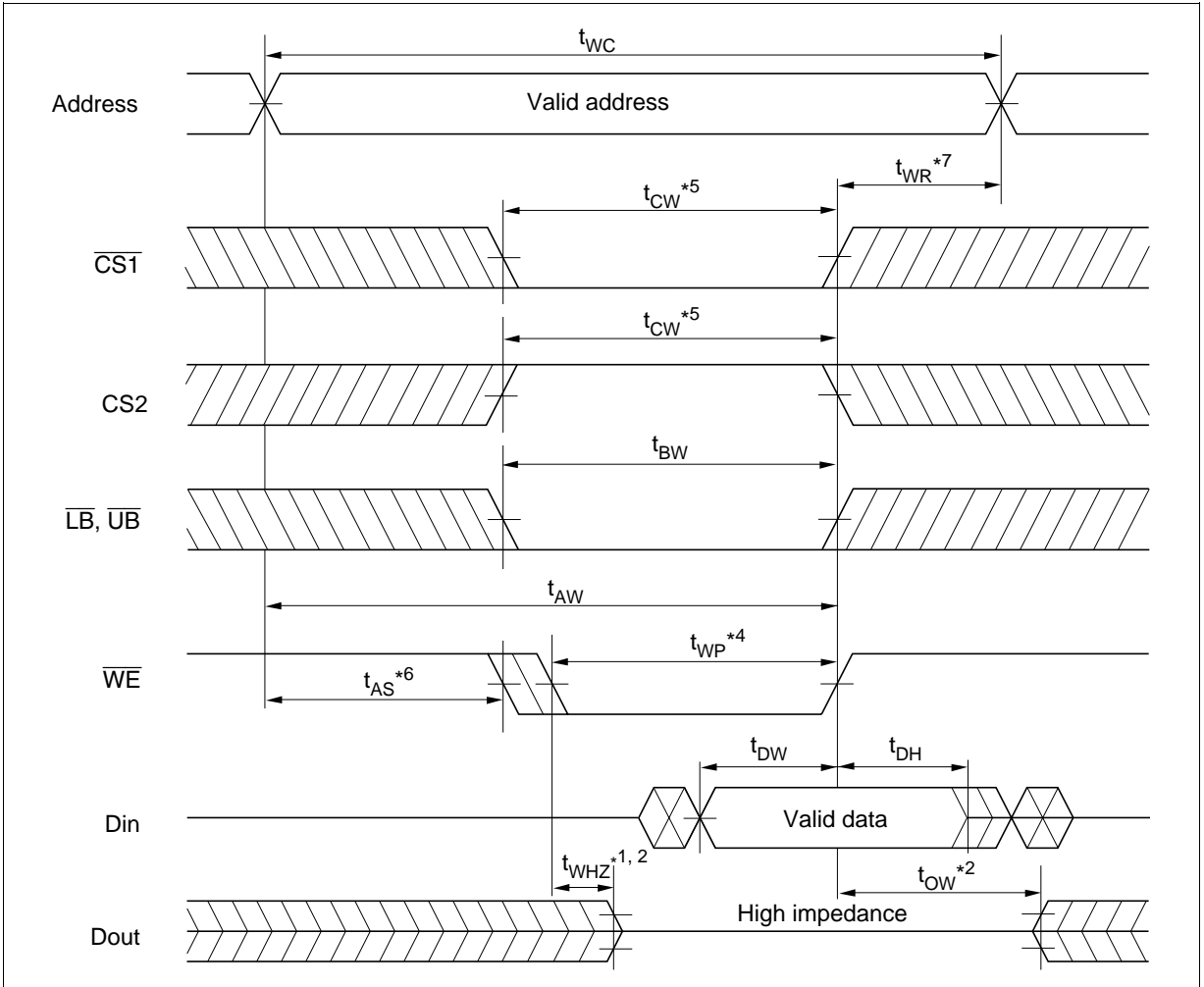
- Notes:
- $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  - A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2, a low  $\overline{WE}$  and a low  $\overline{LB}$  or a low  $\overline{UB}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high,  $\overline{WE}$  going low and  $\overline{LB}$  going low or  $\overline{UB}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low,  $\overline{WE}$  going high and  $\overline{LB}$  going high or  $\overline{UB}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.

Timing Waveform

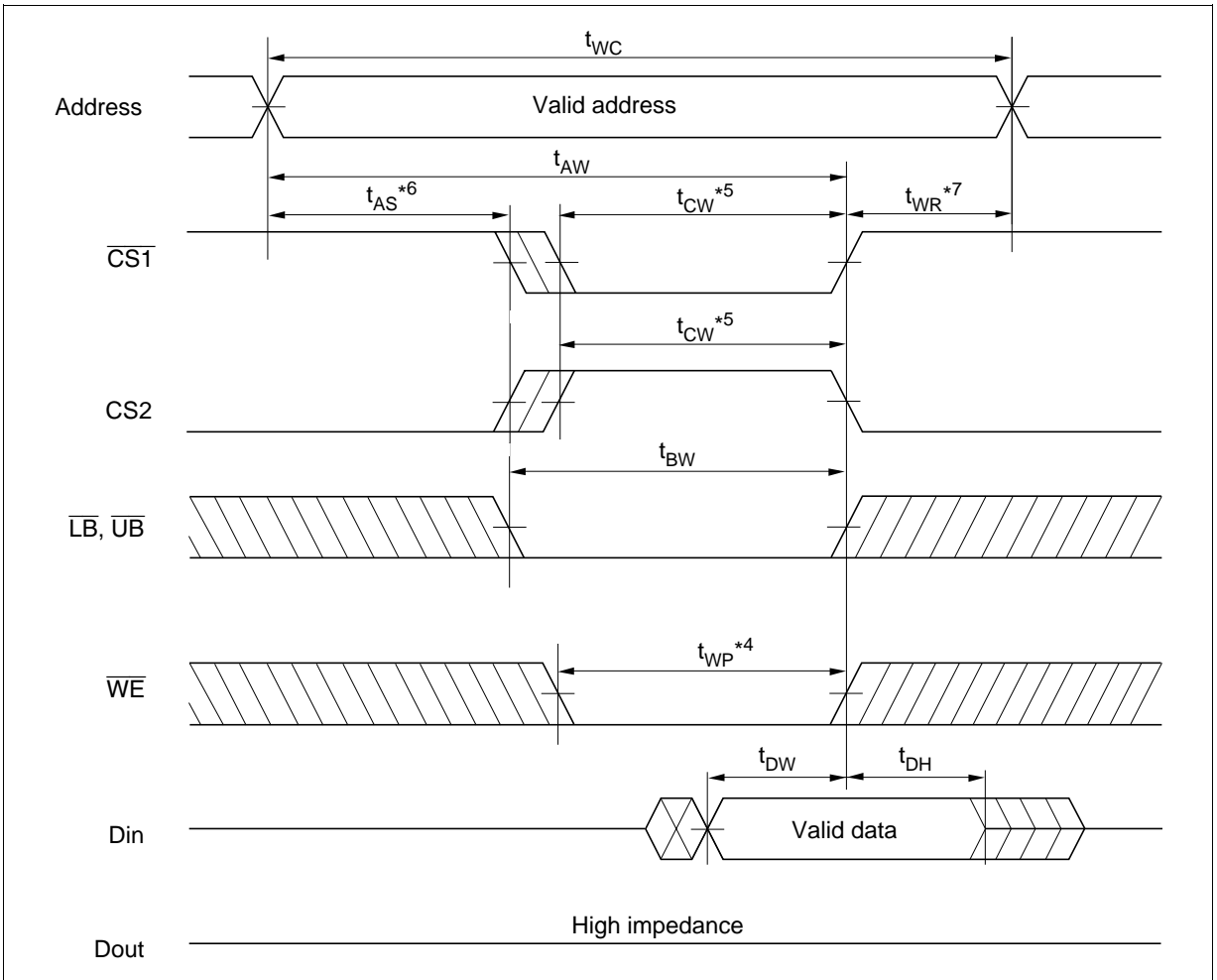
Read Cycle



## Write Cycle (1) ( $\overline{WE}$ Clock)

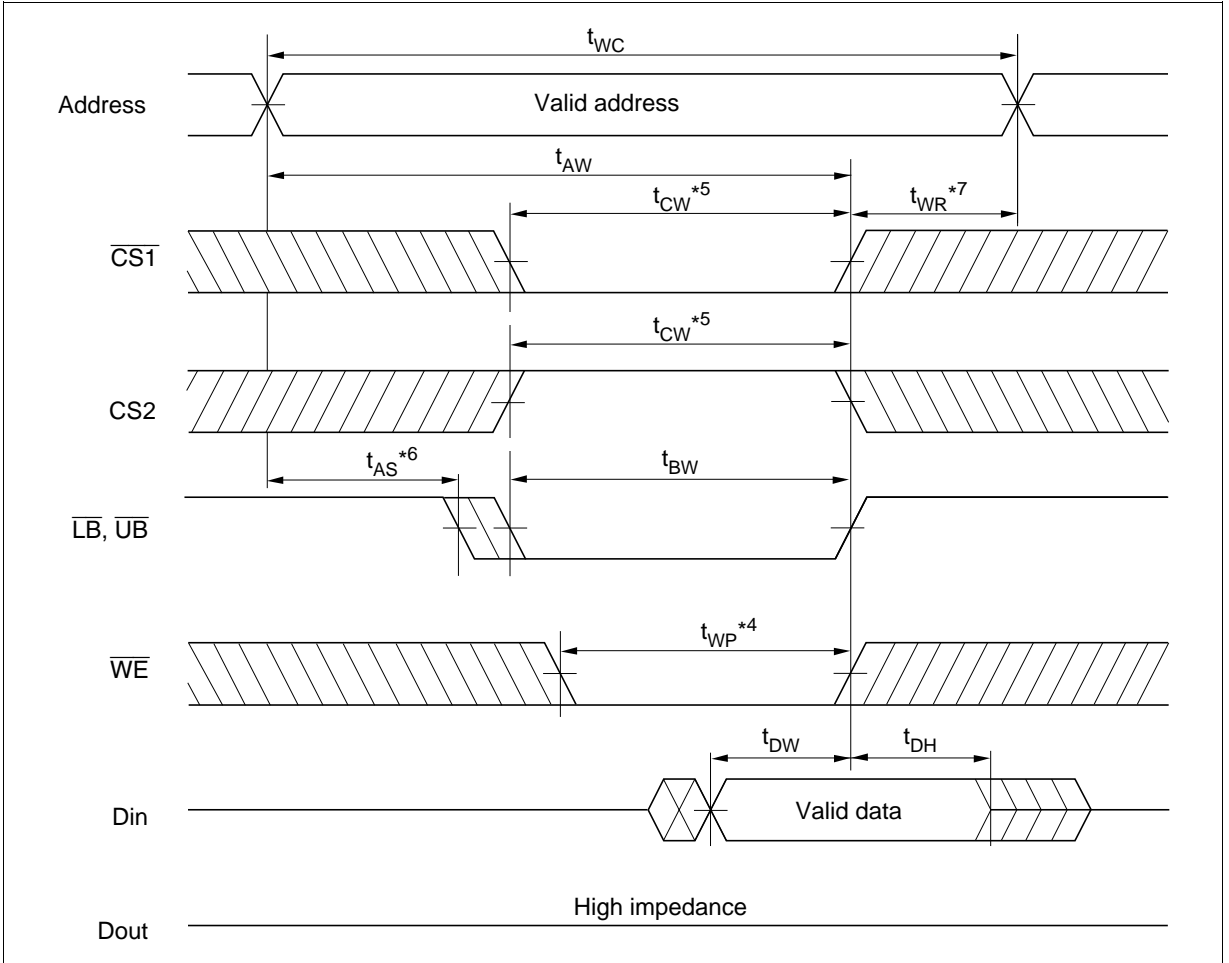


Write Cycle (2) ( $\overline{CS}$  Clock,  $\overline{OE} = V_{IH}$ )



# HM62V16256CBP Series

Write Cycle (3) ( $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  Clock,  $\overline{\text{OE}} = V_{\text{IH}}$ )



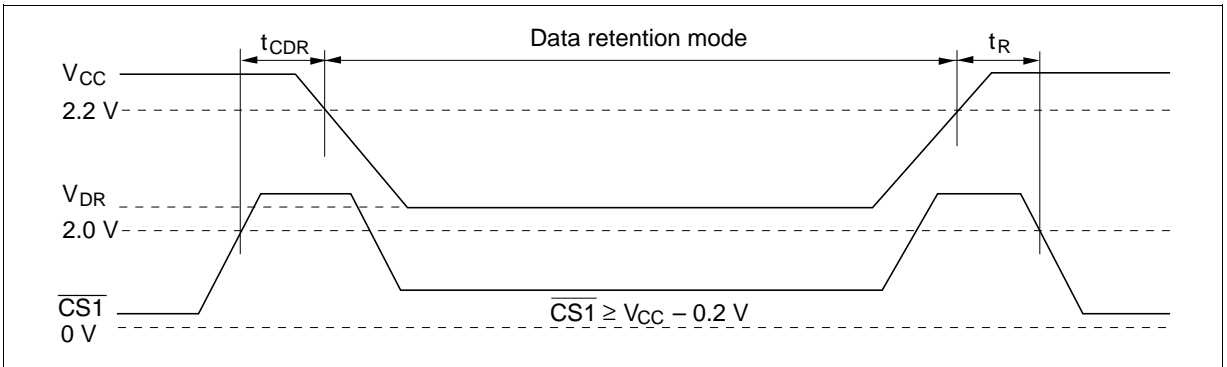


**Low  $V_{CC}$  Data Retention Characteristics ( $T_a = -20$  to  $+70^\circ\text{C}$ )**

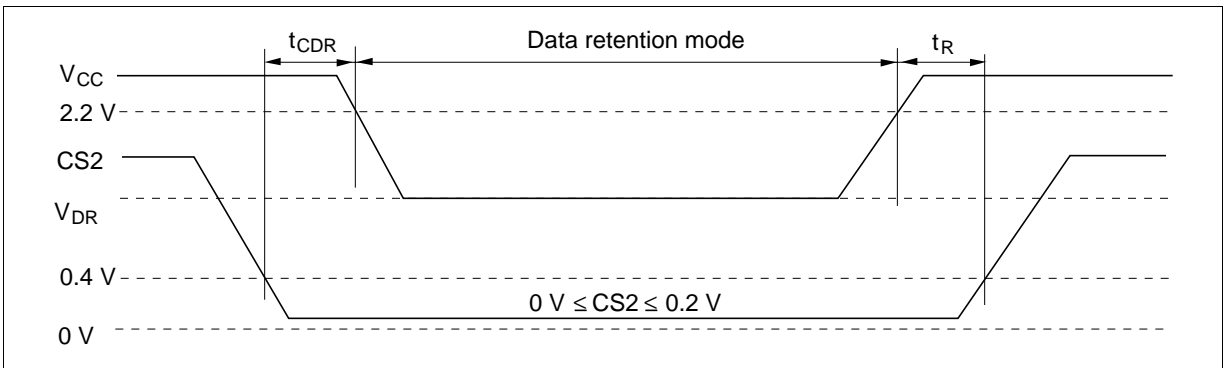
Parameter	Symbol	Min	Typ <sup>*4</sup>	Max	Unit	Test conditions <sup>*3</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	3.6	V	$V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ , $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{V}$ , $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ , $\overline{\text{CS1}} \leq 0.2\text{V}$
Data retention current	$I_{CCDR}^{*1}$	—	0.8	20	$\mu\text{A}$	$V_{CC} = 3.0\text{V}$ , $V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ , $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{V}$ , $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ , $\overline{\text{CS1}} \leq 0.2\text{V}$
	$I_{CCDR}^{*2}$	—	0.8	10	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*5}$	—	—	ns	

- Notes:
1. This characteristic is guaranteed only for L-version, 10  $\mu\text{A}$  max. at  $T_a = -20$  to  $+40^\circ\text{C}$ .
  2. This characteristic is guaranteed only for L-SL version, 3  $\mu\text{A}$  max. at  $T_a = -20$  to  $+40^\circ\text{C}$ .
  3. CS2 controls address buffer,  $\overline{\text{WE}}$  buffer,  $\overline{\text{CS1}}$  buffer,  $\overline{\text{OE}}$  buffer,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{CS1}}$ ,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$ , I/O) can be in the high impedance state. If  $\overline{\text{CS1}}$  controls data retention mode, CS2 must be  $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$  or  $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ . The other input levels (address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$ , I/O) can be in the high impedance state.
  4. Typical values are at  $V_{CC} = 3.0\text{V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.
  5.  $t_{RC}$  = read cycle time.

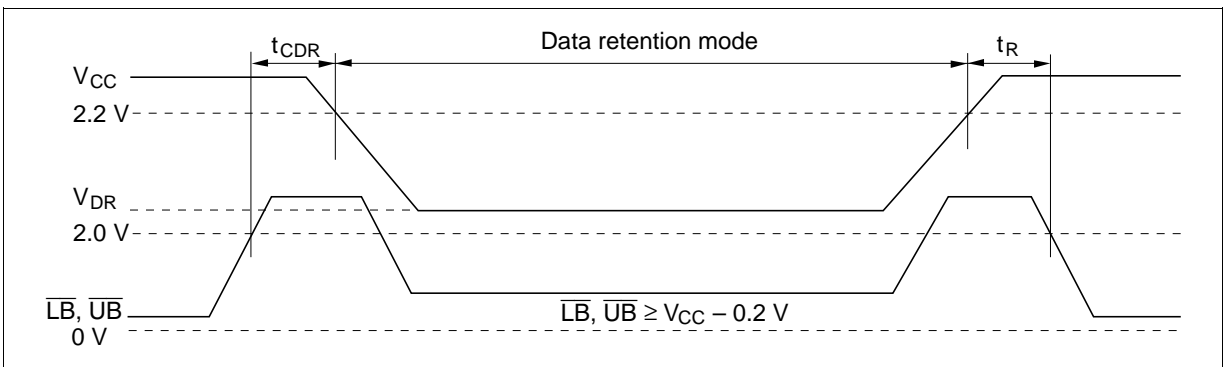
**Low  $V_{CC}$  Data Retention Timing Waveform (1) ( $\overline{CS1}$  Controlled)**



**Low  $V_{CC}$  Data Retention Timing Waveform (2) (CS2 Controlled)**



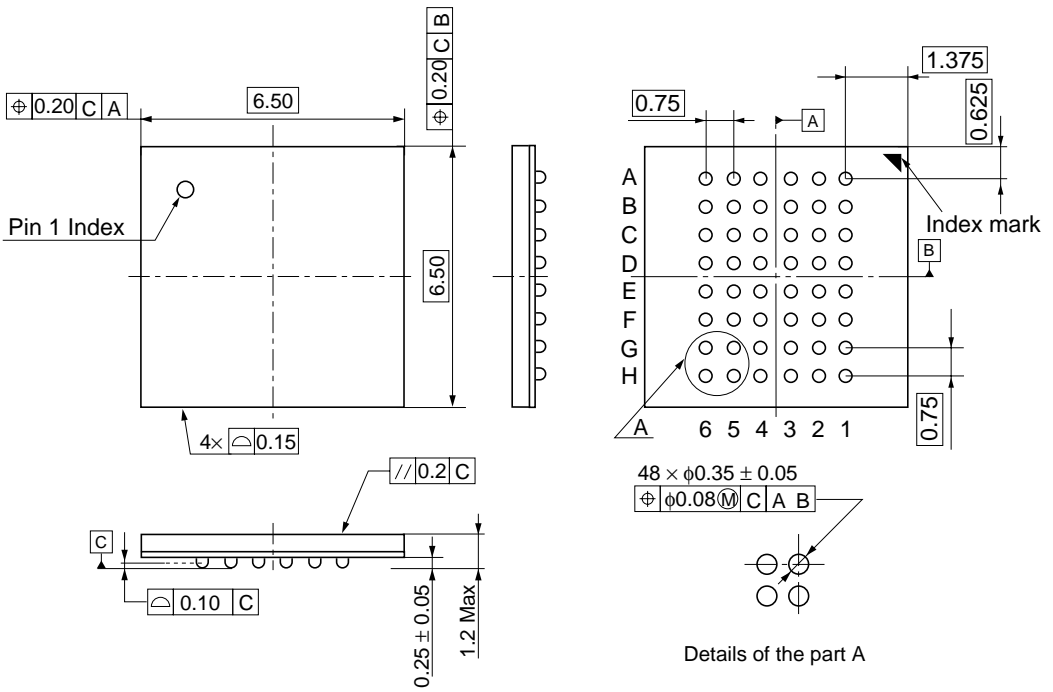
**Low  $V_{CC}$  Data Retention Timing Waveform (3) ( $\overline{LB}$ ,  $\overline{UB}$  Controlled)**



Package Dimensions

HM62V16256CLBP Series (TBP-48)

Unit: mm



Hitachi Code	TBP-48
JEDEC	—
EIAJ	—
Mass	0.09 g

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL      NorthAmerica      : <http://semiconductor.hitachi.com/>  
             Europe                : <http://www.hitachi-eu.com/hel/ecg>  
             Asia                        : <http://sicapac.hitachi-asia.com>  
             Japan                        : <http://www.hitachi.co.jp/Sicd/indx.htm>

## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585200

Hitachi Europe GmbH  
Electronic Components Group  
Domacher StraÙe 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00,  
Singapore 049318  
Tel : <65>-538-6533/538-8577  
Fax : <65>-538-6933/538-3877  
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road,  
Hung-Kuo Building,  
Taipei (105), Taiwan  
Tel : <886>-(2)-2718-3666  
Fax : <886>-(2)-2718-8180  
Telex : 23222 HAS-TP  
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon,  
Hong Kong  
Tel : <852>-(2)-735-9218  
Fax : <852>-(2)-730-0281  
URL : <http://semiconductor.hitachi.com.hk>

Copyright © Hitachi, Ltd., 2001. All rights reserved. Printed in Japan.

Colophon 3.0