



## Frequency Generator for Fibre Channel Systems

### General Description

The ICS9107C-21 and ICS9107C-22 are high-speed clock generators designed to support fibre channel system requirements. The ICS9107C-21 generates a single copy of the 106.25 MHz from a 17 MHz crystal. The ICS9107C-22 provides a second copy of the 106.25 MHz clock with output skew less than  $\pm 100$ ps.

An exact frequency multiplying ratio ensures better than  $\pm 100$  ppm frequency accuracy using a standard AT crystal with external load capacitors (typically  $33\text{pF} \pm 5\%$  for an  $18\text{pF}$  load crystal). Achieving  $\pm 100$  ppm over four years requires the crystal to have a  $\pm 20$  ppm initial accuracy,  $\pm 30$  ppm temperature and  $\pm 5$  ppm/year aging coefficients.

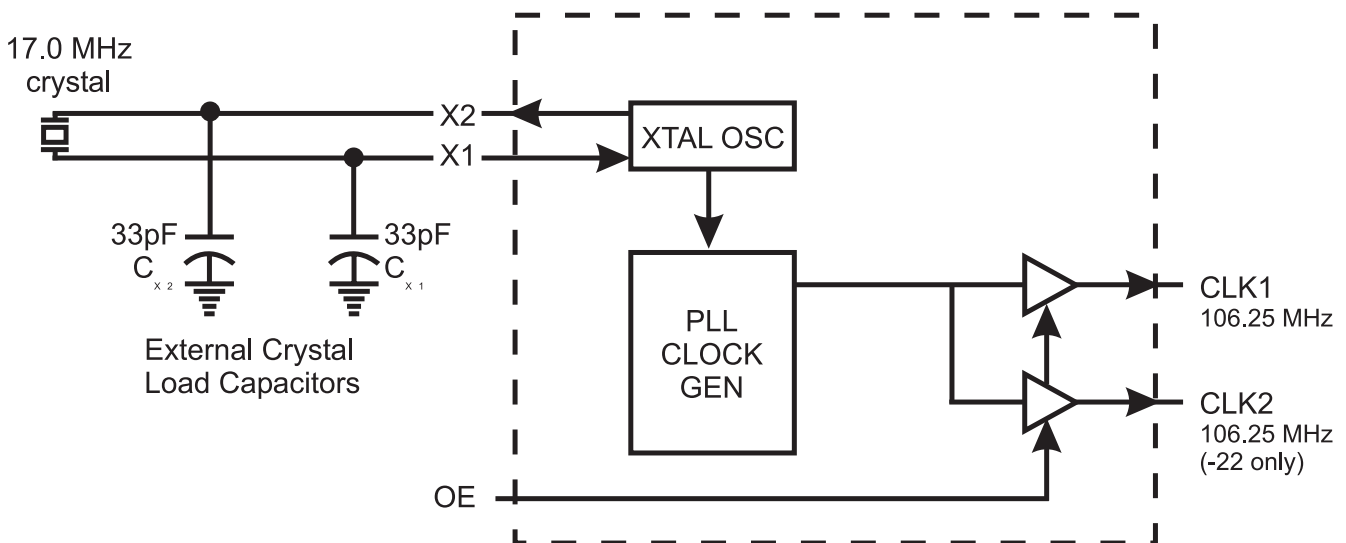
### Features

- Generates one or two 106.25 MHz clocks from a 17 MHz crystal
- Less than 60ps one sigma jitter
- Less than  $\pm 200$ ps absolute jitter
- Output skew less than  $\pm 100$ ps on two channel version (-22)
- Rise/fall times less than 4ns driving  $15\text{pF}$
- On-chip loop filter components
- 5.5V supply range
- 8-pin, 150-mil SOIC package

### Applications

- Specifically designed to support the high-speed clocking requirements of fibre channel systems

### Block Diagram



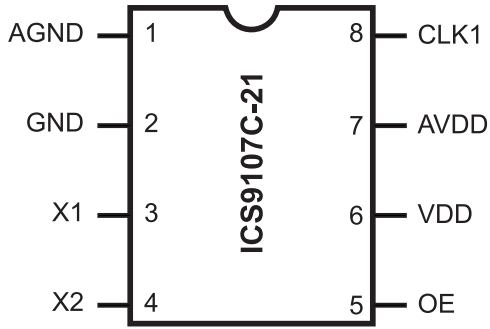
# ICS9107C-21

# ICS9107C-22

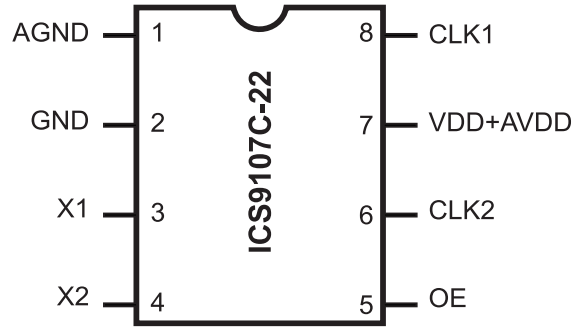
## Preliminary Product Preview



### Pin Configurations



**8-Pin SOIC**



**8-Pin SOIC**

### Functionality

OE	X1, X2 (MHz)	FOUT (MHz)
1	17.00	106.25
0	X	Tristate

### Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	AGND	PWR	Analog ground.
2	GND	PRW	Digital Ground.
3	X1	IN	Crystal or clock input to device; nominally 17.0 MHz. Requires external load capacitors.
4	X2	IN	Crystal drive output from device. Requires external load capacitors.
5	OE	IN	Output enable causes all outputs to tristate when at a logic low level; has a pull-up.
6	VDD CLK2	PWR OUT	+5.0 volt supply (-21). 106.25 MHz clock output (-22).
7	AVDD VDD+AV- DD	PWR PWR	Analog power. (Must equal digital power voltage) (-21). Digital and analog power, +5.0 volt supply (-22).
8	CLK1	OUT	106.25 MHz clock output.



**Absolute Maximum Ratings**

AVDD, VDD referenced to GND . . . . . 7V  
 Operating temperature under bias. . . . . 0°C to +70°C  
 Storage temperature . . . . . -65°C to +150°C  
 Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V  
 Power dissipation . . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

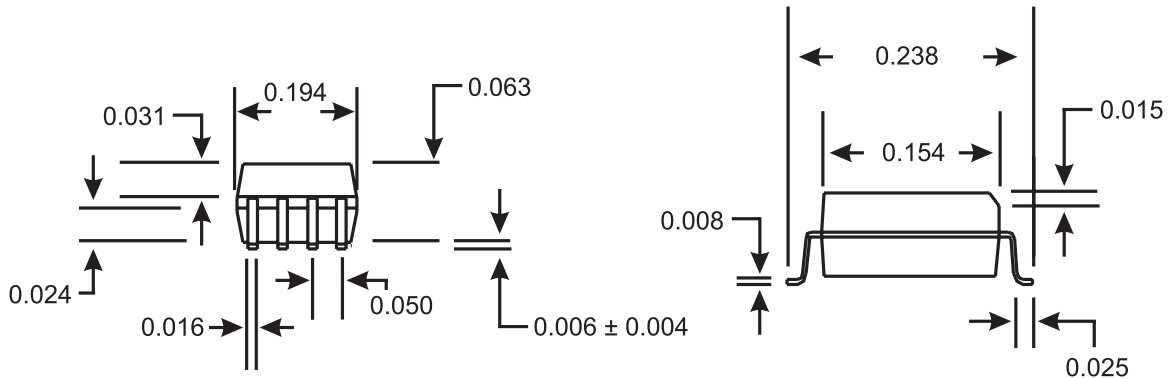
**Electrical Characteristics at 5.0V**

Operating V<sub>DD</sub> = +4.5V to +5.5V; T<sub>A</sub> = 0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V <sub>IL</sub>		-	-	0.8	V
Input High Voltage	V <sub>IH</sub>		2.0	-	-	V
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> =0V (Pull-up input)	-16.0	-6.0	-	μA
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> =V <sub>DD</sub>	-2.0	-	2.0	μA
Output Low Voltage <sup>1</sup>	V <sub>OL</sub>	I <sub>OL</sub> =10mA	-	0.15	0.40	V
Output High Voltage <sup>1</sup>	V <sub>OH</sub>	I <sub>OH</sub> =-30mA	2.4	3.25	-	V
Output Low Current <sup>1</sup>	I <sub>OL</sub>	V <sub>OL</sub> =0.8V	22.0	35.0	-	mA
Output High Current <sup>1</sup>	I <sub>OH</sub>	V <sub>OH</sub> =2.0V	-	-50.0	-35.0	mA
Supply Current	I <sub>DD</sub>	Unloaded	-	22.0	45.0	mA
Pull-up Resistor <sup>1</sup>	R <sub>pu</sub>		-	380.0	700.0	k ohms
AC Characteristics						
Rise Time <sup>1</sup>	T <sub>ri</sub>	15pF load, 0.8 to 2.0V	-	0.8	1.4	ns
Fall Time <sup>1</sup>	T <sub>fi</sub>	15pF load, 2.0 to 0.8V	-	0.7	1.2	ns
Rise Time <sup>1</sup>	T <sub>ri2</sub>	15pF load, 20% to 80%	-	1.5	2.0	ns
Fall Time <sup>1</sup>	T <sub>fi2</sub>	15pF load, 80% to 20%	-	1.0	1.5	ns
Duty Cycle <sup>1</sup>	D <sub>t</sub>	15pF load @ 1.4V	42.0	49.0	55.0	%
Jitter, One Sigma <sup>1</sup>	T <sub>j1s</sub>	15pF load	-	30.0	60.0	ps
Jitter, Absolute <sup>1</sup>	T <sub>jabs</sub>	15pF load	-200.0		200.0	ps
Output Skew, <sup>1</sup> Clock 1 to 2	t <sub>sk1</sub>	15pF load @ 1.4V (-22 only)	-100.0	-20.0	100.0	ps
Input Frequency <sup>1</sup>	F <sub>i</sub>		11.0	17.0	19.0	MHz
Output Frequency <sup>1</sup>	F <sub>o</sub>		2.0	106.25	120.0	MHz
Power-up Time <sup>1</sup>	T <sub>pu</sub>		-	7.58	18.0	ms
Transition Time <sup>1</sup>	T <sub>ft</sub>	8 to 66.6 MHz	-	6.0	13.0	ms
Crystal Input Capacitance <sup>1</sup>	C <sub>inx</sub>	X1 (Pin 3) X2 (Pin 4)	-	5.0	-	pF

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

**ICS9107C-21**  
**ICS9107C-22**  
**Preliminary Product Preview**



**8-Pin Plastic SOIC Package**

**Ordering Information**

**ICS9107C-21CS08 or ICS9107C-22CS08**

Example:

**XXX XXX PPP S X#W**

