

## 8051 Embedded Monitor Controller 64K Flash Type

### GENERAL DESCRIPTIONS

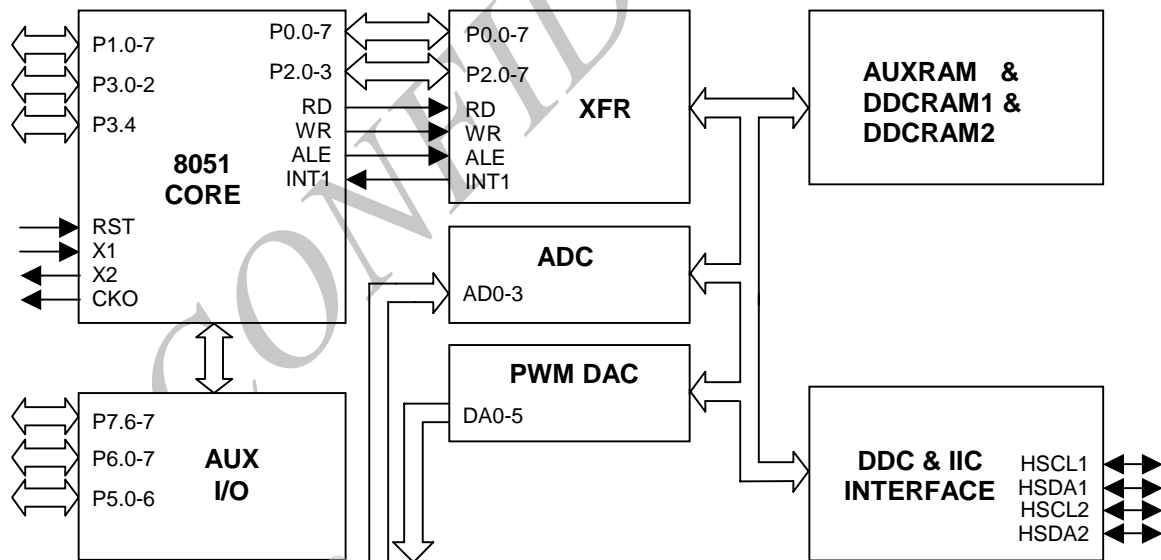
The MTV512M micro-controller is an 8051 CPU core embedded device especially tailored for flat panel display applications. It includes an 8051 CPU core, 768-byte SRAM, 4 channels of 6-bit ADC, 3 external counters/timers, 6 channels of PWM DAC, VESA DDC interface, and a 64K-byte internal program Flash-ROM memory in 44-pin PLCC package.

### FEATURES

- 8051 core, 12MHz operating frequency with single/double CPU clock option
- 0.35um process; 3.3V power supply

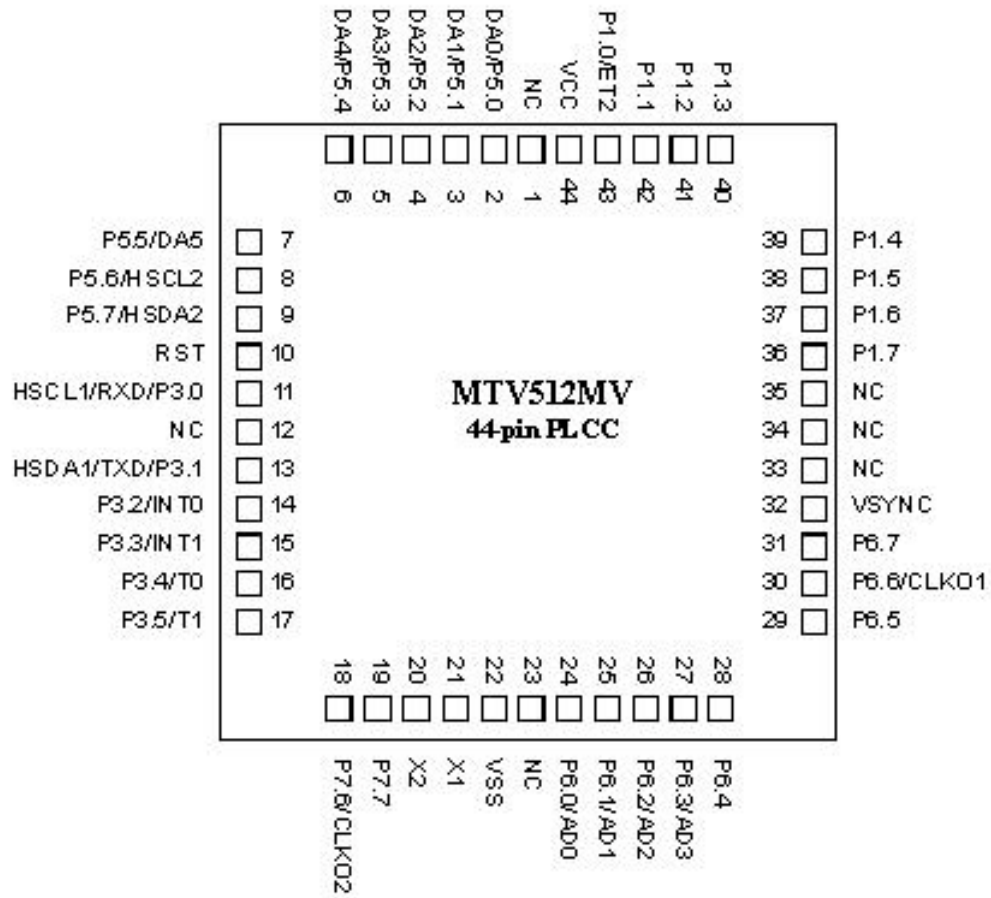
- 768-byte RAM; 64K-byte program Flash memory
- Maximum 6 channels of PWM DAC
- Compliant with VESA DDC1/2B/2Bi/2B+ standard
- Dual slave IIC addresses; two H/W auto transfer DDC1/DDC2x data for both D-sub and DVI interfaces
- Watchdog timer with programmable interval
- Support external counters/timers, 1 & 2
- Single/double frequency clock output
- Two external interrupts, INT1 is shared with Slave IIC interrupt source.
- Maximum 4 channels of 6-bit ADC
- Flash-ROM code protection selection
- 44-pin PLCC package

### BLOCK DIAGRAM



\*This datasheet, which contains proprietary and trade secret information of MYSON CENTURY, INC., is confidential and subject to various privileges against unauthorized disclosure.

PIN CONNECTION



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### PIN CONFIGURATION & DESCRIPTION

A “CMOS output pin” means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.

An “open drain pin” means it can sink at least 4mA current. It can be used as input or output function and needs an external pull up resistor.

An “8051 standard pin” is a pseudo open drain pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 160nS when output transits from low to high, then keeps driving at 120  $\mu$  A to maintain the pin at high level. It can be used as input or output function. It needs an external pull up resistor when driving heavy load device.

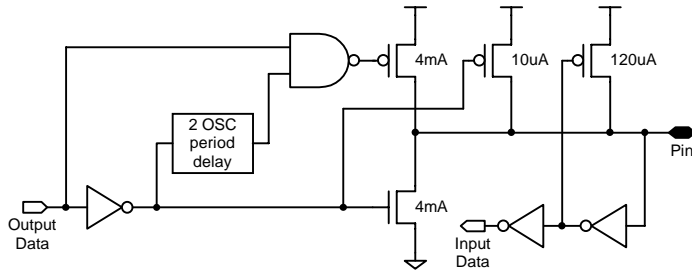
There is an internal pull-up resistance on each CMOS PAD and an internal pull-down resistance on each input PAD. It is recommended to add a pull high resistance on each open drain pin.

| Name            | Pin No. | Direction | Default Direction | Default Output Value | Internal Pull Up/Down | Pin Type             | Description  |
|-----------------|---------|-----------|-------------------|----------------------|-----------------------|----------------------|--|
| NC              | 1       | -         | -                 | -                    | -                     | -                    | No connection  |
| DA0/P5.0        | 2       | I/O       | O                 | 1(DA0)               | -                     | Open Drain           | PWM DAC output/General purpose I/O (open drain)      |
| DA1/P5.1        | 3       | I/O       | O                 | 1(DA1)               | -                     | Open Drain           | PWM DAC output/General purpose I/O (open drain)      |
| DA2/P5.2        | 4       | I/O       | O                 | 1(DA2)               | -                     | Open Drain           | PWM DAC output/General purpose I/O (open drain)      |
| DA3/P5.3        | 5       | I/O       | O                 | 1(DA3)               | -                     | Open Drain           | PWM DAC output/General purpose I/O (open drain)      |
| DA4/ P5.4       | 6       | I/O       | O                 | 1(DA4)               | -                     | Open Drain           | PWM DAC output/General purpose I/O (open drain)      |
| P5.5/DA5        | 7       | I/O       | O                 | 1(P5.5)              | -                     | Open Drain           | PWM DAC output/General purpose I/O (open drain)      |
| P5.6/HSCL2      | 8       | I/O       | I                 | Z(P5.6)              | -                     | Open Drain w/ filter | General purpose I/O/Slave IIC1 SCL2 (open drain)     |
| P5.7/HSDA2      | 9       | I/O       | I                 | Z(P5.7)              | -                     | Open Drain w/ filter | General purpose I/O/Slave IIC1 SDA2 (open drain)     |
| RST             | 10      | I         | I                 | 0                    | down                  | Input                | High Active RESET                                    |
| HSCL1/P3.0/RXD  | 11      | I/O       | I/O               | Z(HSCL1)             | -                     | Open Drain w/ filter | Slave IIC clock/General purpose I/O/Rxd (open drain) |
| NC              | 12      | -         | -                 |                      | -                     | -                    | No connection  |
| HSDA1/P3.1/TXD0 | 13      | I/O       | I/O               | Z(HSDA1)             | -                     | Open Drain w/ filter | Slave IIC data/General purpose I/O/Txd (open drain)  |

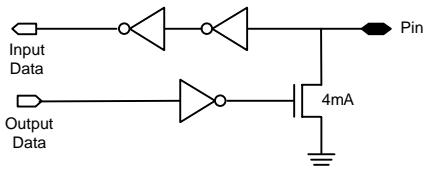
| Name       | Pin No. | Direction | Default Direction | Default Output Value | Internal Pull Up/Down | Pin Type      | Description   |
|------------|---------|-----------|-------------------|----------------------|-----------------------|---------------|---|
| P3.2/INT0  | 14      | I/O       | I                 | Z(P3.2)              | -                     | Standard 8051 | General purpose I/O/External interrupt 0 (Standard 8051)    |
| P3.3/INT1  | 15      | I/O       | I                 | Z(P3.3)              | -                     | Standard 8051 | General purpose I/O/External interrupt 1 (Standard 8051)    |
| P3.4/T0    | 16      | I/O       | I                 | Z(P3.4)              | -                     | Standard 8051 | General purpose I/O/T0 Ext. Counter/Timer 0 (Standard 8051) |
| P3.5/T1    | 17      | I/O       | I                 | Z(P3.5)              | -                     | Standard 8051 | General purpose I/O/T1 Ext. Counter/Timer 1 (Standard 8051) |
| P7.6/CLKO2 | 18      | I/O       | I                 | 1(P7.6)              | up                    | CMOS          | General purpose I/O /Clock out 2 (CMOS)                     |
| P7.7       | 19      | I/O       | I                 | 1                    | up                    | CMOS          | General purpose I/O (CMOS)                                  |
| X2         | 20      | O         | -                 | -                    | -                     | -             | Crystal Out   |
| X1         | 21      | I         | -                 | -                    | -                     | -             | Crystal In  |
| VSS        | 22      | -         | -                 | -                    | -                     | -             | Ground  |
| NC         | 23      | -         | -                 | -                    | -                     | -             | No connection   |
| P6.0/AD0   | 24      | I/O       | I                 | 1(P6.0)              | up                    | CMOS          | General purpose I/O (CMOS) /6-bit ADC channel 0 input       |
| P6.1/AD1   | 25      | I/O       | I                 | 1(P6.1)              | up                    | CMOS          | General purpose I/O (CMOS) /6-bit ADC channel 1 input       |
| P6.2/AD2   | 26      | I/O       | I                 | 1(P6.2)              | up                    | CMOS          | General purpose I/O (CMOS) /6-bit ADC channel 2 input       |
| P6.3/AD3   | 27      | I/O       | I                 | 1(P6.3)              | up                    | CMOS          | General purpose I/O (CMOS) /6-bit ADC channel 3 input       |
| P6.4       | 28      | I/O       | I                 | 1                    | up                    | CMOS          | General purpose I/O (CMOS)                                  |
| P6.5       | 29      | I/O       | I                 | 1                    | up                    | CMOS          | General purpose I/O (CMOS)                                  |
| P6.6/CLKO1 | 30      | I/O       | I                 | 1(P6.6)              | up                    | CMOS          | General purpose I/O/CLKO1 (CMOS)                            |
| P6.7       | 31      | I/O       | I                 | 1                    | up                    | CMOS          | General purpose I/O (CMOS)                                  |

| Name     | Pin No. | Direction | Default Direction | Default Output Value | Internal Pull Up/Down | Pin Type              | Description  |
|----------|---------|-----------|-------------------|----------------------|-----------------------|-----------------------|--|
| VSYNC    | 32      | I         | I                 | 0                    | down                  | Input                 | VSYNC input  |
| NC       | 33      | -         | -                 | -                    | -                     | -                     | No connection  |
| NC       | 34      | -         | -                 | -                    | -                     | -                     | No connection  |
| NC       | 35      | -         | -                 | -                    | -                     | -                     | No connection  |
| P1.7     | 36      | I/O       | I                 | Z                    | -                     | Standard 8051 or CMOS | General purpose I/O (Standard 8051/CMOS)                         |
| P1.6     | 37      | I/O       | I                 | Z                    | -                     | Standard 8051 or CMOS | General purpose I/O (Standard 8051/CMOS)                         |
| P1.5     | 38      | I/O       | I                 | Z                    | -                     | Standard 8051 or CMOS | General purpose I/O (Standard 8051/CMOS)                         |
| P1.4     | 39      | I/O       | I                 | Z                    | -                     | Standard 8051 or CMOS | General purpose I/O (Standard 8051/CMOS)                         |
| P1.3     | 40      | I/O       | I                 | Z                    | -                     | Standard 8051 or CMOS | General purpose I/O (Standard 8051/CMOS)                         |
| P1.2     | 41      | I/O       | I                 | Z                    | -                     | Standard 8051 or CMOS | General purpose I/O (Standard 8051/CMOS)                         |
| P1.1     | 42      | I/O       | I                 | Z                    | -                     | Standard 8051 or CMOS | General purpose I/O (Standard 8051/CMOS)                         |
| P1.0/ET2 | 43      | I/O       | I                 | Z(P1.0)              | -                     | Standard 8051 or CMOS | General purpose I/O/External Counter/Timer2 (Standard 8051/CMOS) |
| VCC      | 44      | -         | -                 | -                    | -                     | -                     | 3.3V power   |

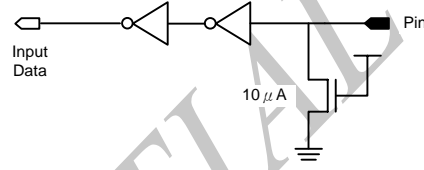
**Pin Types**



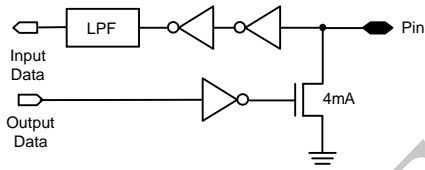
**8051 Standard Pin**



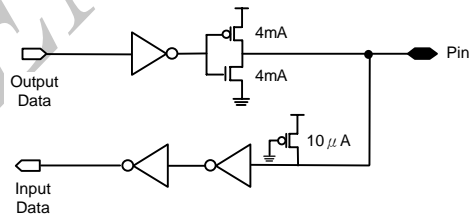
**Open Drain Pin**



**Inputs**



**Open Drain with Filter Pin**



**CMOS**

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## FUNCTIONAL DESCRIPTIONS

### 8051 CPU Core

The CPU core of MTV512M is compatible with the industry standard 8051, which includes 256 bytes RAM, Special Function Registers (SFR), two timers, five interrupt sources and a serial UART interface. The CPU core fetches its program code from the 64K bytes Flash memory in MTV512M. It uses Port0 and Port2 to access the "external special function register" (XFR) and external auxiliary RAM (AUXRAM).

The CPU core can run at double rate when FclkE is set. When the operating X'tal is 12MHz, Once the bit is set, the CPU runs as if a 24MHz X'tal is applied on MTV512M, but the peripherals (IIC, DDC, Etimer, ADC, DAC) still run at the original frequency.

**Note: All registers listed in this document reside in 8051's external RAM area (XFR). For internal RAM memory map, please refer to 8051 spec.**

### Memory Allocation

#### i) Internal Special Function Registers (SFR)

The SFR is a group of registers that are the same as standard 8051.

#### ii) Internal RAM

There are total 256 bytes internal RAM in MTV512M, the same as standard 8052.

#### iii) External Special Function Registers (XFR)

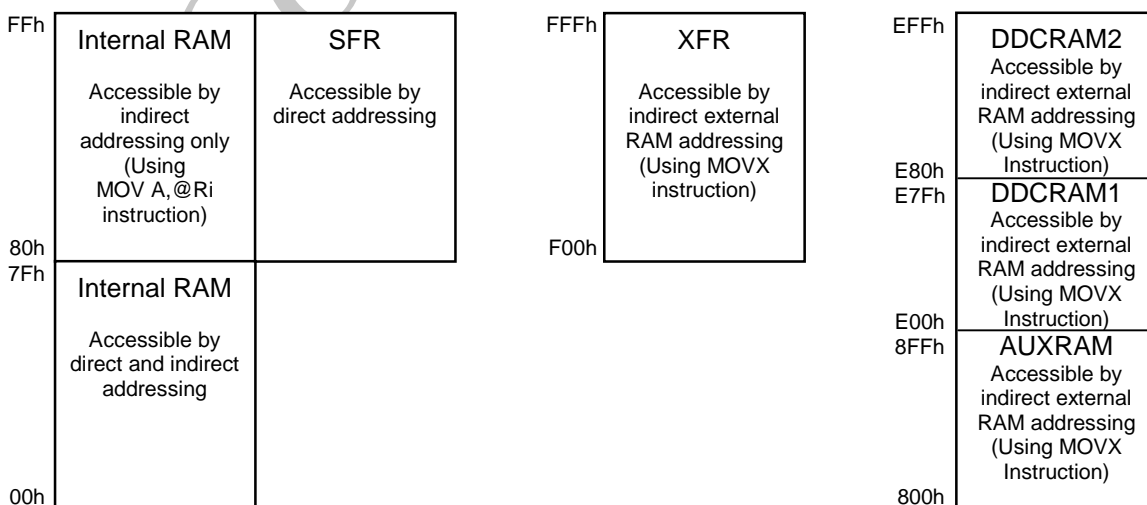
The XFR is a group of registers allocated in the 8051 external RAM area F00h – FFFh. These registers are used for special functions. Programs can use "MOVX" instruction to access these registers.

#### iv) Auxiliary RAM (AUXRAM)

There are total 256 bytes auxiliary RAM allocated in the 8051 external RAM area 800h - 8FFh. Programs can use "MOVX" instruction to access the AUXRAM.

#### v) Dual Port RAM (DDCRAM)

There are 256 bytes Dual Port RAM allocated in the 8051 external RAM area E00h - EFFh. Programs can use "MOVX" instruction to access the RAM. The external DDC1/2 Host can access the RAM as if a 24LC0x EEPROM is connected onto the interface. Address from E00h to E7Fh is for external DDC host1 to access the DDC data. Address from E80h to EFFh is for external DDC host2.



## Chip Configuration

The Chip Configuration registers define configuration of the chip and function of the pins.

| Reg name | addr    | bit7   | bit6   | bit5   | bit4  | bit3  | bit2  | bit1  | bit0  |
|----------|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| PADMOD   | F50h(w) |        |        |        |       | AD3E  | AD2E  | AD1E  | AD0E  |
| PADMOD   | F51h(w) |        |        | P55E   | P54E  | P53E  | P52E  | P51E  | P50E  |
| PADMOD   | F52h(w) | HIIC1E |        | HIIC2E | CKOE1 |       |       |       |       |
| PADMOD   | F53h(w) | P57oe  | P56oe  | P55oe  | P54oe | P53oe | P52oe | P51oe | P50oe |
| PADMOD   | F54h(w) | P67oe  | P66oe  | P65oe  | P64oe | P63oe | P62oe | P61oe | P60oe |
| PADMOD   | F55h(w) | COP17  | COP16  | COP15  | COP14 | COP13 | COP12 | COP11 | COP10 |
| OPTION   | F56h(w) | PWMF   | DIV253 | FclkE  | DCLK  | ENSCL |       |       | IP77E |
| PADMOD   | F5Eh(w) |        | CKOE2  |        |       |       |       |       |       |
| PADMOD   | F5Fh(w) | P77oe  | P76oe  |        |       |       |       |       |       |

**PADMOD (w)** : Pad mode control registers. (All are "0" in Chip Reset, except for HIIC1E bit)

- AD3E = 1 → Pin "P6.3/AD3" is AD3.  
 = 0 → Pin "P6.3/AD3" is P6.3.
- AD2E = 1 → Pin "P6.2/AD2" is AD2.  
 = 0 → Pin "P6.2/AD2" is P6.2.
- AD1E = 1 → Pin "P6.1/AD1" is AD1.  
 = 0 → Pin "P6.1/AD1" is P6.1.
- AD0E = 1 → Pin "P6.0/AD0" is AD0.  
 = 0 → Pin "P6.0/AD0" is P6.0.
- P55E = 1 → Pin "DA5/P5.5" is P5.5.  
 = 0 → Pin "DA5/P5.5" is DA5.
- P54E = 1 → Pin "DA4/P5.4" is P5.4.  
 = 0 → Pin "DA4/P5.4" is DA4.
- P53E = 1 → Pin "DA3/P5.3" is P5.3.  
 = 0 → Pin "DA3/P5.3" is DA3.
- P52E = 1 → Pin "DA2/P5.2" is P5.2.  
 = 0 → Pin "DA2/P5.2" is DA2.
- P51E = 1 → Pin "DA1/P5.1" is P5.1.  
 = 0 → Pin "DA1/P5.1" is DA1.
- P50E = 1 → Pin "DA0/P5.0" is P5.0.  
 = 0 → Pin "DA0/P5.0" is DA0.
- HIIC1E = 1 → Pin "HSCL1/P3.0/Rxd" is HSCL1; pin "HSDA1/P3.1/Txd" is HSDA1.  
 = 0 → Pin "HSCL1/P3.0/Rxd" is P3.0/Rxd; pin "HSDA1/P3.1/Txd" is P3.1/Txd.
- HIIC2E = 1 → Pin "HSCL2/P5.6" is HSCL2. Pin "HSDA2/P5.7" is HSDA2.  
 = 0 → Pin "HSCL2/P5.6" is P5.6. Pin "HSDA2/P5.7" is P5.7.
- CKOE1 = 1 → Pin "P6.6/CLKO1" is P6.6.  
 = 0 → Pin "P6.6/CLKO1" is CLKO1.



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|           |                                    |
|-----------|------------------------------------|
| P57oe = 1 | → P5.7 is output pin.              |
| = 0       | → P5.7 is input pin.               |
| P56oe = 1 | → P5.6 is output pin.              |
| = 0       | → P5.6 is input pin.               |
| P55oe = 1 | → P5.5 is output pin.              |
| = 0       | → P5.5 is input pin.               |
| P54oe = 1 | → P5.4 is output pin.              |
| = 0       | → P5.4 is input pin.               |
| P53oe = 1 | → P5.3 is output pin.              |
| = 0       | → P5.3 is input pin.               |
| P52oe = 1 | → P5.2 is output pin.              |
| = 0       | → P5.2 is input pin.               |
| P51oe = 1 | → P5.1 is output pin.              |
| = 0       | → P5.1 is input pin.               |
| P50oe = 1 | → P5.0 is output pin.              |
| = 0       | → P5.0 is input pin.               |
| P67oe = 1 | → P6.7 is output pin.              |
| = 0       | → P6.7 is input pin.               |
| P66oe = 1 | → P6.6 is output pin.              |
| = 0       | → P6.6 is input pin.               |
| P65oe = 1 | → P6.5 is output pin.              |
| = 0       | → P6.5 is input pin.               |
| P64oe = 1 | → P6.4 is output pin.              |
| = 0       | → P6.4 is input pin.               |
| P63oe = 1 | → P6.3 is output pin.              |
| = 0       | → P6.3 is input pin.               |
| P62oe = 1 | → P6.2 is output pin.              |
| = 0       | → P6.2 is input pin.               |
| P61oe = 1 | → P6.1 is output pin.              |
| = 0       | → P6.1 is input pin.               |
| P60oe = 1 | → P6.0 is output pin.              |
| = 0       | → P6.0 is input pin.               |
| COP17 = 1 | → Pin "P1.7" is CMOS Output.       |
| = 0       | → Pin "P1.7" is 8051 standard I/O. |
| COP16 = 1 | → Pin "P1.6" is CMOS Output.       |
| = 0       | → Pin "P1.6" is 8051 standard I/O. |
| COP15 = 1 | → Pin "P1.5" is CMOS Output.       |
| = 0       | → Pin "P1.5" is 8051 standard I/O. |
| COP14 = 1 | → Pin "P1.4" is CMOS Output.       |
| = 0       | → Pin "P1.4" is 8051 standard I/O. |
| COP13 = 1 | → Pin "P1.3" is CMOS Output.       |
| = 0       | → Pin "P1.3" is 8051 standard I/O. |
| COP12 = 1 | → Pin "P1.2" is CMOS Output.       |

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= 0 → Pin "P1.2" is 8051 standard I/O.  
 COP11 = 1 → Pin "P1.1" is CMOS Output.  
 = 0 → Pin "P1.1" is 8051 standard I/O.  
 COP10 = 1 → Pin "P1.0" is CMOS Output.  
 = 0 → Pin "P1.0" is 8051 standard I/O.  
 P77oe = 1 → P7.7 is output pin.  
 = 0 → P7.7 is input pin.  
 P76oe = 1 → P7.6 is output pin.  
 = 0 → P7.6 is input pin.  
 IP77E = 1 → Pin "P7.7 is P7.7. Available in ICE Mode only.  
 = 0 → reserved.  
 CKOE2 = 1 → Pin "P7.6/CLKO2" is CLKO2.  
 = 0 → Pin "P7.6/CLKO2" is P7.6.

**OPTION (w) :** Chip option configuration (All are "0" in Chip Reset).

PWMF = 1 → Selects 94KHz PWM frequency.  
 = 0 → Selects 47KHz PWM frequency.  
 DIV253 = 1 → PWM pulse width is 253-step resolution.  
 = 0 → PWM pulse width is 256-step resolution.  
 FclkE = 1 → CPU is running at double rate  
 = 0 → CPU is running at normal rate  
 DCLK = 1 → CLKO1 & CLKO2 outputs double frequency system clock.  
 = 0 → CLKO1 & CLKO2 outputs single frequency system clock.  
 ENSCL = 1 → Enable slave IIC block to hold HSCL pin low while MTV512M is unable to catch-up with the external master's speed.

## I/O Ports

### i) Port1

Port1 is a group of pseudo open drain pins or CMOS output pins. It can be used as general purpose I/O. Behavior of Port1 is the same as standard 8051.

### ii) P3.0-2, P3.4

If these pins are not set as IIC pins, Port3 can be used as general purpose I/O, interrupt, UART and Timer pins. Behavior of Port3 is the same as standard 8051.

### iii) Port5, Port6 and Port7

Port5, Port6 and Port7 are used as general purpose I/O. S/W needs to set the corresponding P5(n)oe and P6(n)oe to define whether these pins are input or output.

| Reg name | addr      | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|----------|-----------|------|------|------|------|------|------|------|------|
| PORT5    | F30h(r/w) |      |      |      |      |      |      |      | P50  |
| PORT5    | F31h(r/w) |      |      |      |      |      |      |      | P51  |
| PORT5    | F32h(r/w) |      |      |      |      |      |      |      | P52  |
| PORT5    | F33h(r/w) |      |      |      |      |      |      |      | P53  |

|       |           |  |  |  |  |  |  |  |     |
|-------|-----------|--|--|--|--|--|--|--|-----|
| PORT5 | F34h(r/w) |  |  |  |  |  |  |  | P54 |
| PORT5 | F35h(r/w) |  |  |  |  |  |  |  | P55 |
| PORT5 | F36h(r/w) |  |  |  |  |  |  |  | P56 |
| PORT5 | F37h(r/w) |  |  |  |  |  |  |  | P57 |
| PORT6 | F38h(r/w) |  |  |  |  |  |  |  | P60 |
| PORT6 | F39h(r/w) |  |  |  |  |  |  |  | P61 |
| PORT6 | F3Ah(r/w) |  |  |  |  |  |  |  | P62 |
| PORT6 | F3Bh(r/w) |  |  |  |  |  |  |  | P63 |
| PORT6 | F3Ch(r/w) |  |  |  |  |  |  |  | P64 |
| PORT6 | F3Dh(r/w) |  |  |  |  |  |  |  | P65 |
| PORT6 | F3Eh(r/w) |  |  |  |  |  |  |  | P66 |
| PORT6 | F3Fh(r/w) |  |  |  |  |  |  |  | P67 |
| PORT7 | F76h(r/w) |  |  |  |  |  |  |  | P76 |
| PORT7 | F77h(r/w) |  |  |  |  |  |  |  | P77 |

**PORT5** (r/w) : Port 5 data input/output value.

**PORT6** (r/w) : Port 6 data input/output value.

#### PWM DAC

Each output pulse width of PWM DAC converter is controlled by an 8-bit register in XFR. The frequency of PWM clock is 47KHz or 94KHz, selected by PWMF. And the total duty cycle step of these DAC outputs is 253 or 256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to DAC register generates stable high output. If DIV253=0, the output pulses low at least once even if the DAC register's content is FFH. Writing 00H to DAC register generates stable low output.

| Reg name | addr      | bit7                     | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|----------|-----------|--------------------------|------|------|------|------|------|------|------|
| DA0      | F20h(r/w) | Pulse width of PWM DAC 0 |      |      |      |      |      |      |      |
| DA1      | F21h(r/w) | Pulse width of PWM DAC 1 |      |      |      |      |      |      |      |
| DA2      | F22h(r/w) | Pulse width of PWM DAC 2 |      |      |      |      |      |      |      |
| DA3      | F23h(r/w) | Pulse width of PWM DAC 3 |      |      |      |      |      |      |      |
| DA4      | F24h(r/w) | Pulse width of PWM DAC 4 |      |      |      |      |      |      |      |
| DA5      | F25h(r/w) | Pulse width of PWM DAC 5 |      |      |      |      |      |      |      |

**DA0-5** (r/w) : The output pulse width control for DA0-5.

\* All of PWM DAC converters are centered with value 80h after power on.

#### DDC & IIC Interface

##### i) DDC1/DDC2x Mode, DDCRAM1/DDCRAM2 and SlaveA1/SlaveA2 Block

The MTV512M supports VESA DDC for both D-sub and DVI interfaces through HSCL1/HSDA1 and HSCL2/HSDA2 pins. The HSCL1/HSDA1 pins access DDCRAM1 by SlaveA1, and the HSCL2/HSDA2 pins access DDCRAM2 by SlaveA2. The MTV512M enters DDC1 mode for both DDC channels after Reset. In this mode, VSYNC is used as data clock. The HSCL1/HSCL2 pin should remain at high. The data output to the HSDA1/HSDA2 pin is taken from a shift register in MTV512M. The shift register automatically fetches EDID

data from the lower 128 bytes of the Dual Port RAM (DDCRAM1/DDCRAM2), then sends it in 9-bit packet formats inclusive of a null bit (=1) as packet separator. S/W may enable/disable the DDC1 function by setting/clearing the DDC1en control bit.

The MTV512M switches to DDC2x mode when it detects a high to low transition on the HSCL1/HSCL2 pin. In this mode, the SlaveA1/SlaveA2 IIC block automatically transmits/receives data to/from the IIC Master. The transmitted/received data is taken-from/saved-to the DDCRAM1/DDCRAM2. In simple words, MTV512M can behave as two 24LC0x EEPROMs. The only thing S/W needs to do is to write the EDID data to DDCRAM1/DDCRAM2. These slave addresses of SlaveA1/SlaveA2 block can be chosen by S/W as 5-bit, 6-bit or 7-bit. For example, if S/W chooses 5-bit slave address as 10100b, the SlaveA1 IIC block then responds to slave address 10100xb. The SlaveA1/SlaveA2 can be enabled/disabled by setting/clearing the EnslvA1/EnslvA2 bit. The DDCRAM1/DDCRAM2 can/cannot be written by the IIC Master by setting/clearing the EN128w bit.

The MTV512M returns to DDC1 mode if HSCL1 is kept high for 128 VSYNC clock period. However, it locks in DDC2B mode if a valid IIC address (1010xxxb) has been detected on HSCL1/HSDA1 buses. The DDC2 flag reflects the current DDC status, S/W may clear it by writing a "0" to it.

## ii) SlaveB Block

The SlaveB IIC block is connected to HSDA1 and HSCL1 pins only. This block can receive/transmit data using IIC protocols. S/W may write the SLVBADR register to determine the slave addresses.

In receive mode, the block first detects IIC slave address matching the condition then issues a SlvBMI interrupt. The data from HSDA1 is shifted into shift register then written to RCBBUF register when a data byte is received. The first byte loaded is word address (slave address is dropped). This block also generates a RCBI (receives buffer full interrupt) every time when the RCBBUF is loaded. If S/W is not able to read out the RCBBUF in time, the next byte in shift register is not written to RCBBUF and the slave block returns NACK to the master. This feature guarantees the data integrity of communication. The WadrB flag can tell S/W whether the data in RCBBUF is a word address or not.

In transmit mode, the block first detects IIC slave address matching the condition, then issues a SlvBMI interrupt. In the meantime, the data pre-stored in the TXBBUF is loaded into shift register, resulting in TXBBUF emptying and generates a TXBI (transmit buffer empty interrupt). S/W should write the TXBBUF a new byte for the next transfer before shift register empties. A failure of this process causes data corruption. The TXBI occurs every time when shift register reads out the data from TXBBUF.

The SlvBMI is cleared by writing "0" to corresponding bit in INTFLG register. The RCBI is cleared by reading out RCBBUF. The TXBI is cleared by writing TXBBUF.

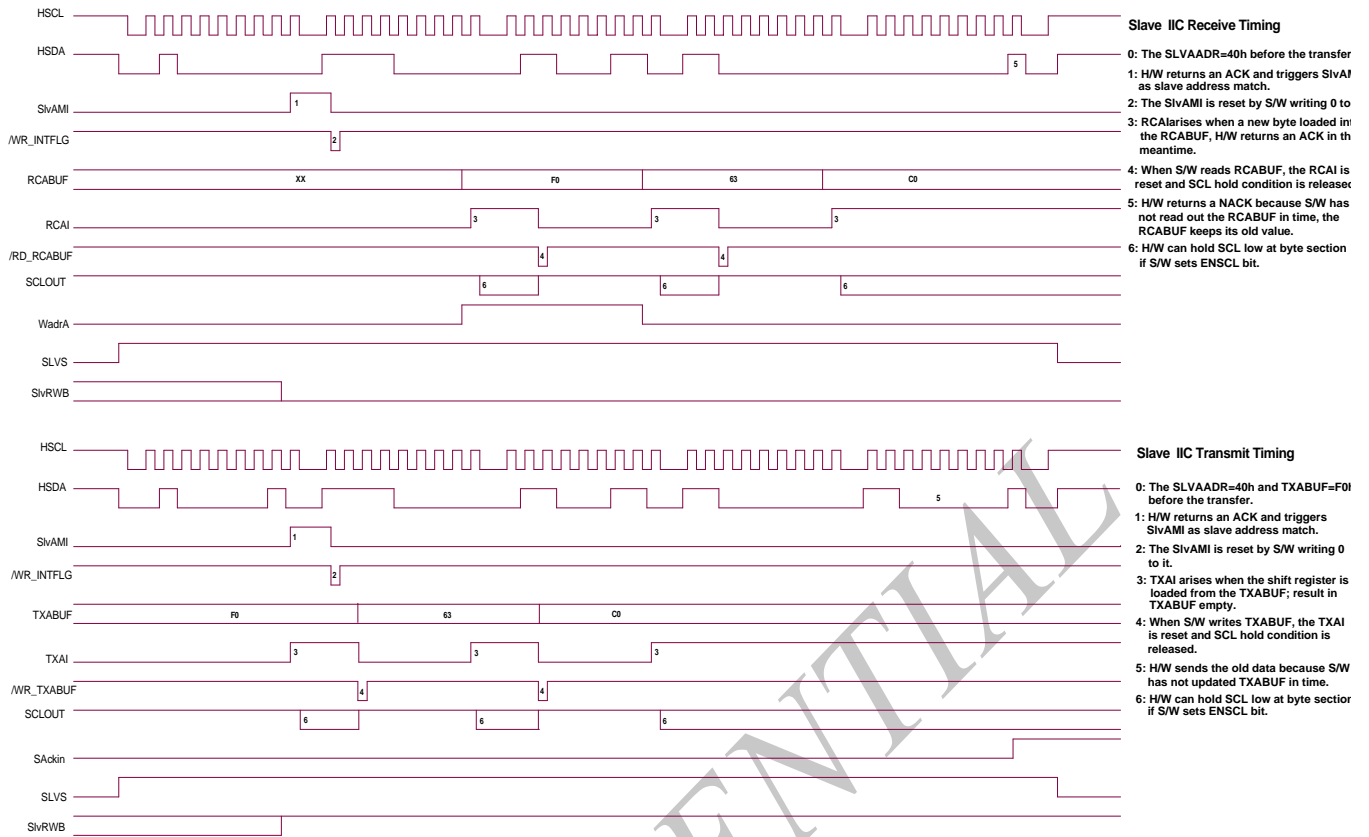


Figure 1. Slave IIC Timing Diagram (Transmit and Receive)

Slave Transmission Timing in Writing Mode

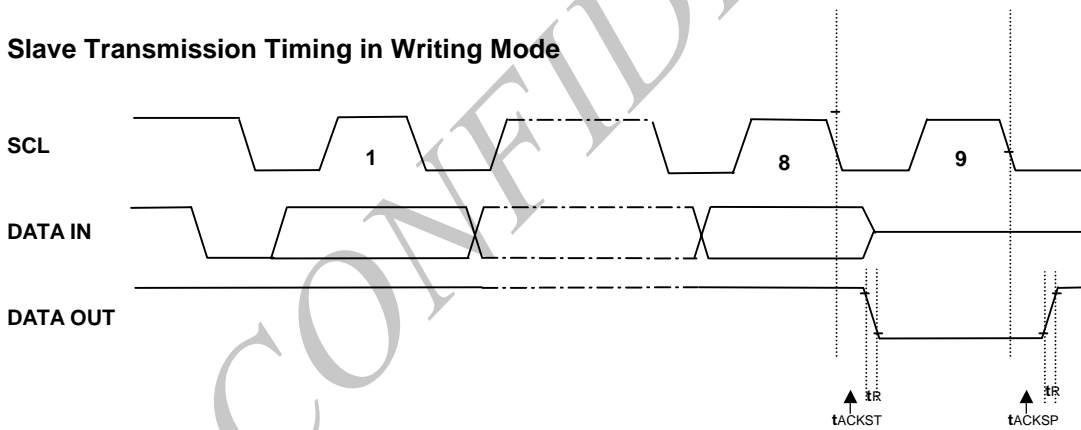
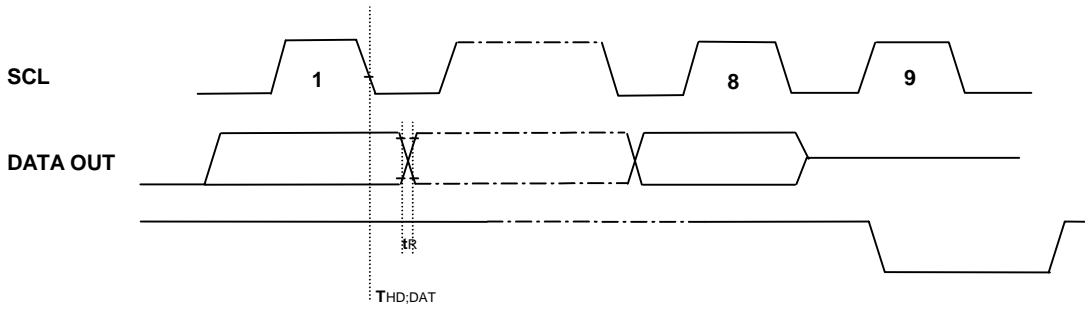


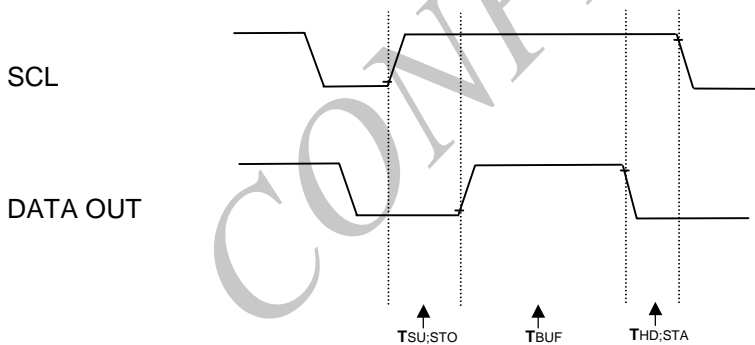
Figure 2. Slave Ack Timing in Write Mode


**Figure 3. Slave Data Transmission Timing in Read Mode**

| Parameter   | Symbol  | time            |            |
|---|---------|-----------------|------------|
|   |         | min             | max        |
| Time interval from SCL falling** edge (under VIL) to data starting to update (10% or 90% swing) | tHD;DAT | 2 x sysclk<br>* | 3 x sysclk |
| Time interval from SCL falling edge (under VIL) to slave starting to update (10% swing)         | tACKST  | 2 x sysclk      | 3 x sysclk |
| Time interval from SCL falling edge (under VIL) to slave starting to update (10% swing)         | tACKSP  | 2 x sysclk      | 3 x sysclk |
| SDA rise time by slave IIC (10% to 90% swing)   | tR      | 123.9ns         | 127.1ns    |
| SDA fall time by slave IIC (90% to 90% swing)   | tF      | 0.85ns          | 2.79ns     |

\*sysclk is the clock input on X1. It is 83ns for 12MHz crystal.

\*\*SCL falling means when SCL drop below VIL of IIC PAD, which is 1.0 volt in typical case.

**Acceptable IIC start/stop Timing**

**Figure 4. Acceptable IIC Start/Stop Timing**

| Parameter  | Symbol  | Min    | Max |
|--|---------|--------|-----|
| Time interval from SCL rising edge (over VIH) to SDA rising edge (10% swing) | tSU;STO | 600ns  | -   |
| Time interval from SDA rising edge to SCL falling edge (90% swing)           | tHD;STA | 600ns  | -   |
| Bus free time between stop and start (from 90% to 90%)                       | tBUF    | 1300ns | -   |

| swing)   |            |                             |                      |         |        |         |          |          |          |
|----------|------------|-----------------------------|----------------------|---------|--------|---------|----------|----------|----------|
| Reg name | addr       | bit7                        | bit6                 | bit5    | bit4   | bit3    | bit2     | bit1     | bit0     |
| IICCTR   | F00h (r/w) | DDC2A1                      | DDC2A2               |         |        |         |          |          |          |
| IICSTUS  | F01h (r)   | WadrB                       |                      | SlvRWB  | SAckIn | SLVS    |          |          |          |
| INTFLG   | F03h (r)   | TXBI                        | RCBI                 | SlvBMI  | STOPI  | ReStal  | WslvA1I  | WslvA2I  |          |
| INTFLG   | F03h (w)   |                             |                      | SlvBMI  | STOPI  | ReStal  | WslvA1I  | WslvA2I  |          |
| INTEN    | F04h (w)   | ETXBI                       | ERCBI                | ESlvBMI | ESTOPI | EReStal | EWSlvA1I | EWSlvA2I |          |
| DDCCTRA1 | F06h (w)   | DDC1en                      | En128W               | Rev0    | Rev1   |         |          | SlvA1bs1 | SlvA1bs0 |
| SLVA1ADR | F07h (w)   | ENSlvA1                     | Slave A1 IIC address |         |        |         |          |          |          |
| RCBBUF   | F08h (r)   | Slave B IIC receive buffer  |                      |         |        |         |          |          |          |
| TXBBUF   | F08h (w)   | Slave B IIC transmit buffer |                      |         |        |         |          |          |          |
| SLVBADR  | F09h (w)   | ENSlvB                      | Slave B IIC address  |         |        |         |          |          |          |
| CTRSLVB  | F0Ah (r)   |                             |                      |         |        |         |          | SlvBa1   | SlvBa0   |
| CTRSLVB  | F0Ah (w)   |                             |                      |         |        |         |          | SlvBbs1  | SlvBbs0  |
| DDCCTRA2 | F86h (w)   | DDC1en                      | En128W               | Rev0    | Rev1   |         |          | SlvA2bs1 | SlvA2bs0 |
| SLVA2ADR | F87h (w)   | ENSlvA2                     | Slave A2 IIC address |         |        |         |          |          |          |

**IICCTR** (r/w) : IIC interface status/control register.

- DDC2A1 = 1 → DDC2 is active for HSCL1/HSDA1 pins.
- = 0 → MTV512M remains in DDC1 mode for HSCL1/HSDA1 pins.
- DDC2A2 = 1 → DDC2 is active for HSCL2/HSDA2 pins.
- = 0 → MTV512M remains in DDC1 mode for HSCL2/HSDA2 pins.

**IICSTUS** (r) : IIC interface status register.

- WadrB = 1 → The data in RCBBUF is word address.
- SlvRWB = 1 → Current transfer is slave transmit
- = 0 → Current transfer is slave receive
- SAckIn = 1 → The external IIC host respond NACK.
- SLVS = 1 → The slave block has detected a START, cleared when STOP detected.

**INTFLG** (w) : Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

- SlvBMI = 1 → No action.
- = 0 → Clears SlvBMI flag.
- STOPI = 1 → No action.
- = 0 → Clears STOPI flag.
- ReStal = 1 → No action.

- = 0 → Clears ReStal flag.
- WslvA1I = 1 → No action.
- = 0 → Clears WslvA1I flag.
- WslvA2I = 1 → No action.
- = 0 → Clears WslvA2I flag.
- MbufI = 1 → No action.
- = 0 → Clears Master IIC bus interrupt flag (MbufI).

**INTFLG (r) :** Interrupt flag.

- TXBI = 1 → Indicates the TXBBUF need a new data byte, cleared by writing TXBBUF.
- RCBI = 1 → Indicates the RCBBUF has received a new data byte, cleared by reading RCBBUF.
- SlvBMI = 1 → Indicates the slave IIC address B match condition.
- STOPI = 1 → Indicates the slave IIC has detected a STOP condition for HSCL1/HSDA1 pins.
- ReStal = 1 → Indicates the slave IIC has detected a repeat START condition for HSCL1/HSDA1 pins.
- WslvA1I = 1 → Indicates the slave A1 IIC has detected a STOP condition of write mode.
- WslvA2I = 1 → Indicates the slave A2 IIC has detected a STOP condition of write mode.

**INTEN (w) :** Interrupt enable.

- ETXBI = 1 → Enables TXBBUF interrupt.
- ERCBI = 1 → Enables RCBBUF interrupt.
- ESlvBMI = 1 → Enables slave address B match interrupt.
- ESTOPI = 1 → Enables IIC bus STOP interrupt.
- EReStal = 1 → Enables IIC bus repeat START interrupt.
- EWSlvA1I = 1 → Enables slave A1 IIC bus STOP of write mode interrupt.
- EWSlvA2I = 1 → Enables slave A2 IIC bus STOP of write mode interrupt.

**DDCCTRA1 (w) :** DDC interface control register for HSCL1, HSDA1 pins.

- DDC1en = 1 → Enables DDC1 data transfer in DDC1 mode.
- = 0 → Disables DDC1 data transfer in DDC1 mode.
- En128W = 1 → The 128 bytes of DDCRAM1 can be written by IIC master.
- = 0 → The 128 bytes of DDCRAM1 cannot be written by IIC master.
- Rev0 = 1 → reserved
- = 0 → Normal operation.
- Rev1 = 1 → Normal operation.
- = 0 → reserved
- SlvA1bs1, SlvA1bs0 : Slave IIC block A1's slave address length.
  - = 1,0 → 5-bit slave address.
  - = 0,1 → 6-bit slave address.
  - = 0,0 → 7-bit slave address.

**SLVA1ADR (w) :** Slave IIC block A1's enable and address.

- EnslvA1 = 1 → Enables slave IIC block A1.
- = 0 → Disables slave IIC block A1.



bit6-0 : Slave IIC address A1 to which the slave block should respond.

**RCBBUF** (r) : Slave IIC block B receives data buffer.

**TXBBUF** (w) : Slave IIC block B transmits data buffer.

**SLVBADR** (w) : Slave IIC block B's enable and address.

ENslvB = 1 → Enables slave IIC block B.

= 0 → Disables slave IIC block B.

bit6-0 : Slave IIC address B to which the slave block should respond.

**CTRLVB** (r/w) : Slave IIC block B's Control registers.

SlvBbs1,SlvBbs0 : Slave IIC block B's slave address length.

= 1,0 → 5-bit slave address.

= 0,1 → 6-bit slave address.

= 0,0 → 7-bit slave address.

SlavBa1 : Bit1 of received Slave B IIC address.

SlavBa0 : Bit0 of received Slave B IIC address.

**DDCCTRA2** (w) : DDC interface control register for HSCL2, HSDA2 pins.

DDC1en = 1 → Enables DDC1 data transfer in DDC1 mode.

= 0 → Disables DDC1 data transfer in DDC1 mode.

En128W = 1 → The 128 bytes of DDCRAM2 can be written by IIC master.

= 0 → The 128 bytes of DDCRAM2 cannot be written by IIC master.

Rev0 = 1 → reserved

= 0 → Normal operation.

Rev1 = 1 → Normal operation.

= 0 → reserved

SlvA2bs1,SlvA2bs0 : Slave IIC block A2's slave address length.

= 1,0 → 5-bit slave address.

= 0,1 → 6-bit slave address.

= 0,0 → 7-bit slave address.

**SLVA2ADR** (w) : Slave IIC block A2's enable and address.

EnslvA2= 1 → Enables slave IIC block A2.

= 0 → Disables slave IIC block A2.

bit6-0 : Slave IIC address A2 to which the slave block should respond.

## A/D converter

The MTV512M is equipped with 4 VDD range 6-bit A/D converters. The ADC conversion range is from VSS to VDD, S/W can select the current convert channel by setting the SADC1/SADC0 bit. The refresh rate for the ADC is OSC freq./2304 (192us for 12MHz X'tal).

The ADC compares the input pin voltage with internal  $VDD \cdot N / 64$  voltage (where  $N = 0 - 63$ ). The ADC output value is N when pin voltage is greater than  $VDD \cdot N / 64$  and smaller than  $VDD \cdot (N+1) / 64$ .

| Reg name | addr     | bit7               | bit6 | bit5 | bit4 | bit3  | bit2  | bit1  | bit0  |
|----------|----------|--------------------|------|------|------|-------|-------|-------|-------|
| ADC      | F10h (w) | ENADC              |      |      |      | SADC3 | SADC2 | SADC1 | SADC0 |
| ADC      | F10h (r) | ADC convert result |      |      |      |       |       |       |       |
| WDT      | F18h (w) | WEN                | WCLR |      |      |       | WDT2  | WDT1  | WDT0  |

### Low Power Reset (LVR) & Watchdog Timer

When the voltage level of power supply is below 2.4V (+/-0.4V) for a specific period of time, the LVR generates a chip reset signal. After the power supply is above 2.4V (+/-0.4V), LVR maintains in reset state for 144 X'tal cycle to guarantee the chip exit reset condition with a stable X'tal oscillation. The Watchdog Timer automatically generates a device reset when it is overflowed. The interval of overflow is 0.25 sec x N, when N is a number from 1 to 8, and can be programmed via register WDT (2:0). The timer function is disabled after power on reset, users can activate this function by setting WEN, and clear the timer by setting WCLR.

**WDT (w) :** Watchdog Timer control register.

|            |     |                                     |
|------------|-----|-------------------------------------|
| WEN        | = 1 | → Enables Watchdog Timer.           |
| WCLR       | = 1 | → Clears Watchdog Timer.            |
| WDT2: WDT0 | = 0 | → Overflow interval = 8 x 0.25 sec. |
|            | = 1 | → Overflow interval = 1 x 0.25 sec. |
|            | = 2 | → Overflow interval = 2 x 0.25 sec. |
|            | = 3 | → Overflow interval = 3 x 0.25 sec. |
|            | = 4 | → Overflow interval = 4 x 0.25 sec. |
|            | = 5 | → Overflow interval = 5 x 0.25 sec. |
|            | = 6 | → Overflow interval = 6 x 0.25 sec. |
|            | = 7 | → Overflow interval = 7 x 0.25 sec. |

**ADC (w) :** ADC control.

|       |     |                           |
|-------|-----|---------------------------|
| ENADC | = 1 | → Enables ADC.            |
| SADC0 | = 1 | → Selects ADC0 pin input. |
| SADC1 | = 1 | → Selects ADC1 pin input. |
| SADC2 | = 1 | → Selects ADC2 pin input. |
| SADC3 | = 1 | → Selects ADC3 pin input. |

**ADC (r) :** ADC convert result.

### Etimer

The Etimer is a 16-bit Timer/Counter which provide capture/reload functions like timer2 in 8052. The type is selected by C/T2 in the SFRETCTR. Etimer has 2 modes, capture/auto-reload (up or down counting). The modes are selected by CP/RLS in ETCTR. Etimer contains two 8-bit registers, TLET and THET. When it is used in the timer mode, THET-TLET count rate is 1/12 of the oscillator frequency. In the counter mode, the counter is incremented when 1 → 0 transition at Port 1.0,

#### 1. Capture mode

In the capture mode, if EXEN2 = 0, Etimer is a 16-bit timer or counter. When EXEN2 = 0, Etimer counters up to FFFFh and then set TF2 upon overflow. This bit will generate an interrupt (INT1) to 8051. If EXEN2 = 1, Etimer capture the current value in THET-TLET into RCAPETH-RCAPETL, respectively when 1 → 0 transition at Port. 1.1. This will also generate an interrupt.

#### 2. Auto-reload mode

Etimer can be programmed to count-up or down when in auto-reload mode. This feature is selected by DCEN in SFR ETMOD. If EXEN2 = 0, Etimer counts up to 0FFFFh and then set TF2 (overflow). At this mode, the counter is reloaded the 16-bit value from RCAPETH-RCAPETL. If EXEN2 = 1, the reload function can be triggered by overflow or by 1 → 0 transition at Port 1.1.

|       |          |     |      |   |   |       |     |      |        |
|-------|----------|-----|------|---|---|-------|-----|------|--------|
| ETCTR | F88h (w) | TF2 | EXF2 | - | - | EXEN2 | TR2 | C/T2 | CP/RL2 |
|-------|----------|-----|------|---|---|-------|-----|------|--------|

|          |          |         |      |       |  |       |     |      |        |
|----------|----------|---------|------|-------|--|-------|-----|------|--------|
|          | F88h (r) | TF2     | EXF2 |       |  | EXEN2 | TR2 | C/T2 | CP/RL2 |
| ETMOD    | F89h (w) |         |      |       |  |       |     |      | DCEN   |
|          | F89h (r) |         |      |       |  |       |     |      | DCEN   |
| THET     | F8Ah (w) | THET    |      |       |  |       |     |      |        |
|          | F8Ah (r) | THET    |      |       |  |       |     |      |        |
| TLET     | F8Bh (w) | TLET    |      |       |  |       |     |      |        |
|          | F8Bh (r) | TLET    |      |       |  |       |     |      |        |
| RCAPETH  | F8Ch (w) | RCAPETH |      |       |  |       |     |      |        |
|          | F8Ch (r) | RCAPETH |      |       |  |       |     |      |        |
| RCAPETL  | F8Dh (w) | RCAPETL |      |       |  |       |     |      |        |
|          | F8Dh (r) | RCAPETL |      |       |  |       |     |      |        |
| EINT1PEN | F8Eh (w) | EEINT1  | ETE  | TSTP1 |  |       |     |      |        |

**ETCTR (w):** Etimer control register

- TF2 =1 → No actions  
 =0 → Clear Etimer overflow interrupt
- EXF2 =1 → No actions  
 =0 → Clear Etimer external capture / reload interrupt
- EXEN2 =1 → Enable Port 1.1 capture / reload trigger  
 =0 → Disable Port 1.1 capture / reload trigger
- TR2 =1 → Enable Etimer  
 =0 → Disable Etimer
- C/T2 =1 → Etimer functions as a counter  
 =0 → Etimer functions as a timer
- CP/RL2 =1 → Set Etimer in Capture mode  
 =0 → Set Etimer in Auto-reload mode

**ETCTR (r):** Etimer control register

- TF2 = → TF2 state
- EXF2 = → EXF2 state
- EXEN2 = → EXEN2 state
- TR2 = → TR2 state
- C/T2 = → CT2 state
- CP/RL2 = → CP/RL2 state

**THET (w/r):** Etimer high 8-bit register

**TLET (w/r):** Etimer low 8-bit register

**RCAPETH(w/r):** Etimer high 8-bit capture/reload register

**RCAPETL(w/r):** Etimer high 8-bit capture/reload register

**EINT1PEN(w):** External interrupt control

- ETINT1 (w): =1 → Enable P3.3 as external interrupt1 trigger  
 =0 → Disable P3.3 as external interrupt1 trigger
- ETE (w): =1 → Enable Etimer interrupt  
 =0 → Disable Etimer interrupt
- TSTP1 (w): =1 → Reserved  
 =0 → Normal operation

**VSYNC Interrupt**

The MTV512M checks the VSYNC input pulse and generates an interrupt at its leading edge. The VSYNC flag is set each time when MTV512M detects a VSYNC pulse. The flag is cleared by S/W writing a "0".

|        |           |  |  |  |  |  |  |  |        |
|--------|-----------|--|--|--|--|--|--|--|--------|
| INTFLG | F48h(r/w) |  |  |  |  |  |  |  | Vsync  |
| INTEN  | F49h(w)   |  |  |  |  |  |  |  | EVsync |

INTFLG(w): Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the INT1 source of 8051 core will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

Vsync = 1 → No action.

= 0 → Clears VSYNC interrupt flag.

INTFLG(r): Interrupt flag.

Vsync = 1 → Indicates a VSYNC interrupt.

INTEN(w): Interrupt enable.

EVsync = 1 → Enables VSYNC interrupt.

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## Memory Map of XFR

| Reg name | addr       | bit7                         | bit6                | bit5    | bit4   | bit3    | bit2    | bit1     | bit0    |
|----------|------------|------------------------------|---------------------|---------|--------|---------|---------|----------|---------|
| IICCTR   | F00h (r/w) | DDC2A1                       | DDC2A2              |         |        |         |         |          |         |
| IICSTUS  | F01h (r)   | WadrB                        |                     | SlvRWB  | SAckIn | SLVS    |         |          |         |
| INTFLG   | F03h (r)   | TXBI                         | RCBI                | SlvBMI  | STOPI  | ReStal  | WSlvAI  | WslvA2I  |         |
| INTFLG   | F03h (w)   |                              |                     | SlvBMI  | STOPI  | ReStal  | WSlvAI  | WslvA2I  |         |
| INTEN    | F04h (w)   | ETXBI                        | ERCBI               | ESlvBMI | ESTOPI | EReStal | EWSlvA1 | EWSlvA2I |         |
| DDCCTRA1 | F06h (w)   | DDC1en                       | En128W              | Rev0    | Rev1   |         |         | SlvAbs1  | SlvAbs0 |
| SLVA1ADR | F07h (w)   | ENSlvA                       | Slave A IIC address |         |        |         |         |          |         |
| RCBBUF   | F08h (r)   | Slave B IIC receives buffer  |                     |         |        |         |         |          |         |
| TXBBUF   | F08h (w)   | Slave B IIC transmits buffer |                     |         |        |         |         |          |         |
| SLVBADR  | F09h (w)   | ENSlvB                       | Slave B IIC address |         |        |         |         |          |         |
| CTRSLVB  | F0Ah (r)   |                              |                     |         |        |         |         | SlvBa1   | SlvBa0  |
| CTRSLVB  | F0Ah (w)   |                              |                     |         |        |         |         | SlvBbs1  | SlvBbs0 |
| ADC      | F10h (w)   | ENADC                        |                     |         |        | SADC3   | SADC2   | SADC1    | SADC0   |
| ADC      | F10h (r)   | ADC convert Result           |                     |         |        |         |         |          |         |
| WDT      | F18h (w)   | WEN                          | WCLR                |         |        |         | WDT2    | WDT1     | WDT0    |
| DA0      | F20h(r/w)  | Pulse width of PWM DAC 0     |                     |         |        |         |         |          |         |
| DA1      | F21h(r/w)  | Pulse width of PWM DAC 1     |                     |         |        |         |         |          |         |
| DA2      | F22h(r/w)  | Pulse width of PWM DAC 2     |                     |         |        |         |         |          |         |
| DA3      | F23h(r/w)  | Pulse width of PWM DAC 3     |                     |         |        |         |         |          |         |
| DA4      | F24h(r/w)  | Pulse width of PWM DAC 4     |                     |         |        |         |         |          |         |
| DA5      | F25h(r/w)  | Pulse width of PWM DAC 5     |                     |         |        |         |         |          |         |
| PORT5    | F30h(r/w)  |                              |                     |         |        |         |         |          | P50     |
| PORT5    | F31h(r/w)  |                              |                     |         |        |         |         |          | P51     |
| PORT5    | F32h(r/w)  |                              |                     |         |        |         |         |          | P52     |
| PORT5    | F33h(r/w)  |                              |                     |         |        |         |         |          | P53     |
| PORT5    | F34h(r/w)  |                              |                     |         |        |         |         |          | P54     |
| PORT5    | F35h(r/w)  |                              |                     |         |        |         |         |          | P55     |
| PORT5    | F36h(r/w)  |                              |                     |         |        |         |         |          | P56     |
| PORT6    | F38h(r/w)  |                              |                     |         |        |         |         |          | P60     |
| PORT6    | F39h(r/w)  |                              |                     |         |        |         |         |          | P61     |
| PORT6    | F3Ah(r/w)  |                              |                     |         |        |         |         |          | P62     |
| PORT6    | F3Bh(r/w)  |                              |                     |         |        |         |         |          | P63     |
| PORT6    | F3Ch(r/w)  |                              |                     |         |        |         |         |          | P64     |
| PORT6    | F3Dh(r/w)  |                              |                     |         |        |         |         |          | P65     |
| PORT6    | F3Eh(r/w)  |                              |                     |         |        |         |         |          | P66     |
| PORT6    | F3Fh(r/w)  |                              |                     |         |        |         |         |          | P67     |
| PADMOD   | F50h(w)    | DA13E                        | DA12E               | DA11E   | DA10E  | AD3E    | AD2E    | AD1E     | AD0E    |
| PADMOD   | F51h(w)    | P57E                         | P56E                | P55E    | P54E   | P53E    | P52E    | P51E     | P50E    |

|          |           |         |                      |        |       |       |       |              |              |  |
|----------|-----------|---------|----------------------|--------|-------|-------|-------|--------------|--------------|--|
| PADMOD   | F52h(w)   | HIIC1E  | IIICE                | HIIC2E | CKOE  |       |       |              |              |  |
| PADMOD   | F53h(w)   | P57oe   | P56oe                | P55oe  | P54oe | P53oe | P52oe | P51oe        | P50oe        |  |
| PADMOD   | F54h(w)   | P67oe   | P66oe                | P65oe  | P64oe | P63oe | P62oe | P61oe        | P60oe        |  |
| PADMOD   | F55h(w)   | COP17   | COP16                | COP15  | COP14 | COP13 | COP12 | COP11        | COP10        |  |
| OPTION   | F56h(w)   | PWMF    | DIV253               | FclkE  | DCLK  | ENSCL |       |              | IP77E        |  |
| PADMOD   | F5Eh(w)   |         | P76E                 |        |       |       |       |              |              |  |
| PADMOD   | F5Fh(w)   | P77oe   | P76oe                |        |       |       |       |              |              |  |
| PORT7    | F76h(r/w) |         |                      |        |       |       |       |              | P76          |  |
| PORT7    | F77h(r/w) |         |                      |        |       |       |       |              | P77          |  |
| DDCCTRA2 | F86h (w)  | DDC1en  | En128W               | Rev0   | Rev1  |       |       | SlvA2bs<br>1 | SlvA2bs<br>0 |  |
| SLVA2ADR | F87h (w)  | ENSlvA2 | Slave A2 IIC address |        |       |       |       |              |              |  |
|          |           |         |                      |        |       |       |       |              |              |  |
| ETCTR    | F88h (w)  | TF2     | EXF2                 | RCLK   | TCLK  | EXEN2 | TR2   | C/T2         | CP/RL2       |  |
|          | F88h (r)  | TF2     | EXF2                 | RCLK   | TCLK  | EXEN2 | TR2   | C/T2         | CP/RL2       |  |
| ETMOD    | F89h (w)  |         |                      |        |       |       |       |              | DCEN         |  |
|          | F89h (r)  |         |                      |        |       |       |       |              | DCEN         |  |
|          | F8Ah (w)  | THET    |                      |        |       |       |       |              |              |  |
|          | F8Ah (r)  | THET    |                      |        |       |       |       |              |              |  |
|          | F8Bh (w)  | TLET    |                      |        |       |       |       |              |              |  |
|          | F8Bh (r)  | TLET    |                      |        |       |       |       |              |              |  |
|          | F8Ch (w)  | RCAPETH |                      |        |       |       |       |              |              |  |
|          | F8Ch (r)  | RCAPETH |                      |        |       |       |       |              |              |  |
|          | F8Dh (w)  | RCAPETL |                      |        |       |       |       |              |              |  |
|          | F8Dh (r)  | RCAPETL |                      |        |       |       |       |              |              |  |
| EINT1PEN | F8Eh (w)  | EEINT1  | ETE                  | TSTP1  |       |       |       |              |              |  |

**ELECTRICAL PARAMETERS**
**Absolute Maximum Ratings**

at: Ta= 0 to 70 °C, VSS=0V

| Name   | Symbol | Range           | Unit |
|--|--------|-----------------|------|
| Maximum Supply Voltage                                 | VDD    | -0.3 to +3.6    | V    |
| Maximum Input Voltage (HSYNC, VSYNC & open-drain pins) | Vin1   | -0.3 to 3.3+0.3 | V    |
| Maximum Input Voltage (other pins)                     | Vin2   | -0.3 to VDD+0.3 | V    |
| Maximum Output Voltage                                 | Vout   | -0.3 to VDD+0.3 | V    |
| Maximum Operating Temperature                          | Topg   | 0 to +70        | °C   |
| Maximum Storage Temperature                            | Tstg   | -25 to +125     | °C   |

**Allowable Operating Conditions**

at: Ta= 0 to 70 °C, VSS=0V

| Name              | Symbol | Condition         | Min.      | Max.      | Unit |
|-------------------|--------|-------------------|-----------|-----------|------|
| Supply Voltage    | VDD    | 3.3V applications | 3.0       | 3.6       | V    |
| Input "H" Voltage | Vih    | 3.3V applications | 0.6 x VDD | VDD +0.3  | V    |
| Input "L" Voltage | Vil    | 3.3V applications | -0.3      | 0.3 x VDD | V    |
| Operating Freq.   | Fopg   |                   | -         | 15        | MHz  |

**DC Characteristics**

at: Ta=0 to 70 °C, VDD=3.3V, VSS=0V

| Name                                  | Symbol | Condition            | Min. | Typ. | Max. | Unit |
|---------------------------------------|--------|----------------------|------|------|------|------|
| Output "H" Voltage, open drain pin    | Voh1   | VDD=3.3V, loh=0 μA   | 2.65 |      |      | V    |
| Output "H" Voltage, 8051 I/O port pin | Voh2   | VDD=3.3V, loh=-50 μA | 2.65 |      |      | V    |
| Output "H" Voltage, CMOS output       | Voh3   | VDD=3.3V, loh=-4mA   | 2.65 |      |      | V    |
| Output "L" Voltage                    | Vol    | lol=5mA              |      |      | 0.45 | V    |
| Power Supply Current                  | Idd    | Active               |      | 18   | 24   | mA   |
|                                       |        | Idle                 |      | 1.3  | 4.0  | mA   |
|                                       |        | Power-Down           |      | 50   | 80   | μA   |
| RST Pull-Down Resistor                | Rrst   | VDD=3.3V             | 150  |      | 250  | Kohm |
| Pin Capacitance                       | Cio    |                      |      |      | 15   | pF   |

**AC Characteristics**

at: Ta=0 to 70 °C, VDD=3.3V, VSS=0V

| Name                          | Symbol | Condition   | Min.   | Typ. | Max.  | Unit |
|-------------------------------|--------|-------------|--------|------|-------|------|
| Crystal Frequency             | fXtal  |             |        | 12   |       | MHz  |
| PWM DAC Frequency             | fDA    | fXtal=12MHz | 46.875 |      | 94.86 | KHz  |
| HS input pulse Width          | tHIPW  | fXtal=12MHz | 0.3    |      | 7.5   | uS   |
| VS input pulse Width          | tVIPW  | fXtal=12MHz | 3      |      |       | uS   |
| HSYNC to Hblank output jitter | tHBJ   |             |        |      | 5     | nS   |
| H+V to Vblank output delay    | tVVBD  | fXtal=12MHz |        | 8    |       | uS   |
| VS pulse width in H+V signal  | tVCPW  | FXtal=12MHz | 20     |      |       | uS   |

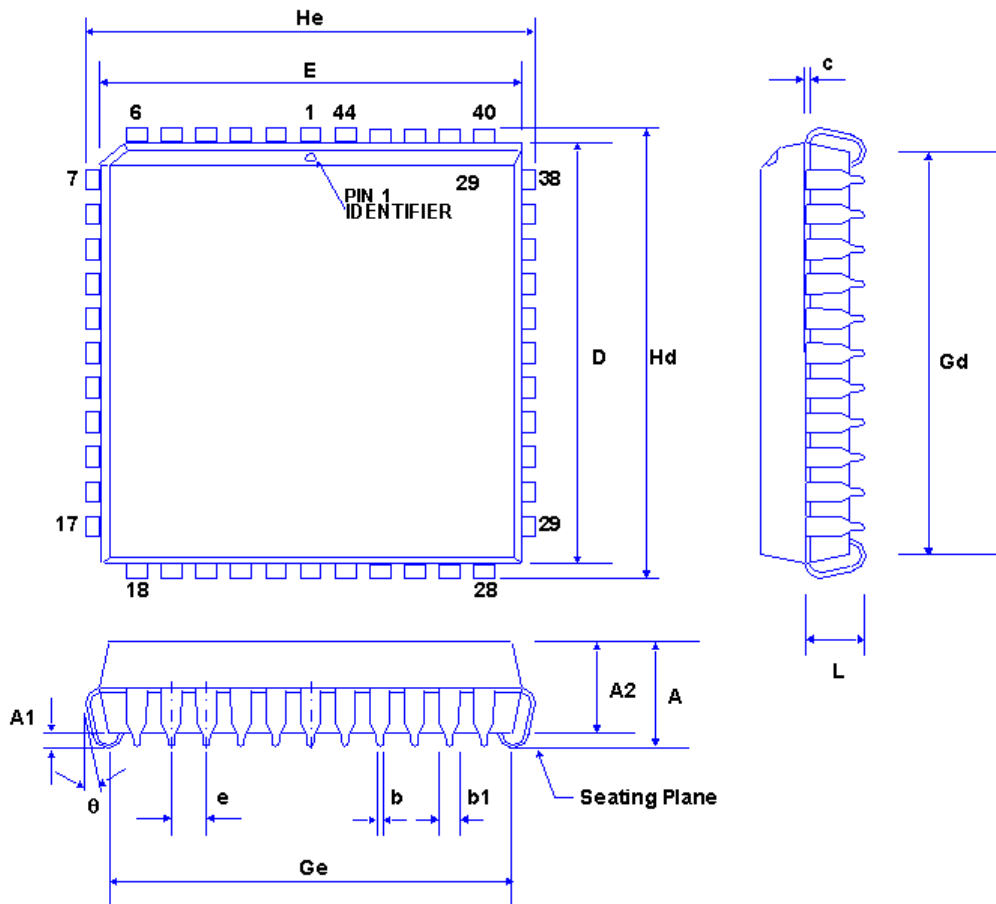
**Test Mode Condition**

In normal application, users should avoid the MTV512M entering its test mode or writer mode, outlined as follows: adding pull-up resistor to HSCL1/HSDA1/HSCL2/HSDA2 pins is recommended.

**Test Mode:** RESET's falling edge & HSCL1=0 & HSDA1 & HSCL2=0 & HSDA2 = 0

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**PACKAGE DIMENSION**
**44-pin PLCC**


| Symbol | Dimension in Millimeters |       |       | Dimension in Inches |       |       |
|--------|--------------------------|-------|-------|---------------------|-------|-------|
|        | Min                      | Nom   | Max   | Min                 | Nom   | Max   |
| A      | -                        | -     | 4.70  | -                   | -     | 0.185 |
| A1     | 0.51                     | -     | -     | 0.020               | -     | -     |
| A2     | 3.70                     | 3.80  | 3.90  | 0.145               | 0.150 | 0.155 |
| b      | 0.41                     | 0.46  | 0.56  | 0.016               | 0.018 | 0.022 |
| b1     | 0.65                     | 0.70  | 0.80  | 0.026               | 0.028 | 0.032 |
| c      | 0.18                     | 0.25  | 0.33  | 0.007               | 0.010 | 0.013 |
| D      | 16.46                    | 16.60 | 16.71 | 0.648               | 0.653 | 0.658 |
| E      | 16.46                    | 16.60 | 16.71 | 0.648               | 0.653 | 0.658 |
| e      | 1.27 (Typ)               |       |       | 0.050 (Typ)         |       |       |
| Gd     | 15.00                    | 15.50 | 16.00 | 0.590               | 0.610 | 0.630 |
| Ge     | 15.00                    | 15.50 | 16.00 | 0.590               | 0.610 | 0.630 |
| Hd     | 17.30                    | 17.50 | 17.80 | 0.680               | 0.690 | 0.700 |
| He     | 17.30                    | 17.50 | 17.80 | 0.680               | 0.690 | 0.700 |
| L      | 2.29                     | 2.54  | 2.80  | 0.090               | 0.100 | 0.110 |
|        | 0°                       | -     | 10°   | 0°                  | -     | 10°   |

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[Ordering Information](#)

## Standard Configurations:

| Prefix | Part Type | Package Type |
|--------|-----------|--------------|
| MTV    | 512M      | V: PLCC      |

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