

# SL74HC109

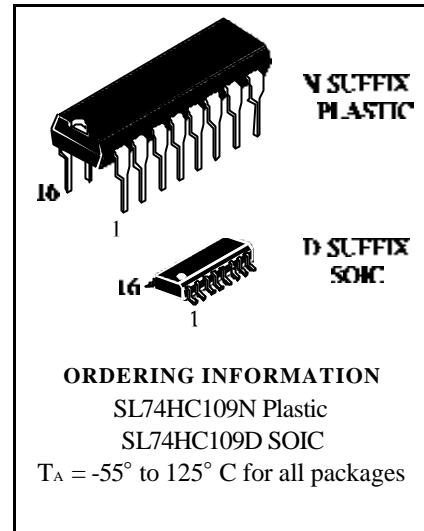
## Dual J-K Flip-Flop with Set and Reset

### High-Performance Silicon-Gate CMOS

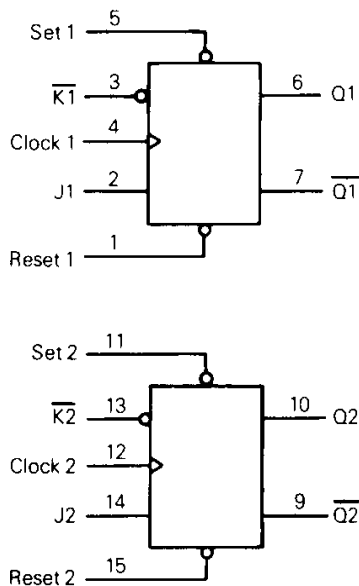
The SL74HC109 is identical in pinout to the LS/ALS109. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of two J-K flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low-to-high transition of the clock. Both Q to Q outputs are available from each flip-flop.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



### LOGIC DIAGRAM



PIN 16 = V<sub>CC</sub>  
 PIN 8 = GND

### PIN ASSIGNMENT

RESET 1	1	16	V <sub>CC</sub>
J1	2	15	RESET 2
K1	3	14	J2
CLOCK 1	4	13	K2
SET 1	5	12	CLOCK 2
Q1	6	11	SET 2
Q1-bar	7	10	Q2
GND	8	9	Q2-bar

### FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H		L	L	L	H
H	H		H	L	Toggle	
H	H		L	H	No Change	
H	H		H	H	H	L
H	H	L	X	X	No Change	

X = Don't care

\* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 +Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
 SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> = 2.0 V	0	1000	ns
	V <sub>CC</sub> = 4.5 V	0	500	
	V <sub>CC</sub> = 6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.



# SL74HC109

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55 °C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0 μA	6.0	4.0	40	80	μA

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub>=50pF, Input t<sub>r</sub>=t<sub>f</sub>=6.0 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q or Q <sup>̄</sup> (Figures 1 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Set or Reset to Q or Q <sup>̄</sup> (Figures 2 and 4)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>IN</sub>	Maximum Input Capacitance	-	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Flip-Flop)	Typical @25°C, V <sub>CC</sub> =5.0 V			pF
	Used to determine the no-load dynamic power consumption: P <sub>D</sub> =C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	40			

## TIMING REQUIREMENTS (C<sub>L</sub>=50pF, Input t<sub>r</sub>=t<sub>f</sub>=6.0 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>SU</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>H</sub>	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>REC</sub>	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>W</sub>	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	12	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	12	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	



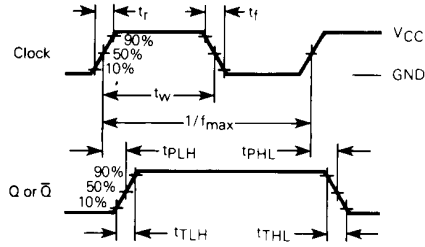


Figure 1. Switching Waveforms

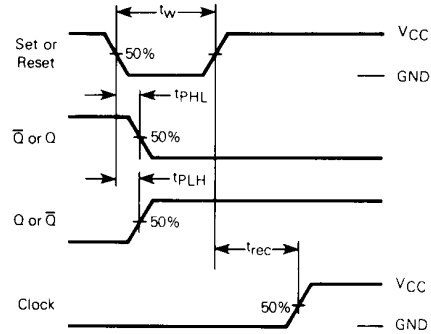


Figure 2. Switching Waveforms

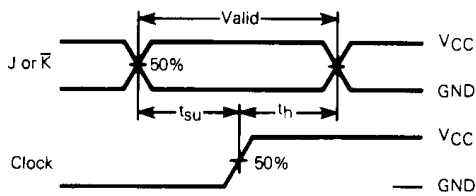
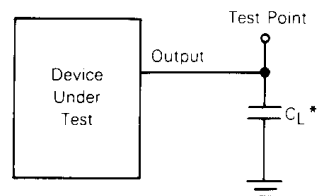


Figure 3. Switching Waveforms



\* Includes all probe and jig capacitance.

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM

