

DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μ PD35H71A

5000-BIT CCD LINEAR IMAGE SENSOR

The μ PD35H71A is a high sensitivity 5000-bit linear image sensor consisting of charge coupled devices (CCD) which changes optical images to electrical signal.

Especially, the μ PD35H71A has extra high speed CCD register, so it is suitable for high resolution scanner and facsimile which scan high definition document at high speed.

FEATURES

- Valid photocell: 5000-bit
- Photocell's pitch: 7 μ m
- Low Image Lag: Image lag is 1 % or less. One fifth of the existing equivalent NEC product (μ PD35H71).
- High response sensitivity: Providing a response three times better than the existing equivalent NEC product (μ PD3571) to the light from a day light fluorescent lamp. Equal with μ PD35H71.
- High resolution: 16 dot/mm across the shorter side of a A3-size (297 x 420 mm) sheet
- 40 MHz high speed scan: 126 μ s/line
- Peak response wavelength: 550 nm (green)
- Power supply: +12 V
- All clock signal input level: CMOS output under +5 V operation

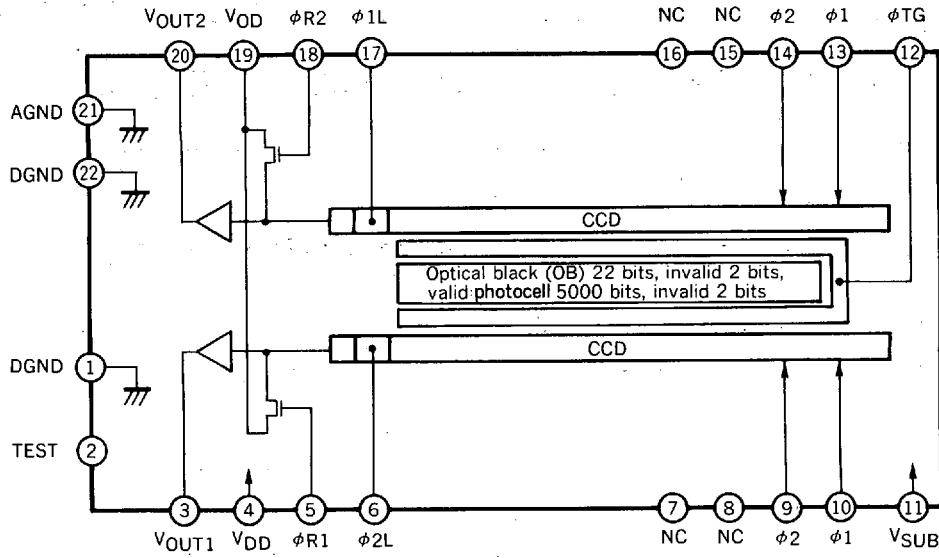
ORDERING INFORMATION

Part Number	Package	Quality Grade
μ PD35H71AD	CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

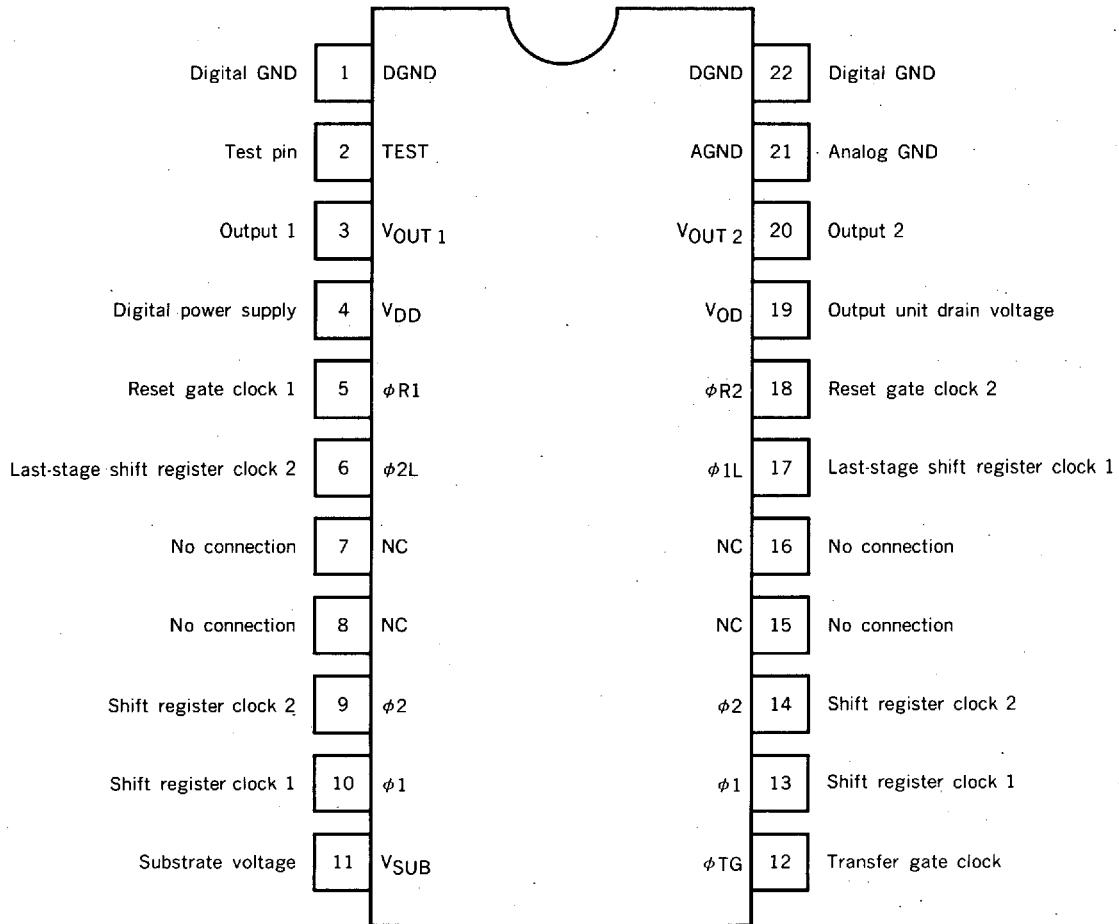
The information in this document is subject to change without notice.

BLOCK DIAGRAM

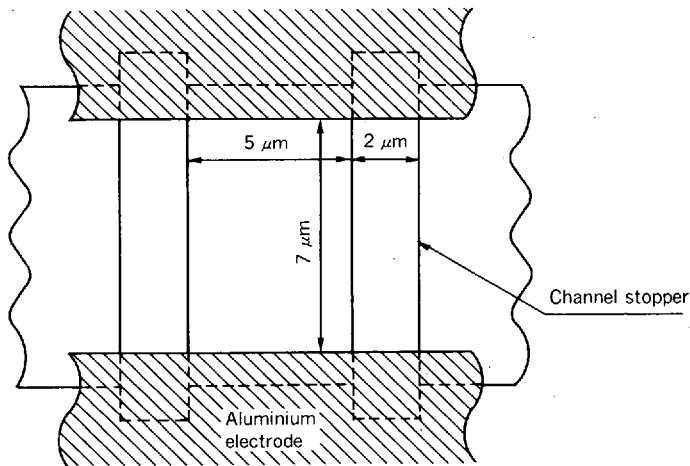


PIN CONFIGURATION (Top View)

CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)



PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

Parameter	Symbol	Ratings	Unit
Output unit drain voltage	V _{OD}	-0.3 to +15	V
Digital power supply	V _{DD}	-0.3 to +15	V
Substrate voltage	V _{SUB}	-0.3 to +15	V
Shift register clock voltage	V _{φ1,φ2}	-0.3 to +15	V
Reset signal voltage	V _{φR}	-0.3 to +15	V
Transfer gate signal voltage	V _{φTG}	-0.3 to +15	V
Operating ambient temperature	T _{opt}	-25 to +55	°C
Storage temperature	T _{stg}	-40 to +100	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -25 to +55 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output unit drain voltage	V _{OD}	11.4	12.0	12.6	V
Digital power supply	V _{DD}	11.4	12.0	12.6	V
Substrate voltage	V _{SUB}	11.4	12.0	12.6	V
Shift register clock φ1, φ1L signal high level	V _{φ1H}	4.5	5.0	5.5	V
Shift register clock φ1, φ1L signal low level	V _{φ1L}	-0.3	0	+0.5	V
Shift register clock φ2, φ2L signal high level	V _{φ2H}	4.5	5.0	5.5	V
Shift register clock φ2, φ2L signal low level	V _{φ2L}	-0.3	0	+0.5	V
Reset signal φR1 high level	V _{φR1H}	4.5	5.0	5.5	V
Reset signal φR1 low level	V _{φR1L}	-0.3	0	+0.5	V
Reset signal φR2 high level	V _{φR2H}	4.5	5.0	5.5	V
Reset signal φR2 low level	V _{φR2L}	-0.3	0	+0.5	V
Transfer gate signal high level	V _{φTGH}	4.5	5.0	5.5	V
Transfer gate signal low level	V _{φTGL}	-0.3	0	+0.5	V
Date rate	f _{φR}		2	40	MHz

- Caution**
1. Leave Test pin (pin 2) unconnected.
 2. Input reset signal φR1, φR2 to pin 5, 18 via resistor and capacitor. Concerning the connection method refer to APPLICATION CIRCUIT.
 3. Operating conditions of reset signal φR1, φR2 are not the condition at device pins but the condition of the signal which applied to resistor.

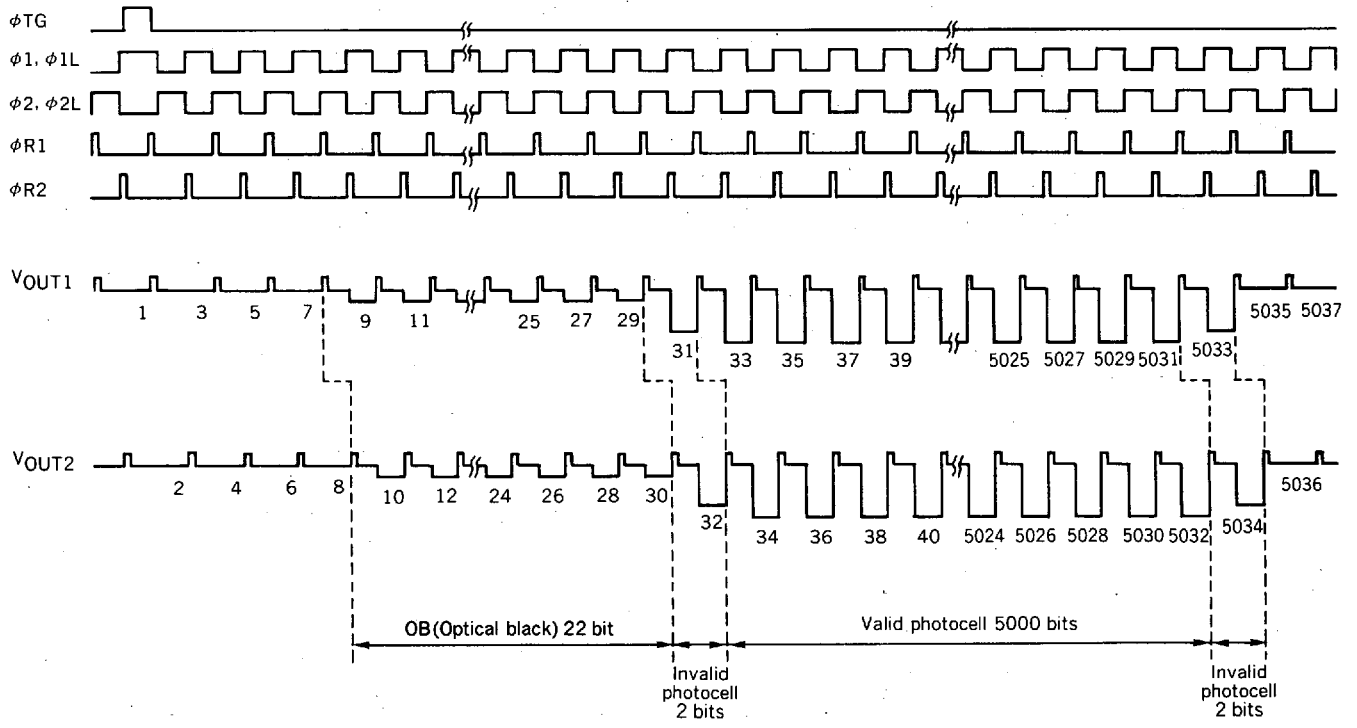
ELECTRICAL CHARACTERISTICS

$T_a = +25\text{ }^\circ\text{C}$, $V_{DD} = 12\text{ V}$, $f_{\phi 1} = 1\text{ MHz}$, data rate = 2 MHz, storage time = 10 ms,
light source = 3200 K halogen lamp +C500 (infrared cut filter), input signal clock = 5 V_{p-p}

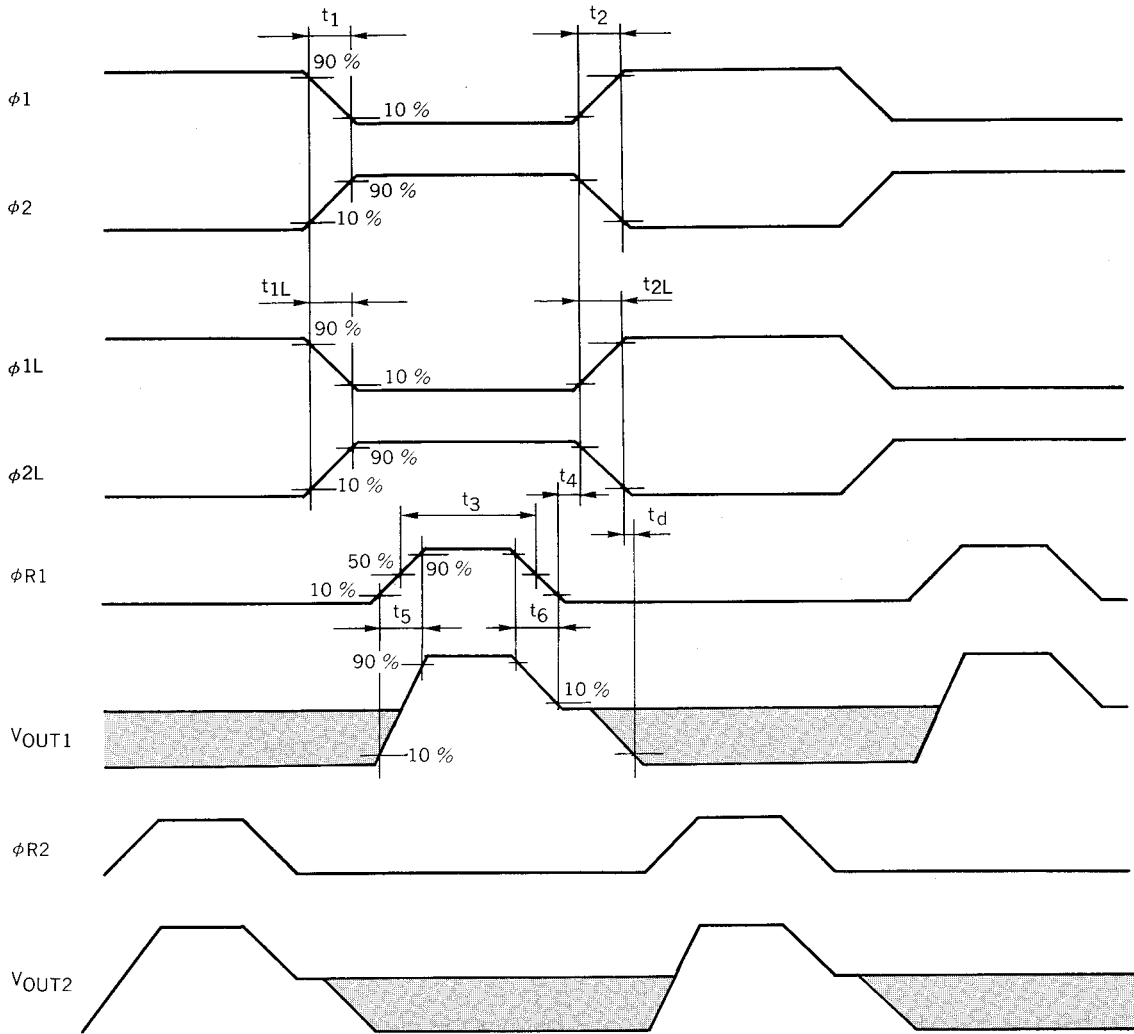
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V _{sat}		1.0	1.5		V
Saturation exposure	SE	Daylight color fluorescent lamp		0.29		lx·s
Photo response non-uniformity	PRNU	V _{OUT} = 500 mV		±5	±10	%
Average dark signal	ADS	Light shielding		1.0	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	-3	+3 -1	+6	mV
Power consumption	P _W			200		mW
Output impedance	Z _O			0.2	0.5	kΩ
Response	R _F	Daylight color fluorescent lamp	4.15	5.2	6.25	V/lx·s
Response peak wavelength				550		nm
Image lag	IL	V _{OUT} =1V		0.3	1.0	%
Offset level	V _{OS}		2.0	3.0	5.0	V
Shift register clock input capacitance	C _{φ1} C _{φ2}		400	500	800	pF
Last-stage shift register clock input capacitance	C _{φ1L} C _{φ2L}		40	50	100	pF
Reset input capacitance	C _{φR1} C _{φR2}		8	10	15	pF
Transfer gate signal input capacitance	C _{φTG}		100	150	200	pF
Output rise delay time	t _d Note	Time from 90% to 10% of φ2L fall is 5 ns.		20		ns
Register imbalance	RI	V _{OUT} = 500 mV		0	4	%
Transfer efficiency	TTE	V _{OUT} = 500 mV, f _{φR1} = 20 MHz	92	98		%
Dynamic range	DR	V _{sat} /DSNU		500		times
Reset feed through noise	RFSN	Light shielding		250	500	mV

Note t_d is defined as a time from 10 % of φ2L to 10 % of V_{OUT}, output after passing through two steps of emitter follower in the APPLICATION CIRCUIT.

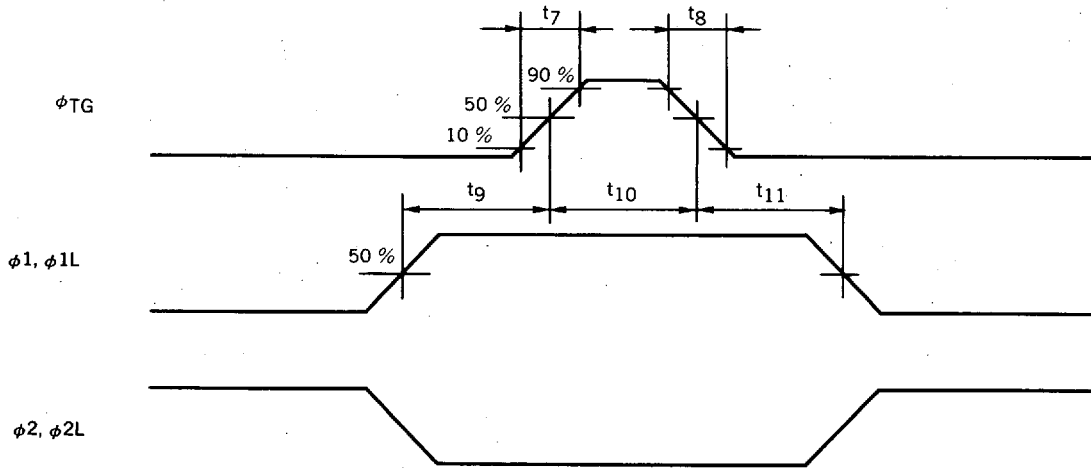
TIMING CHART 1



TIMING CHART 2



TIMING CHART 3



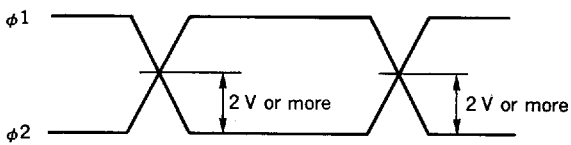
Recommended Timing

(Unit: ns)

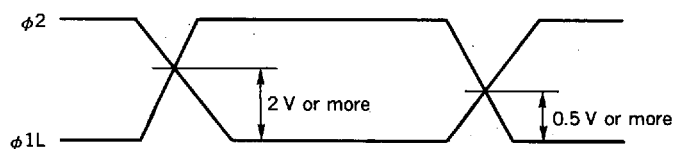
Parameter	MIN.	TYP.	MAX.
t_1, t_2	0	50	200
t_{1L}, t_{2L}	0	5	25
t_3	15	50	(500)
t_4	5	20	(500)
t_5, t_6	0	20	50
t_7, t_8	0	50	100
t_9, t_{11}	10	100	(500)
t_{10}	1000	2000	(5000)

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μ PD35H71A is destroyed.

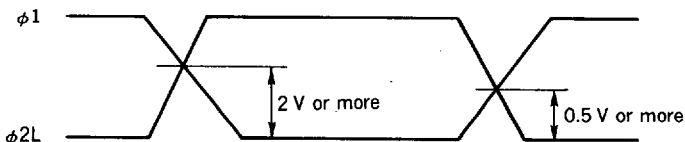
CROSS POINTS for ϕ_1, ϕ_2



CROSS POINTS for ϕ_{1L}, ϕ_2



CROSS POINTS for ϕ_1, ϕ_{2L}



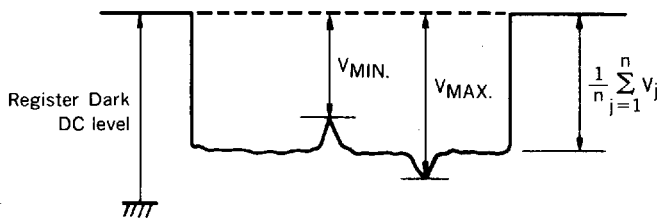
Remark Adjust cross point of (ϕ_1, ϕ_2), (ϕ_{1L}, ϕ_2), (ϕ_1, ϕ_{2L}) by each pin external input resistor.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE
Product of intensity of illumination (Ix) and storage time(s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU
The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU(\%) = \left(\frac{V_{MAX. \text{ or } V_{MIN.}} - 1}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

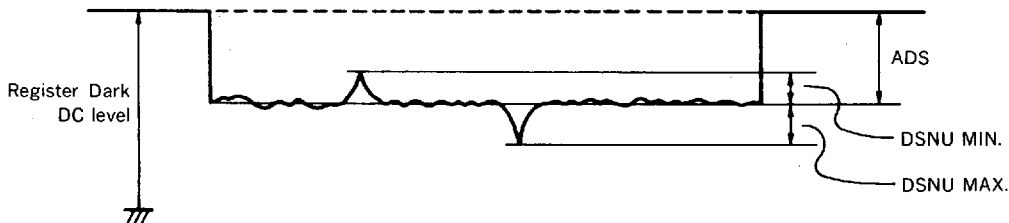
n : Number of valid bits
 V_j : Output voltage of each bit



4. Average dark signal: ADS
Output average voltage in light shielding.

$$ADS(mV) = \frac{1}{n} \sum_{j=1}^n V_j$$

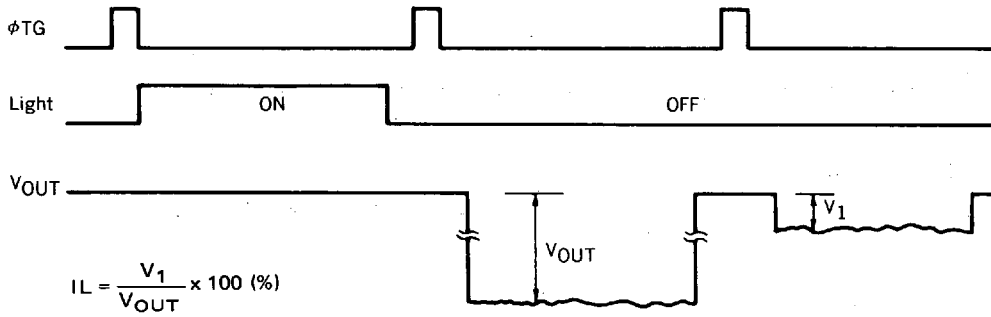
5. Dark signal non-uniformity: DSNU
The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance: Z_o
Output pin impedance viewed from outside.
7. Response: R
Output voltage divided by exposure (Ix·s).
Note that the response varies with the light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.

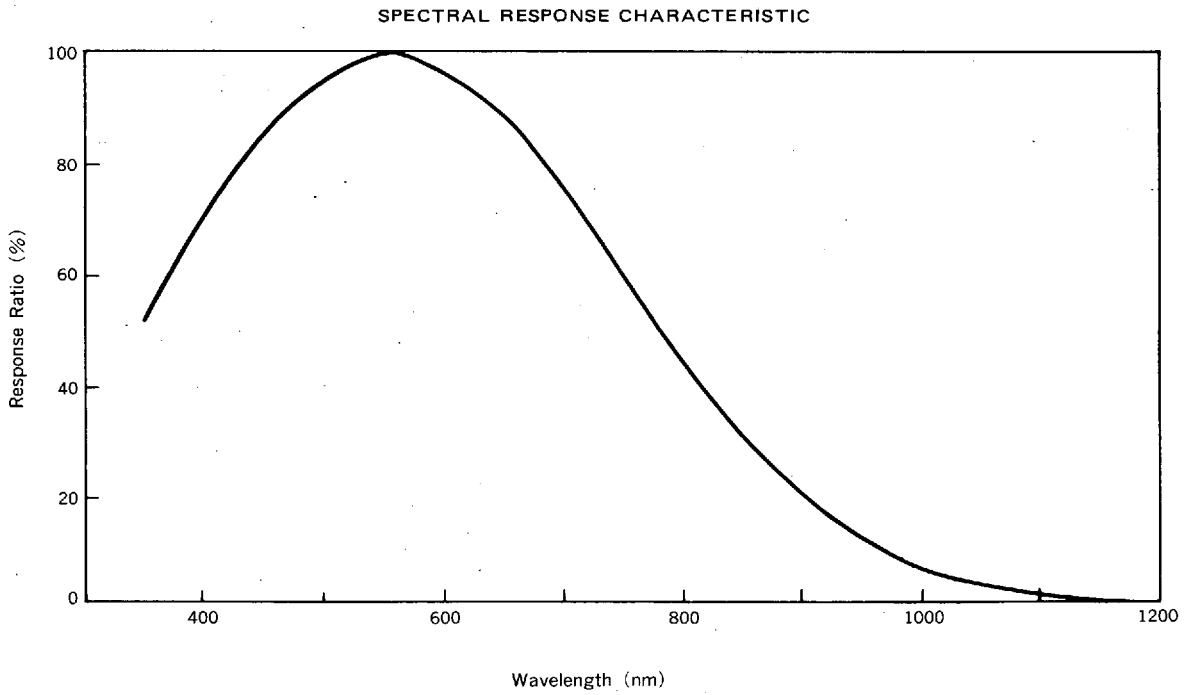
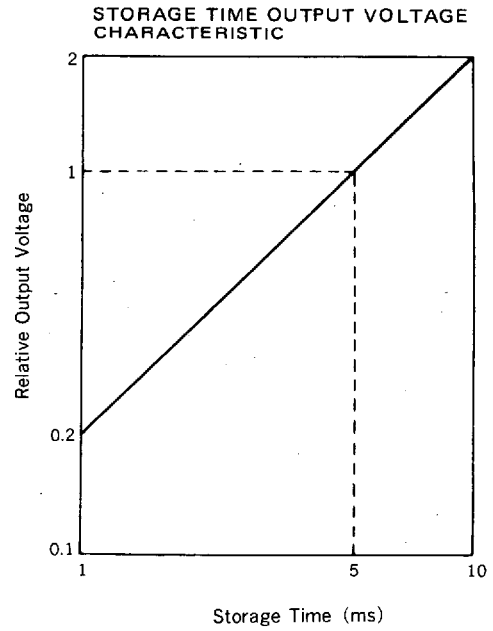
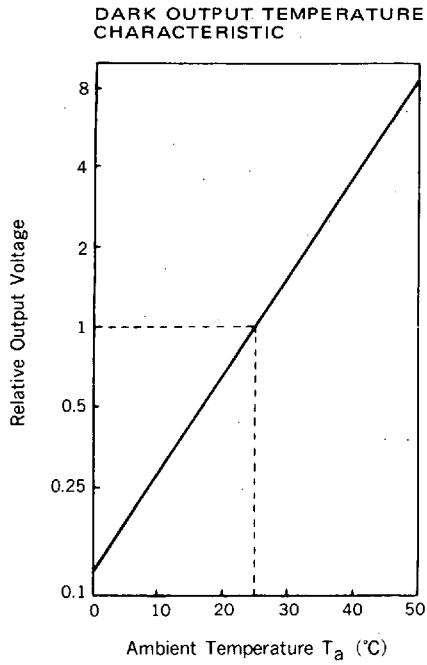


9. Register Imbalance: RI

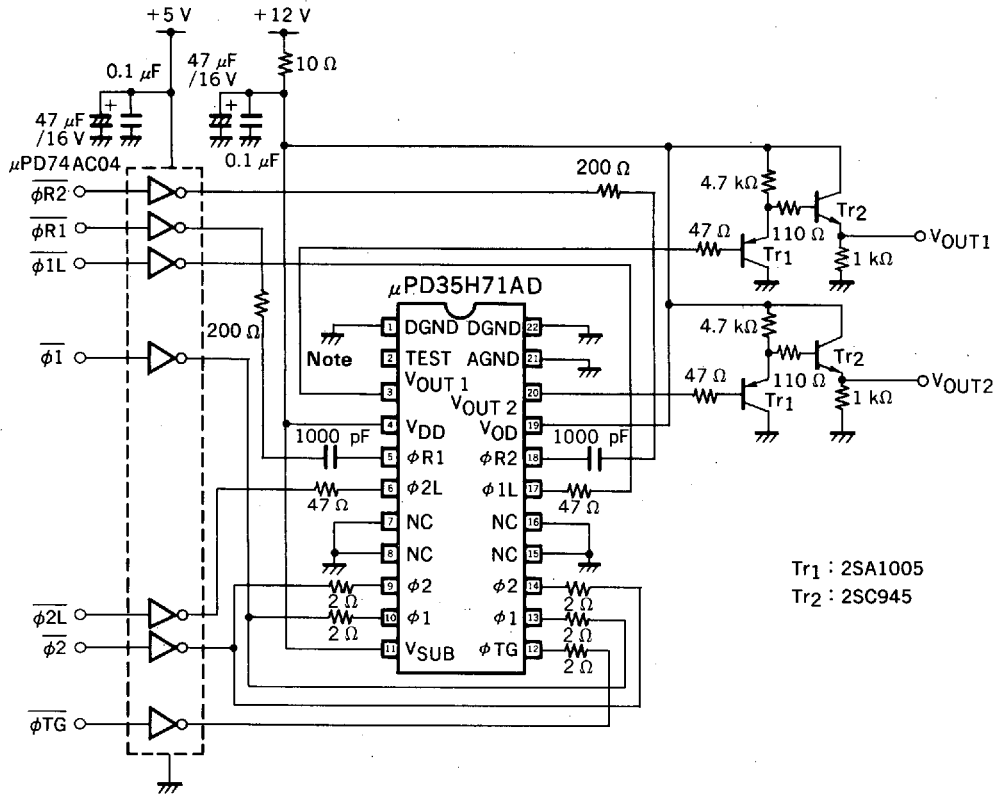
The rate of the difference between the average of the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

$$RI = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100 (\%)$$

STANDARD CHARACTERISTIC CURVES ($T_a = +25^\circ\text{C}$)



APPLICATION CIRCUIT



Tr1 : 2SA1005
Tr2 : 2SC945

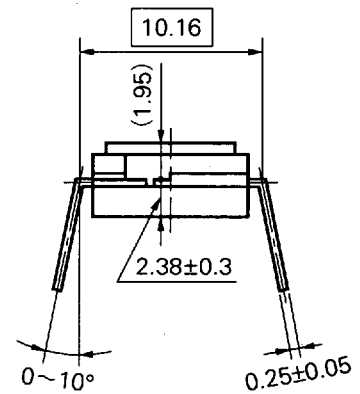
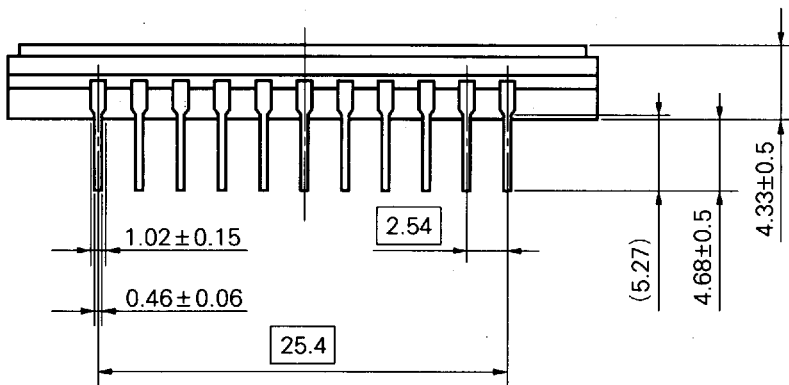
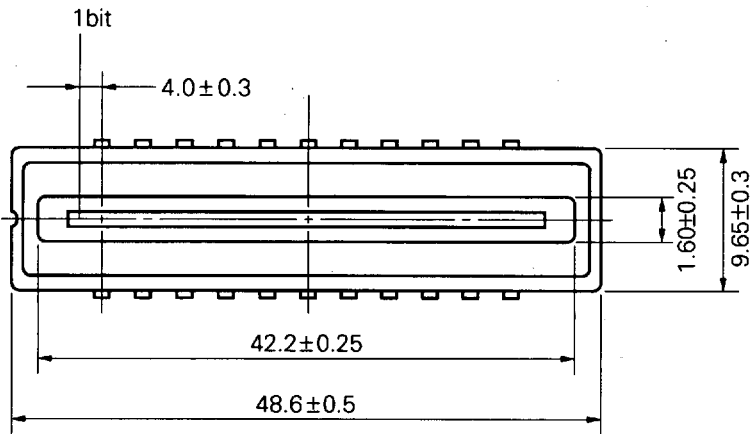
Note Leave this pin unconnected.

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

PACKAGE DIMENSIONS

CCD LINEAR IMAGE SENSOR 22PIN CERAMIC DIP(CERDIP)(400mil)

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

22D-1CCD-PKG8

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 1 Type of Through Hole Device

μPD35H71AD: CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)

Soldering Process	Soldering Conditions
Wave soldering (For leads only)	Solder temperature: 260 °C or below Flow time: 10 seconds or below
Partial heating method	Pin temperature: 260 °C or below Time: 10 seconds or below

Caution Do not jet molten solder on the surface of package.