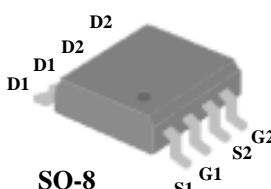


- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching

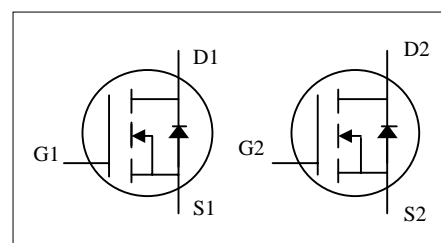


$BV_{DSS}$	25V
$R_{DS(ON)}$	25m $\Omega$
$I_D$	7A

## Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	25	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	7	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	5.7	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	20	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient <sup>3</sup>	Max. 62.5	$^\circ\text{C}/\text{W}$


**Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	25	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	-	0.037	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=7A$	-	-	25	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=5.2A$	-	-	35	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=7A$	-	14	-	S
$I_{DSS}$	Drain-Source Leakage Current ( $T_j=25^\circ\text{C}$ )	$V_{DS}=25V, V_{GS}=0V$	-	-	1	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )	$V_{DS}=20V, V_{GS}=0V$	-	-	25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=7A$	-	10.5	-	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=15V$	-	1.9	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	7.5	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=15V$	-	8	-	ns
$t_r$	Rise Time	$I_D=1A$	-	9.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=6\Omega, V_{GS}=10V$	-	25	-	ns
$t_f$	Fall Time	$R_D=15\Omega$	-	13.5	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	395	-	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	260	-	pF
$C_{riss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	105	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$I_S$	Continuous Source Current ( Body Diode )	$V_D=V_G=0V, V_S=1.2V$	-	-	1.67	A
$V_{SD}$	Forward On Voltage <sup>2</sup>	$T_j=25^\circ\text{C}, I_S=2.1A, V_{GS}=0V$	-	-	1.2	V

**Notes:**

1. Pulse width limited by Max. junction temperature.
2. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on  $1\text{ in}^2$  copper pad of FR4 board ;  $135^\circ\text{C}/W$  when mounted on Min. copper pad.

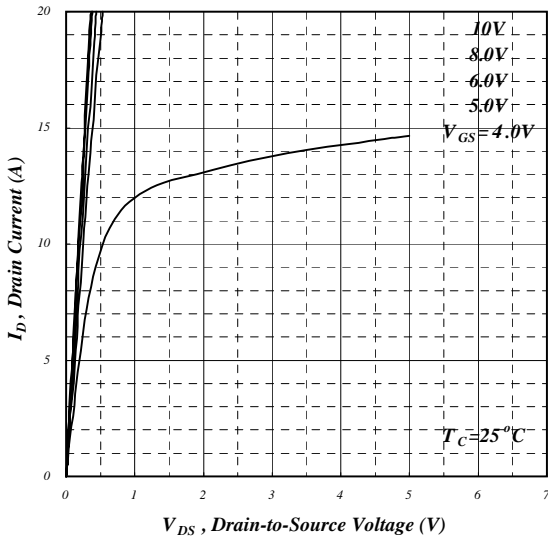


Fig 1. Typical Output Characteristics

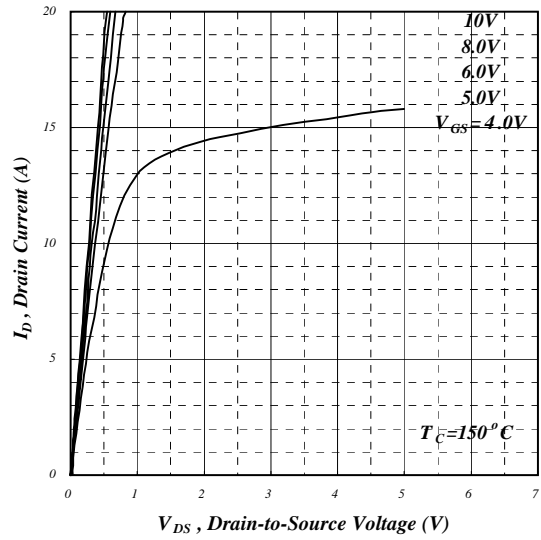


Fig 2. Typical Output Characteristics

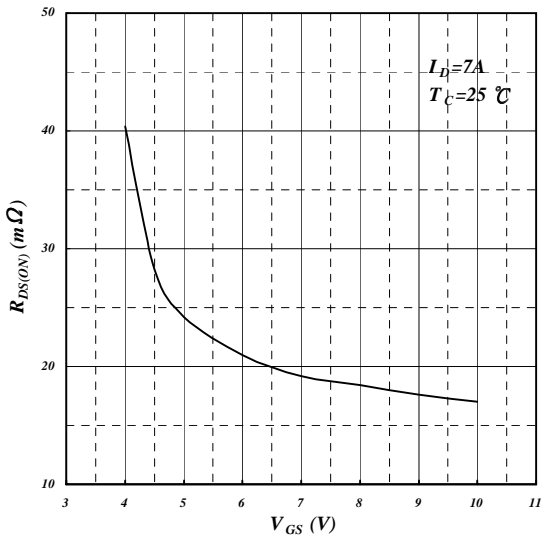


Fig 3. On-Resistance v.s. Gate Voltage

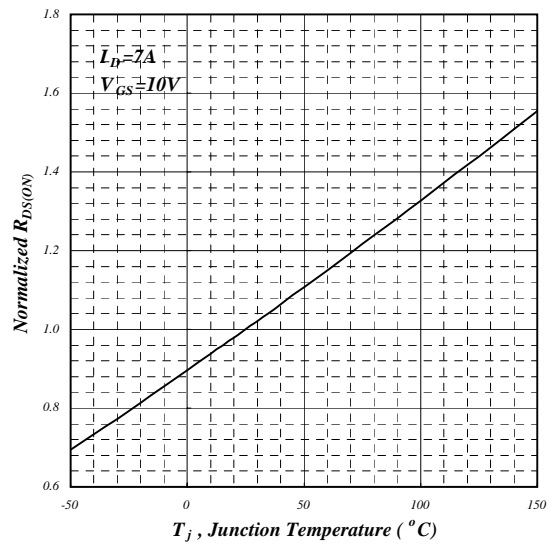


Fig 4. Normalized On-Resistance v.s. Junction Temperature

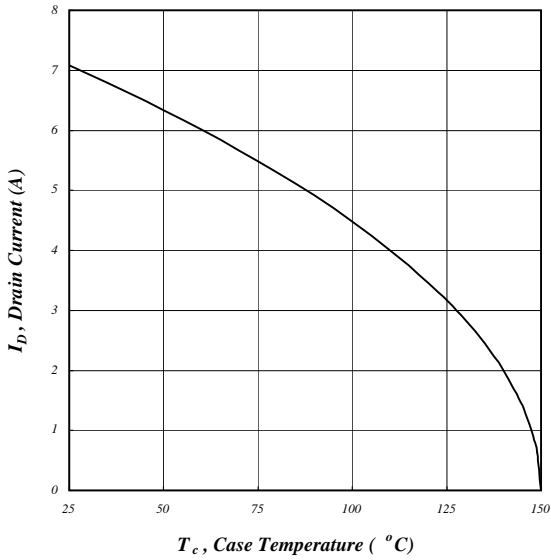


Fig 5. Maximum Drain Current v.s. Case Temperature

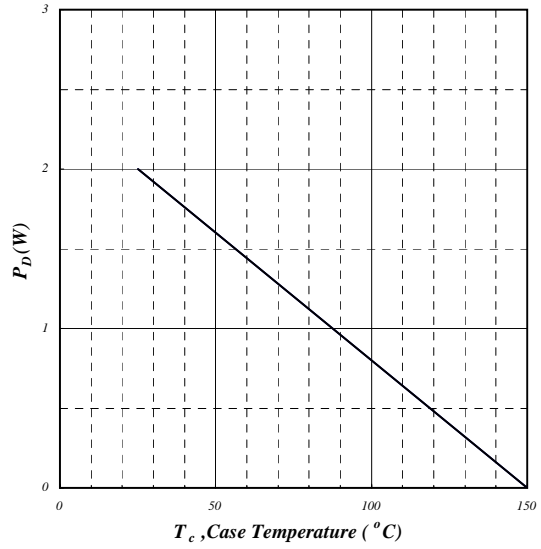


Fig 6. Typical Power Dissipation

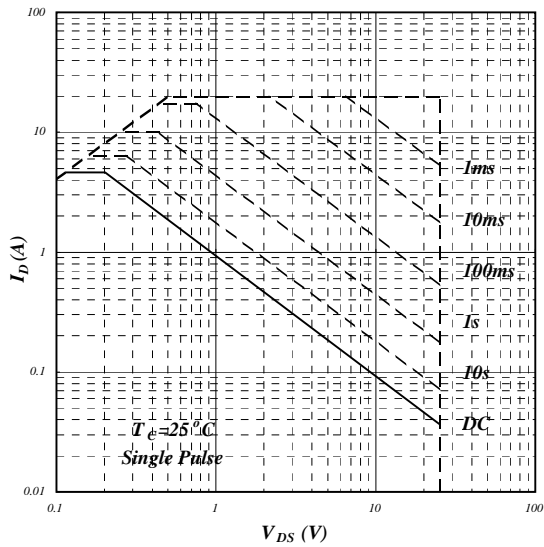


Fig 7. Maximum Safe Operating Area

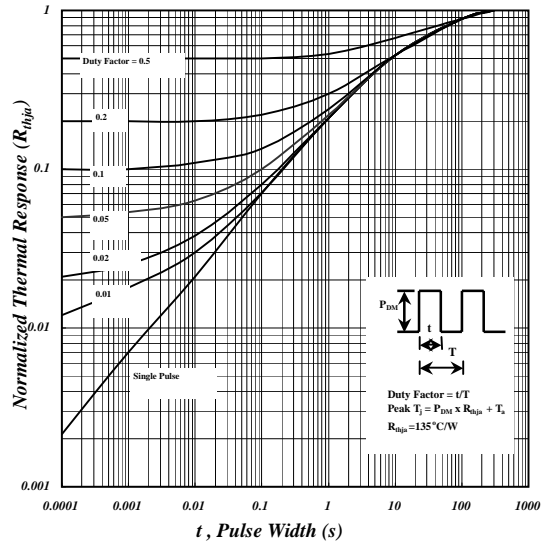


Fig 8. Effective Transient Thermal Impedance

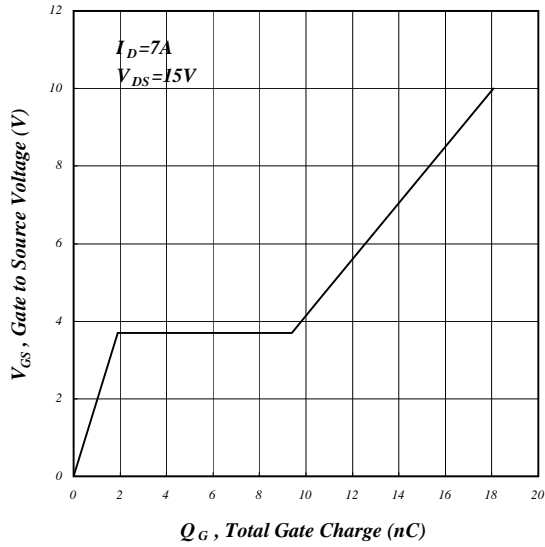


Fig 9. Gate Charge Characteristics

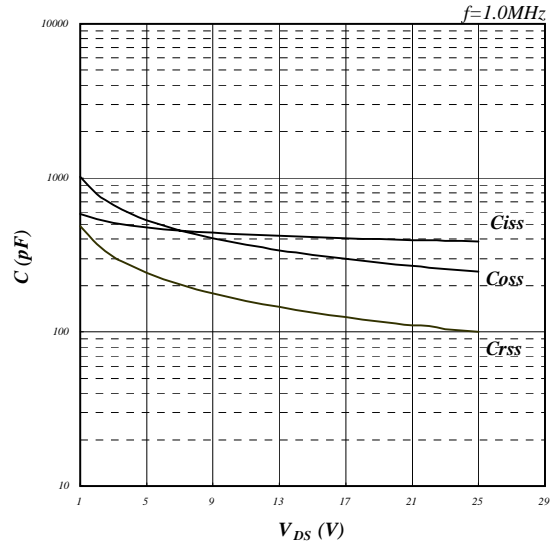


Fig 10. Typical Capacitance Characteristics

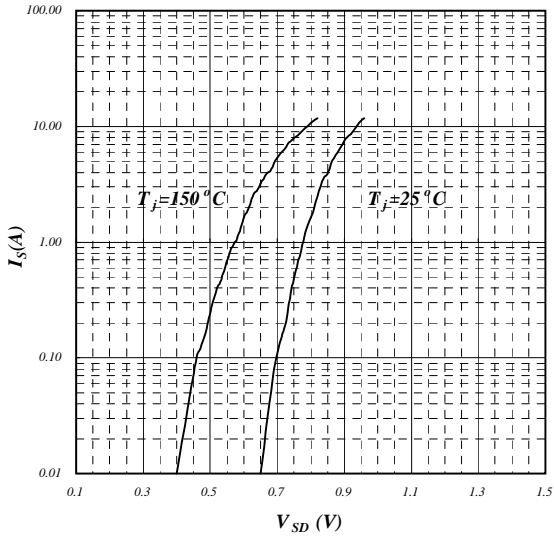


Fig 11. Forward Characteristic of Reverse Diode

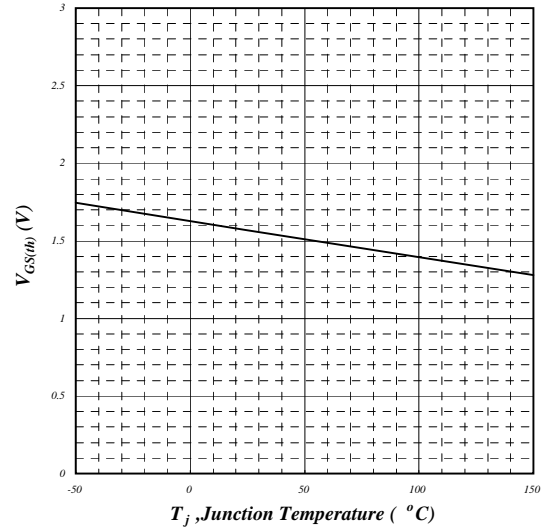


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

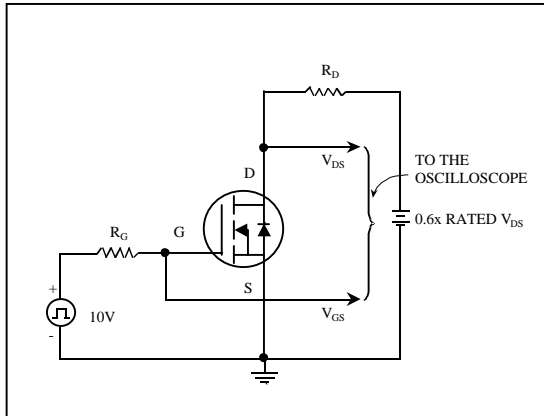


Fig 13. Switching Time Circuit

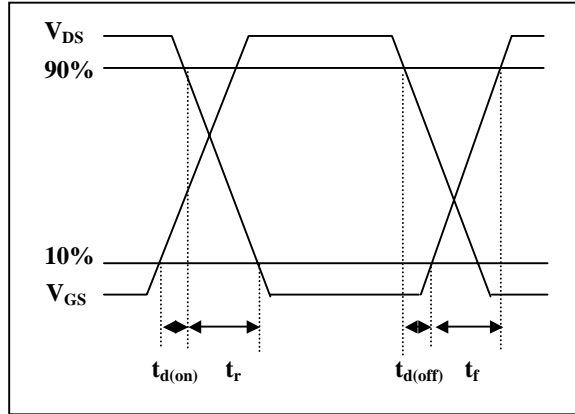


Fig 14. Switching Time Waveform

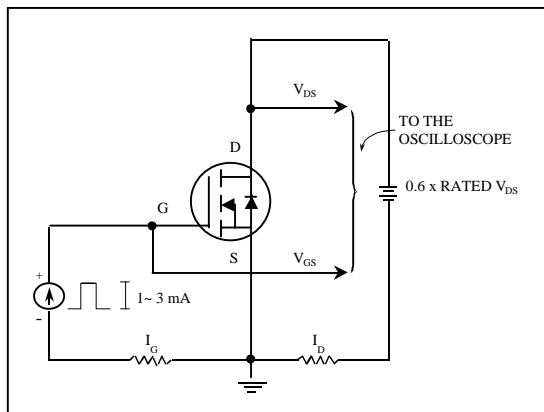


Fig 15. Gate Charge Circuit

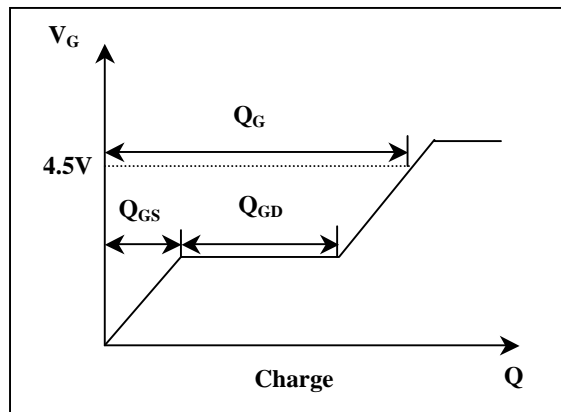


Fig 16. Gate Charge Waveform