4 Mbit (512K x 8)
3V Only CMOS Flash Memory

1. FEATURES

- Single supply voltage 3.0V-3.6V
- Fast access time: 70/90 ns
- Compatible with JEDEC standard
  - Pin-out, packages and software commands compatible with single-power supply Flash
- Low power consumption
  - 7mA typical active current
  - 25uA typical standby current
- 10,000 minimum program/erase cycles
- Command register architecture
  - Byte programming (9us typical)
  - Sector Erase(sector structure: eight 64 KB)
- Auto Erase (chip & sector) and Auto Program
  - Any combination of sectors can be erased concurrently; Chip erase also provided.
  - Automatically program and verify data at specified address
- Erase Suspend/Erase Resume
  - Suspend or Resume erasing sectors to allow the read/program in another sector
- End of program or erase detection
  - Data polling
  - Toggle bits
- Sector Protection /Un-protection
  - Hardware Protect/Unprotect any combination of sectors from a program or erase operation.
- Low V_{CC} Write inhibit is equal to or less than 2.0V
- Boot Sector Architecture
  - U = Upper Boot Sector
  - B = Bottom Boot Sector
- Packages available:
  - 32-pin TSOPI
  - 32-pin PLCC

2. ORDERING INFORMATION

Part No	Boot	Speed	Package	Part No	Boot	Speed	Package
F49L040A-70T	Upper/Bottom	70 ns	TSOPI	F49L040A-90T	Upper/Bottom	90 ns	TSOPI
F49L040A-70N	Upper/Bottom	70 ns	PLCC	F49L040A-90N	Upper/Bottom	90 ns	PLCC

3. GENERAL DESCRIPTION

The F49L040A is a 4 Megabit, 3V only CMOS Flash memory device organized as 512K bytes of 8 bits. This device is packaged in standard 32-pin TSOPI and 32-pin PLCC. It is designed to be programmed and erased both in system and can in standard EPROM programmers.

With access times of 70 ns and 90 ns, the F49L040A allows the operation of high-speed microprocessors. The device has separate chip enable $\overline{CE}$, write enable $\overline{WE}$, and output enable $\overline{OE}$ controls. EFST's memory devices reliably store memory data even after 100,000 program and erase cycles.

The F49L040A is entirely pin and command set compatible with the JEDEC standard for 4 Megabit Flash memory devices. Commands are written to the command register using standard microprocessor write timings.

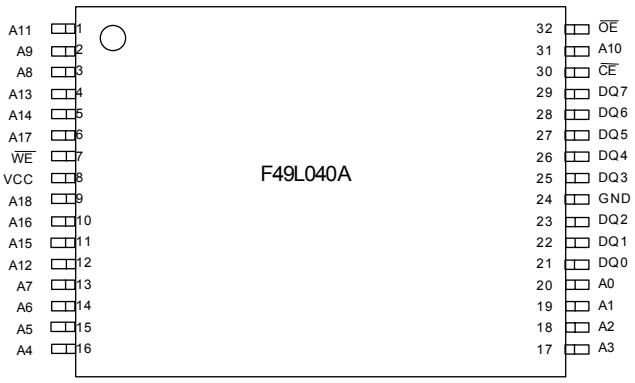
The F49L040A features a sector erase architecture. The device memory array is divided into eight 64 Kbytes. Sectors can be erased individually or in groups without affecting the data in other sectors. Multiple-sector erase and whole chip erase capabilities provide the flexibility to revise the data in the device.

The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory. This can be achieved in-system or via programming equipment.

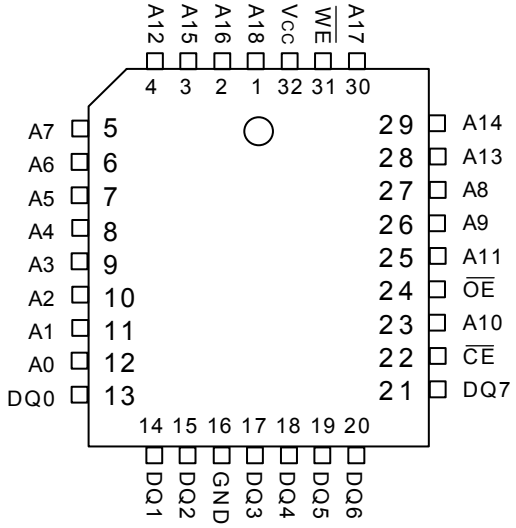
A low V_{CC} detector inhibits write operations on loss of power. End of program or erase is detected by the Data Polling of DQ7, or by the Toggle Bit I feature on DQ6. Once the program or erase cycle has been successfully completed, the device internally resets to the Read mode.

4. PIN CONFIGURATIONS

4.1 32-pin TSOP I



4.2 32-pin PLCC



4.3 Pin Description

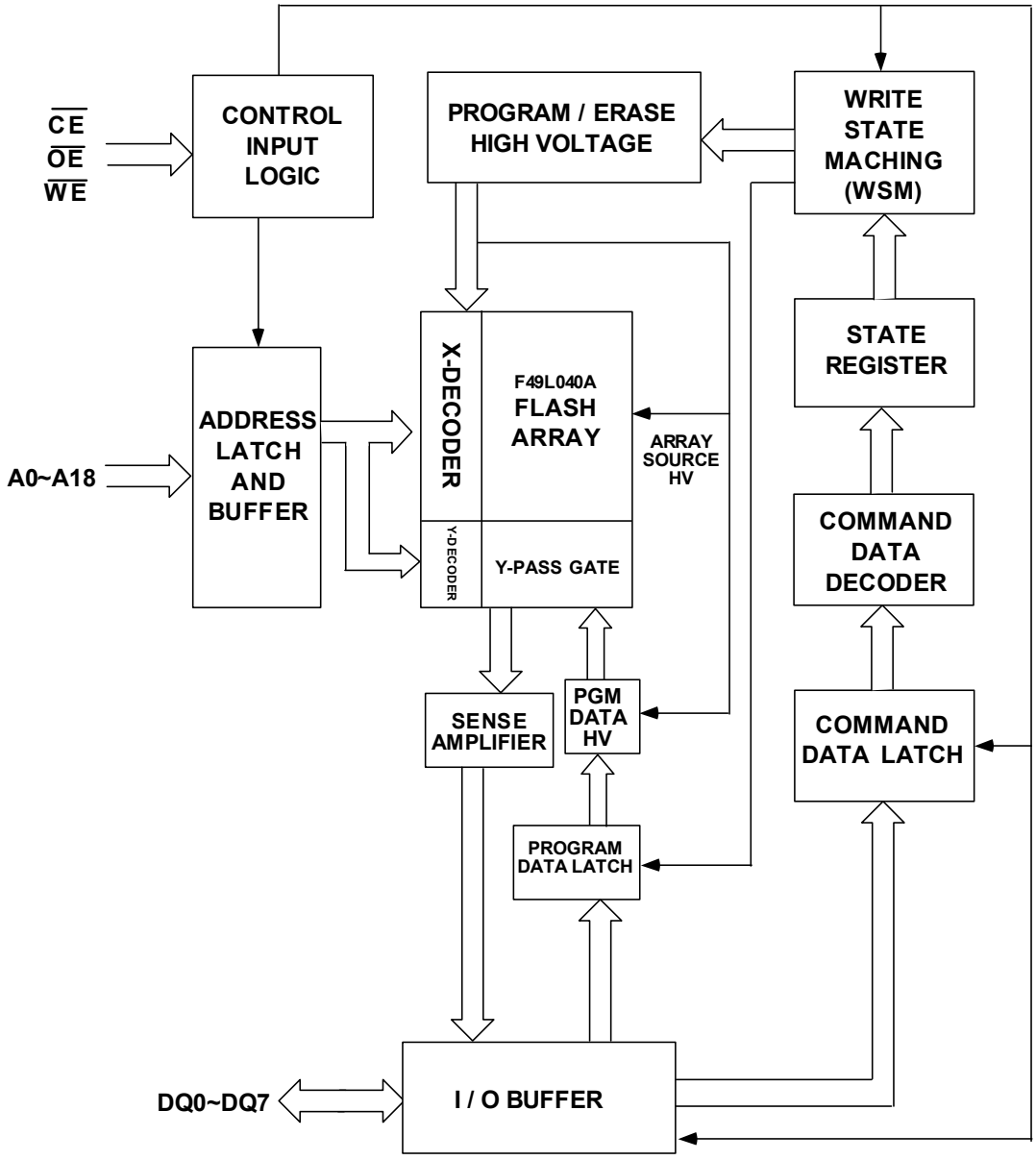
Symbol	Pin Name	Functions
A0~A18	Address Input	To provide memory addresses.
DQ0~DQ7	Data Input/Output	To output data when Read and receive data when Write. The outputs are in tri-state when $\overline{OE}$ or $\overline{CE}$ is high.
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{OE}$	Output Enable	To gate the data output buffers.
$\overline{WE}$	Write Enable	To control the Write operations.
V_{CC}	Power Supply	To provide power
GND	Ground	

5. SECTOR STRUCTURE

Table 1: F49L040A Sector Address Table

Sector	Sector Size (Kbytes)	Address range	Sector Address					
			A18	A17	A16	A15	A14	A13
SA7	64	70000H-7FFFFH	1	1	1	X	X	X
SA6	64	60000H-6FFFFH	1	1	0	X	X	X
SA5	64	50000H-5FFFFH	1	0	1	X	X	X
SA4	64	40000H-4FFFFH	1	0	0	X	X	X
SA3	64	30000H-3FFFFH	0	1	1	X	X	X
SA2	64	20000H-2FFFFH	0	1	0	X	X	X
SA1	64	10000H-1FFFFH	0	0	1	X	X	X
SA0	64	00000H-0FFFFH	0	0	0	X	X	X

6. FUNCTIONAL BLOCK DIAGRAM



7. FUNCTIONAL DESCRIPTION

7.1 Device operation

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The register is composed of latches that store the command, address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The F49L040A features various bus operations as Table 2.

Table 2. F49L040A Operation Modes Selection

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS								DQ0~DQ7
				A18 | A13	A12 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0	
Read	L	L	H	AIN								Dout
Write	L	H	L	AIN								DIN
Output Disable	L	H	H	X								High Z
Standby	H	X	X	X								High Z
Sector Protect(2)	L	H	L	SA	X	V_{ID}	X	L	X	H	L	DIN
Sector Unprotect(2)	L	H	L	SA	X	V_{ID}	X	H	X	H	L	DIN
Auto-select	See Table 3											

Notes:

1. L= Logic Low = V_{IL}, H= Logic High = V_{IH}, X= Don't Care, SA= Sector Address, V_{ID}=11.5V to 12.5V. AIN= Address In, DIN = Data In, Dout = Data Out.
2. The sector protect and unprotect functions may also be implemented via programming equipment.

Table 3. F49L040A Auto-Select Mode (High Voltage Method)

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS								DQ0~DQ7
				A18 | A13	A12 | A10	A9	A8 | A4	A6	A3	A2	A1	A0	
(Manufacturer ID:EFST)	L	L	H	X	X	V_{ID}	X	X	L	H	L	L	7FH
	L	L	H	X	X	V_{ID}	X	X	H	L	L	L	7FH
	L	L	H	X	X	V_{ID}	X	X	H	H	L	L	7FH
	L	L	H	X	X	V_{ID}	X	X	L	L	L	L	8CH
(Device ID: F49L040A)	L	L	H	X	X	V_{ID}	X	X	X	X	L	H	4FH
Sector Protection Verify	L	L	H	SA	X	V_{ID}	X	L	X	X	H	L	Code(2)

Notes :

1.Manufacturer and device codes may also be accessed via the software command sequence in Table 4.
2. Code=00H means unprotected.
Code =01H means protected.

Read Mode

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to V_{IL}. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at V_{IH}. The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

No command is necessary in this mode to obtain array data. Standard microprocessor's read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Read Command" section for more information. Refer to the AC Read Operations Table 9 for timing specifications and to Figure 5 for the timing diagram. I_{CC1} in the DC Characteristics Table 8 represents the active current specification for reading array data.

Write Mode

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}. The "Program Command" section has details on programming data to the device using standard command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 1 indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Software Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

When the system writes the auto-select command sequence, the device enters the auto-select mode. The system can then read auto-select codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Auto-select Mode and Auto-select Command sections for more information. I_{CC2} in the DC Characteristics Table 8 represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification Table 10 and timing diagrams for write operations.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain unchanged for over 250ns. The automatic sleep mode is independent of the $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics Table 8 represents the automatic sleep mode current specification.

Output Disable Mode

With the $\overline{OE}$ is at a logic high level (V_{IH}), outputs from the devices are disabled. This will cause the output pins in a high impedance state

Standby Mode

When $\overline{CE}$ held at V_{CC} ± 0.3V, the device enter CMOS Standby mode. If $\overline{CE}$ held at V_{IH}, but not within the range of V_{CC} ± 0.3V, the device will still be in the standby mode, but the standby current will be larger.

If the device is deselected during auto algorithm of erasure or programming, the device draws active current I_{CC2} until the operation is completed. I_{CC3} in the DC Characteristics Table 8 represents the standby current specification.

The device requires standard access time (t_{CE}) for read access from either of these standby modes, before it is ready to read data.

Sector Protect / Un-protect Mode

The hardware sector protect feature disables both program and erase operations in any sector. The hardware sector unprotect feature re-enables both the program and erase operations in previously protected sectors. Sector protect/unprotect can be implemented A6 pin via programming equipment.

Figure 16 shows the algorithms and Figure 15 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

Auto-select Mode

The auto-select mode provides manufacturer and device identification and sector protection verification, through outputs on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the auto-select codes can also be accessed in-system through the command register.

When using programming equipment, this mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. While address pins A3, A2, A1, and A0 must be as shown in Table 3.

To verify sector protection, all necessary pins have to be set as required in Table 3, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the auto-select codes in-system, the host system can issue the auto-select command via the command register, as shown in Table 4. This method does not require V_{ID}. See " Software Command Definitions" for details on using the auto-select mode.

7.2 Software Command Definitions

Writing specific address and data commands or sequences into the command register initiates the device operations. Table 4 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Refer to the corresponding timing diagrams in the AC Characteristics section.

Table 4. F49L040A Software Command Definitions

Command	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset (5)	1	XXXH	F0H	-	-	-	-	-	-	-	-	-	-
Read (4)	1	RA	RD	-	-	-	-	-	-	-	-	-	-
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend (6)	1	XXXH	B0H	-	-	-	-	-	-	-	-	-	-
Sector Erase Resume (7)	1	XXXH	30H	-	-	-	-	-	-	-	-	-	-
Auto-select	See Table 5.												

Notes:

1. X = don't care
   RA = Address of memory location to be read.
   RD = Data to be read at location RA.
   PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address of the sector.
2. Except Read command and Auto-select command, all command bus cycles are write operations.
3. Address bits A18–A16 are don't cares.
4. No command cycles required when reading array data.
5. The system may read and program in non-erasing sectors, or enter the auto-select mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
6. The Erase Resume command is valid only during the Erase Suspend mode.

Table 5. F49L040A Auto-Select Command

Command	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Manufacture ID	4	555H	AAH	2AAH	55H	555H	90H	X04H	7FH	-	-	-	-
	4	555H	AAH	2AAH	55H	555H	90H	X08H	7FH	-	-	-	-
	4	555H	AAH	2AAH	55H	555H	90H	X0CH	7FH	-	-	-	-
	4	555H	AAH	2AAH	55H	555H	90H	X00H	8CH	-	-	-	-
Device ID, Upper boot	4	555H	AAH	2AAH	55H	555H	90H	X01H	4FH	-	-	-	-
Sector Protect Verify	4	555H	AAH	2AAH	55H	555H	90H	(SA) x02H	00H 01H	-	-	-	-

Notes :

1. The fourth cycle of the auto-select command sequence is a read cycle.
2. For Sector Protect Verify operation: If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are all don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an auto-select command sequence. Once in the auto-select mode, the reset command must be written to return to reading array data (also applies to auto-select during Erase Suspend).

If DQ5 goes high(see "DQ5: Exceeded Timing Limits" section) during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Read Command

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

When the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the auto-select mode. See the "Reset Command" section. See also the "Read Mode" in the "Device Operations" section for more information. Refer to Figure 5 for the timing diagram.

Program Command

The program command sequence programs one byte into the device. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 and DQ6. See "Write Operation Status" section for more information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Chip Erase Command

Chip erase is a six-bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure the data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6 or DQ2. See "Write Operation Status" section for more information on these status bits.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. See the Erase/Program Operations Table 11 in "AC Characteristics" for parameters.

Sector Erase Command

Sector erase is a six-bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 μs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 μs, otherwise the last address and command might not be accepted, and erasure may begin.

It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 μs, the system need not monitor DQ3.

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.
Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a hardware reset during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure the data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6 or DQ2. (Refer to "Write Operation Status" section for more information on these status bits.)
Refer to the Erase/Program Operations Table 11 in the "AC Characteristics" section for parameters.

Sector Erase Suspend/Resume Command

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure (The device "erase suspends" all sectors selected for erasure.). This command is valid only during the sector erase operation, including the 50 μs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are "don't-cares" when writing the Erase Suspend command as shown in Table 4.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 μs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" section for more information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the auto-select command sequence when the device is in the Erase Suspend mode. The device allows reading auto-select codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the auto-select mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation.

The system must write the Erase Resume command (address bits are “don’t care” as shown in Table 4) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Auto-select Command

The auto-select command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 5 shows the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The auto-select command sequence is initiated by writing two unlock cycles, followed by the auto-select command. The device then enters the auto-select mode, and the system may read at any address any number of times, without initiating another command sequence. The read cycles at address 04H, 08H, 0CH, and 00H retrieves the EFST manufacturer ID. A read cycle at address 01H retrieves the device ID. A read cycle containing a sector address (SA) and the address 02H returns 01H if that sector is protected, or 00H if it is unprotected. Refer to Table 1 for valid sector addresses.

The system must write the reset command to exit the auto-select mode and return to reading array data.

7.3 Write Operation Status

The device provides several bits to determine the status of a write operation: DQ7, DQ6, DQ5, DQ3, DQ2, and. Table 6 and the following subsections describe the functions of these bits. DQ7, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress.

Table 6. Write Operation Status

	Status		DQ7 (Note1)	DQ6	DQ5 (Note2)	DQ3	DQ2
In Progress	Embedded Program Algorithm		$\overline{DQ7}$	Toggle	0	N/A	No Toggle
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Reading Erase Suspended Sector	1	No Toggle	0	N/A	Toggle
		Reading Non-Erase Suspended Sector	Data	Data	Data	Data	Data
		Erase Suspend Program	$\overline{DQ7}$	Toggle	0	N/A	N/A
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ7}$	Toggle	1	N/A	No Toggle
	Embedded Erase Algorithm		0	Toggle	1	1	Toggle
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	N/A	N/A

Notes:

1. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See “DQ5: Exceeded Timing Limits” for more information.

DQ7: Data Polling

The DQ7 indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend mode. The Data Polling is valid after the rising edge of the final $\overline{WE}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed
to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the true data on DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data Polling on DQ7 is active for approximately 1 μs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data Polling on DQ7 is active for approximately 100 μs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7~ DQ0 on the following read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable ($\overline{OE}$) is asserted low. Refer to Figure 19, Data Polling Timings (During Embedded Algorithms), Figure 17 shows the Data Polling algorithm.

DQ6:Toggle BIT I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles. When the operation is complete, DQ6 stops toggling.

When an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (i.e. the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7.

If a program address falls within a protected sector, DQ6 toggles for approximately 2 μs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete. Table 6 shows the outputs for Toggle Bit I on DQ6. Figure 18 shows the toggle bit algorithm. Figure 20 shows the toggle bit timing diagrams. Figure 21 shows the differences between DQ2 and DQ6 in graphical form. Refer to the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ or $\overline{CE}$, whichever happens first, in the command sequence.
DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended.

DQ6, by comparison, indicates whether the device is actively erasing, or whether is in erase-suspended, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for DQ2 and DQ6.

Figure 18 shows the toggle bit algorithm in flowchart form. See also the DQ6: Toggle Bit I subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/ DQ2

Refer to Figure 18 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described earlier. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions DQ5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.
If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination
of sectors are bad.

If this time-out condition occurs during the programming operation, it specifies that the sector containing that byte is bad and this sector may not be reused, however other sectors are still functional and can be reused.

The time-out condition will not appear if a user tries to program a non blank location without erasing. Please note that this is not a device failure condition since the device was incorrectly used.

DQ3:Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire timeout also applies after each additional sector erase command.
When the time-out is complete, DQ3 switches from "0" to "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 μs, the system need not monitor DQ3.

When the sector erase command sequence is written, the system should read the status on DQ7 (Data Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the internally controlled erase cycle has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete.

If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 6 shows the outputs for DQ3.

7.4 More Device Operations

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{cc} Write Inhibit

When V_{CC} is less than VLKO, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power Supply Decoupling

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its V_{CC} and GND.

Power-Up Sequence

The device powers up in the Read Mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

Power-Up Write Inhibit

If $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} during power up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to reading array data on power-up.

8. ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C
Ambient Temperature
with Power Applied. . . . . –65°C to +125°C
Voltage with Respect to Ground
V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V
A9 and $\overline{OE}$ (Note 2) . . . . . –0.5 V to +12.5 V
All other pins (Note 1). . . . . –0.5 V to V_{CC} +0.5 V
Output Short Circuit Current (Note 3) . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 2.
2. Minimum DC input voltage on pins A9 and $\overline{OE}$ is -0.5 V. During voltage transitions, A9 and $\overline{OE}$ may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Maximum Negative Overshoot Waveform

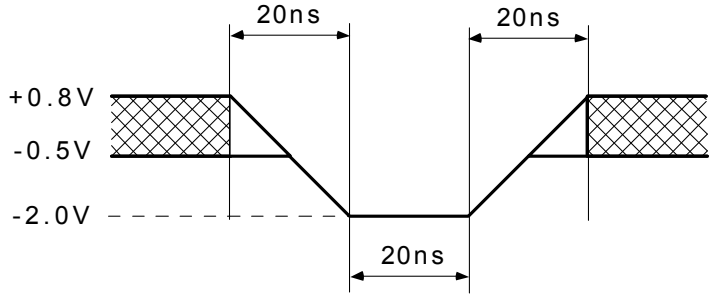
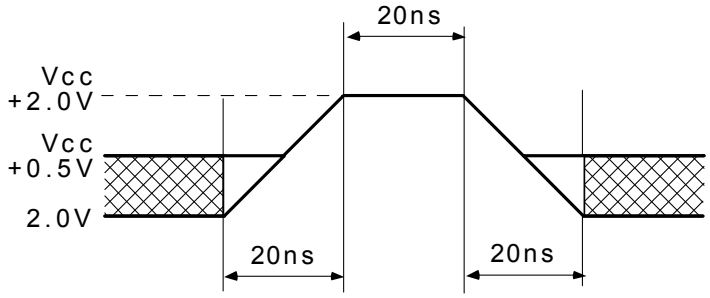


Figure 2. Maximum Positive Overshoot Waveform



OPERATING RANGES

Commercial (C) Devices Ambient Temperature (TA) . . . . . 0°C to +70°C

V_{CC} Supply Voltages V_{CC} for all devices . . . . . 3.0 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Table 7. Capacitance T_A = 25°C , f = 1.0 MHz

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	V_{IN} = 0V			8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0V			12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			12	pF

9. DC CHARACTERISTICS

Table 8. DC Characteristics T_A = 0C to 70C, V_{CC} = 3.0V to 3.6V

Symbol	Description	Conditions		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}, $V_{CC} = V_{CC}$ max.				±1	uA
I_{LIT}	A9 Input Leakage Current	$V_{CC} = V_{CC}$ max; A9=12.5V				35	uA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, $V_{CC} = V_{CC}$ max				±1	uA
I_{CC1}	V_{CC} Active Read Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	@5MHz		7	25	mA
			@1MHz		2	5	mA
I_{CC2}	V_{CC} Active write Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$			15	30	mA
I_{CC3}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3V$			25	100	uA
I_{CC4}	V_{CC} Standby Current During Reset	$\overline{CE} = V_{CC} \pm 0.3V$			25	100	uA
I_{CC5}	Automatic sleep mode	$V_{IH} = V_{CC} \pm 0.3V$; $V_{IL} = V_{SS} \pm 0.3V$			25	100	uA
V_{IL}	Input Low Voltage(Note 1)			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Auto-Select and Temporary Sector Unprotect	V_{CC} =3.3V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0mA, $V_{CC} = V_{CC}$ min				0.45	V
V_{OH1}	Output High Voltage(TTL)	I_{OH} = -2mA, $V_{CC} = V_{CC}$ min		0.7x V_{CC}			
V_{OH2}	Output High Voltage	I_{OH} = -100uA, V_{CC} min		V_{CC} -0.4			
V_{LKO}	Low V_{CC} Lock-out Voltage			2.3		2.5	V

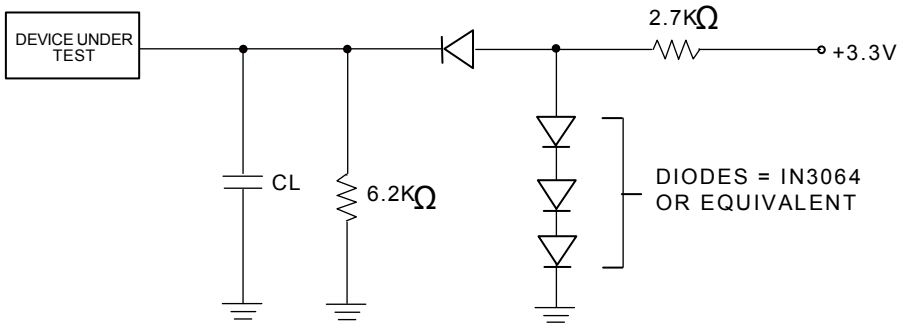
Notes :

1. V_{IL} min. = -1.0V for pulse width is equal to or less than 50 ns.
   V_{IL} min. = -2.0V for pulse width is equal to or less than 20 ns.
2. V_{IH} max. = V_{CC} + 1.5V for pulse width is equal to or less than 20 ns
   If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
3. Automatic sleep mode enable the low power mode when addresses remain stable for 250 ns

10. AC CHARACTERISTICS

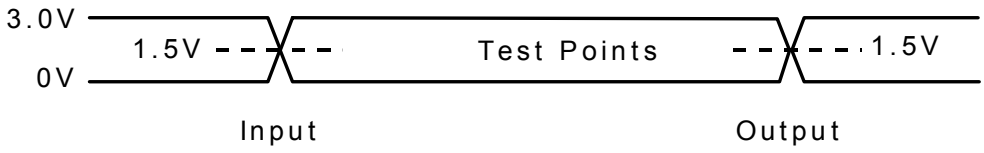
TEST CONDITIONS

Figure 3. Test Setup



CL = 100pF Including jig capacitance
CL = 30pF for F49L040A

Figure 4. Input Waveforms and Measurement Levels



AC TESTING : Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0"
Input pulse rise and fall times are < 5ns.

10.1 Read Operation

TA = 0C to 70C, V_{CC} = 3.0V~3.6V

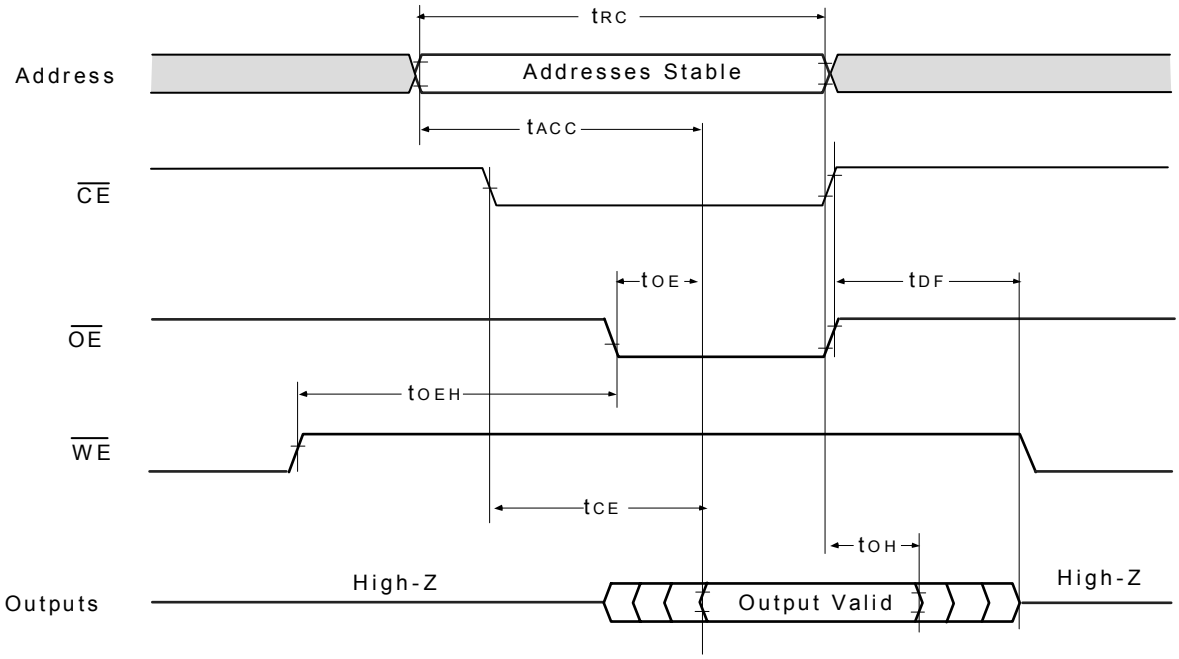
Table 9. Read Operations

Symbol	Description		Conditions	-70		-90		Unit
				Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time (Note 1)			70		90		ns
t_{ACC}	Address to Output Delay		$\overline{CE}=\overline{OE}=V_{IL}$		70		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE}=V_{IL}$		70		90	ns
t_{OE}	$\overline{OE}$ to Output Delay		$\overline{CE}=V_{IL}$		30		35	ns
t_{DF}	$\overline{OE}$ High to Output Float (Note1)		$\overline{CE}=V_{IL}$		25		30	ns
t_{OEH}	Output Enable	Read		0		0		ns
	Hold Time	Toggle and Data Polling		10		10		ns
t_{OH}	Address to Output hold		$\overline{CE}=\overline{OE}=V_{IL}$	0		0		ns

Notes :

1. Not 100% tested.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Figure 5. Read Timing Waveform



10.2 Program/Erase Operation

Table 10. $\overline{WE}$ Controlled Program/Erase Operations(T_A = 0C to 70C, V_{CC} = 3.0V~3.6V)

Symbol	Description	-70		-90		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time (Note 1)	**70**		**90**		ns
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	45		45		ns
t_{DS}	Data Setup Time	35		35		ns
t_{DH}	Data Hold Time	0		0		ns
t_{OES}	Output Enable Setup Time	0		0		ns
t_{GHWL}	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ low)	0		0		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		ns
t_{WP}	Write Pulse Width	35		35		ns
t_{WPH}	Write Pulse Width High	30		30		ns
t_{WHWH1}	Programming Operation (Note 2) (Byte program time)	9(typ.)		9(typ.)		us
t_{WHWH2}	Sector Erase Operation (Note 2)	0.7(typ.)		0.7(typ.)		sec
t_{VCS}	V_{CC} Setup Time (Note 1)	50		50		us

Notes :

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Table 11. $\overline{CE}$ Controlled Program/Erase Operations(T_A = 0C to 70C, V_{CC} = 3.0V~3.6V)

Symbol	Description	-70		-90		
		Min.	Max.	Min.	Max.	Unit
t_{WC}	Write Cycle Time (Note 1)	70		90		ns
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	45		45		ns
t_{DS}	Data Setup Time	35		35		ns
t_{DH}	Data Hold Time	0		0		ns
t_{OES}	Output Enable Setup Time	0		0		ns
t_{GHEL}	Read Recovery Time Before Write	0		0		ns
t_{WS}	$\overline{WE}$ Setup Time	0		0		ns
t_{WH}	$\overline{WE}$ Hold Time	0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width	35		35		ns
t_{CPH}	$\overline{CE}$ Pulse Width High	30		30		ns
t_{WHWH1}	Programming Operation(note2)	9(typ.)		9(typ.)		us
t_{WHWH2}	Sector Erase Operation (note2)	0.7(typ.)		0.7(typ.)		sec

Notes :

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Figure 6. Write Command Timing Waveform

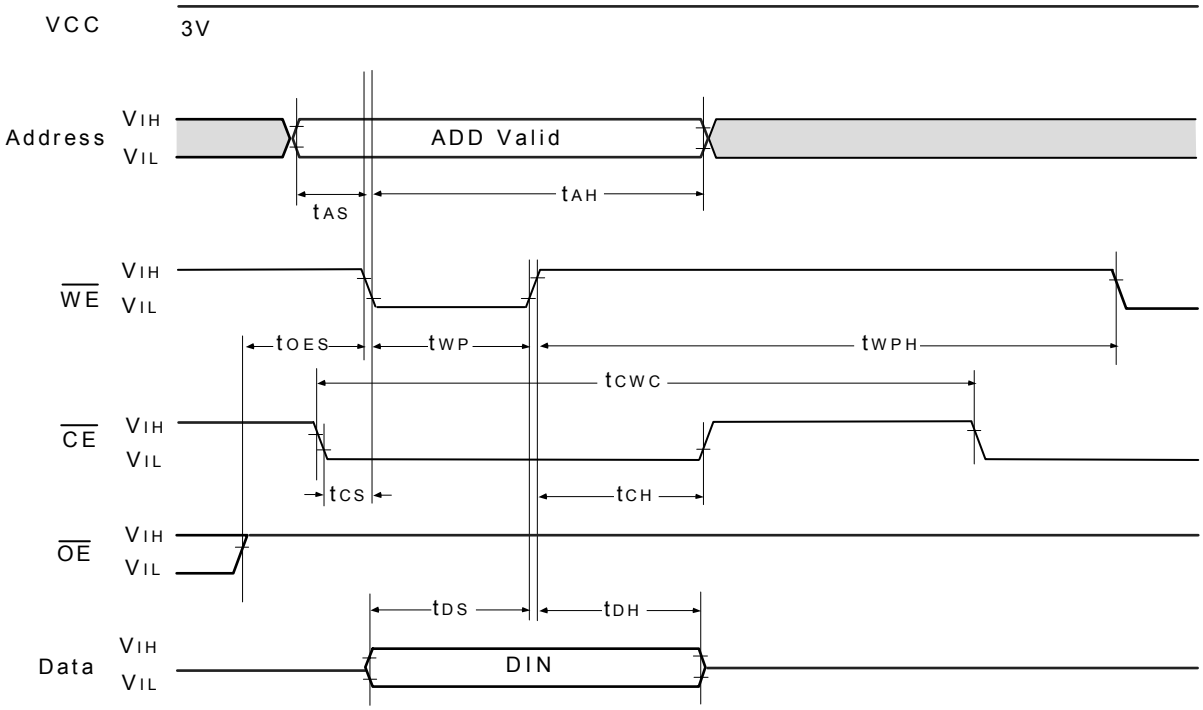
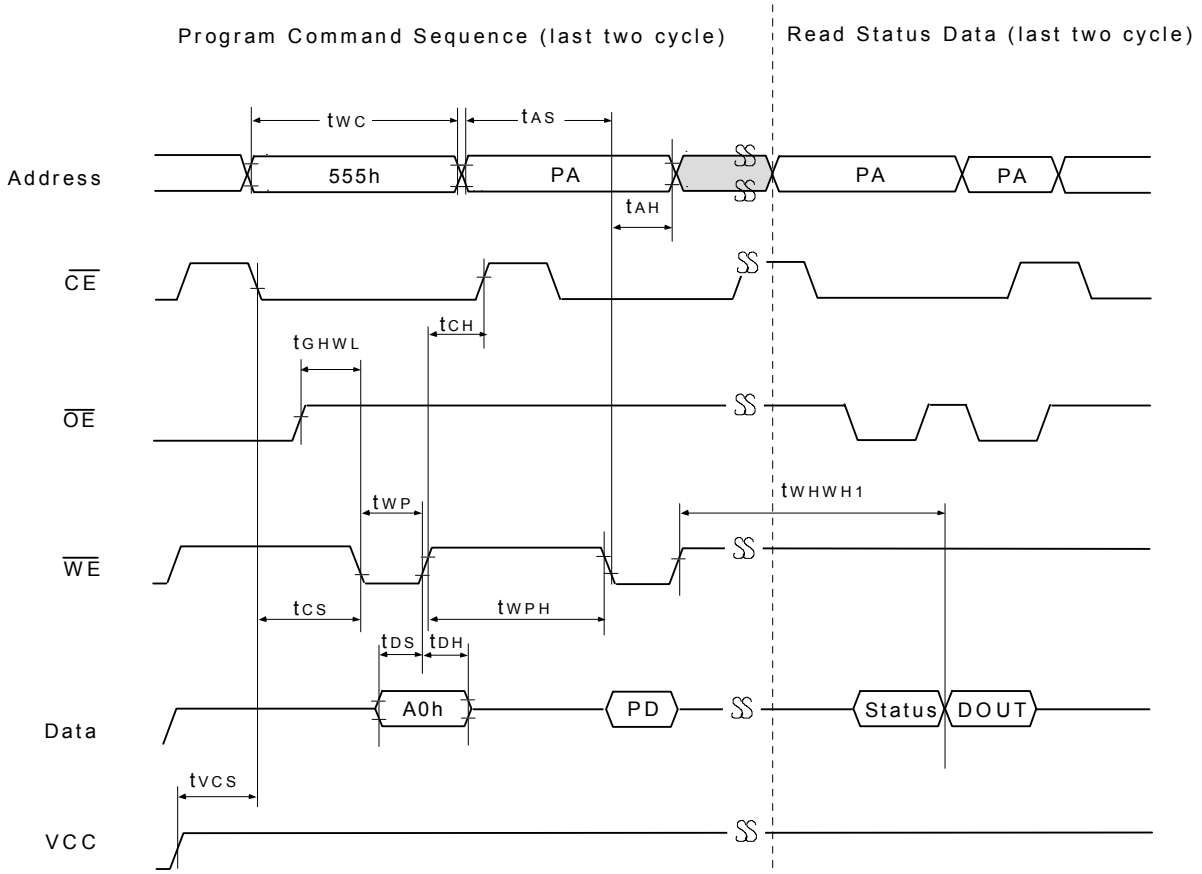


Figure 7. Embedded Programming Timing Waveform



Notes :

1. PA = Program Address, PD = Program Data, DOUT is the true data the program address.

Figure 8. Embedded Programming Algorithm Flowchart

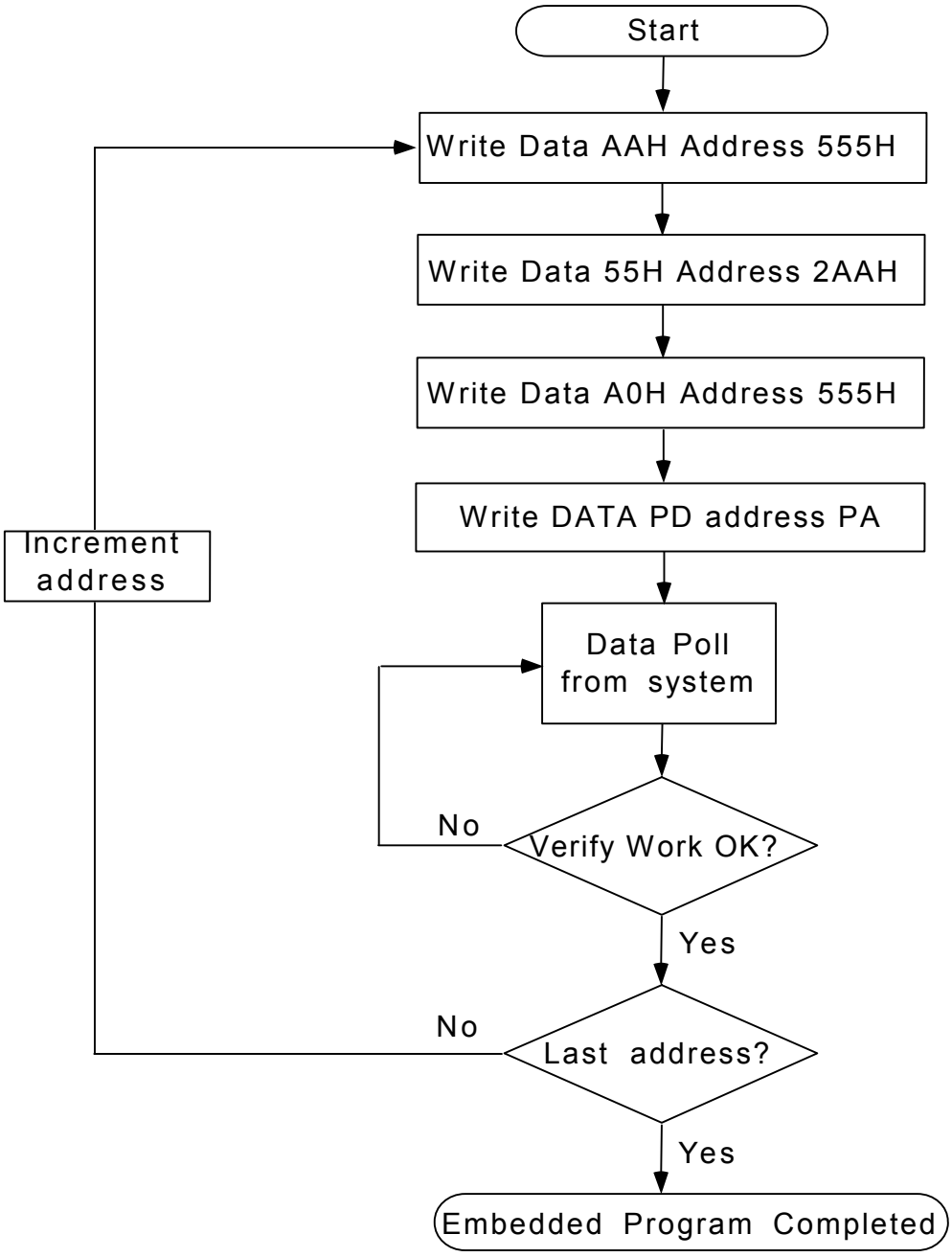
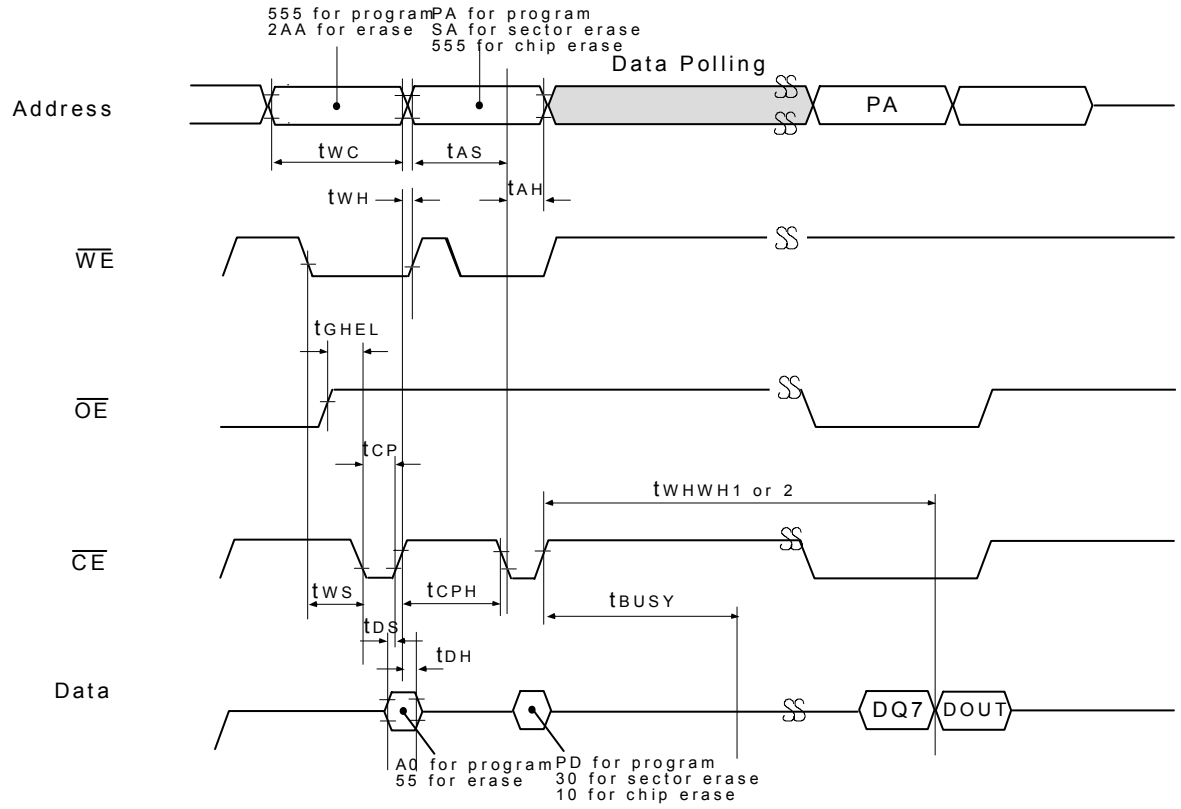


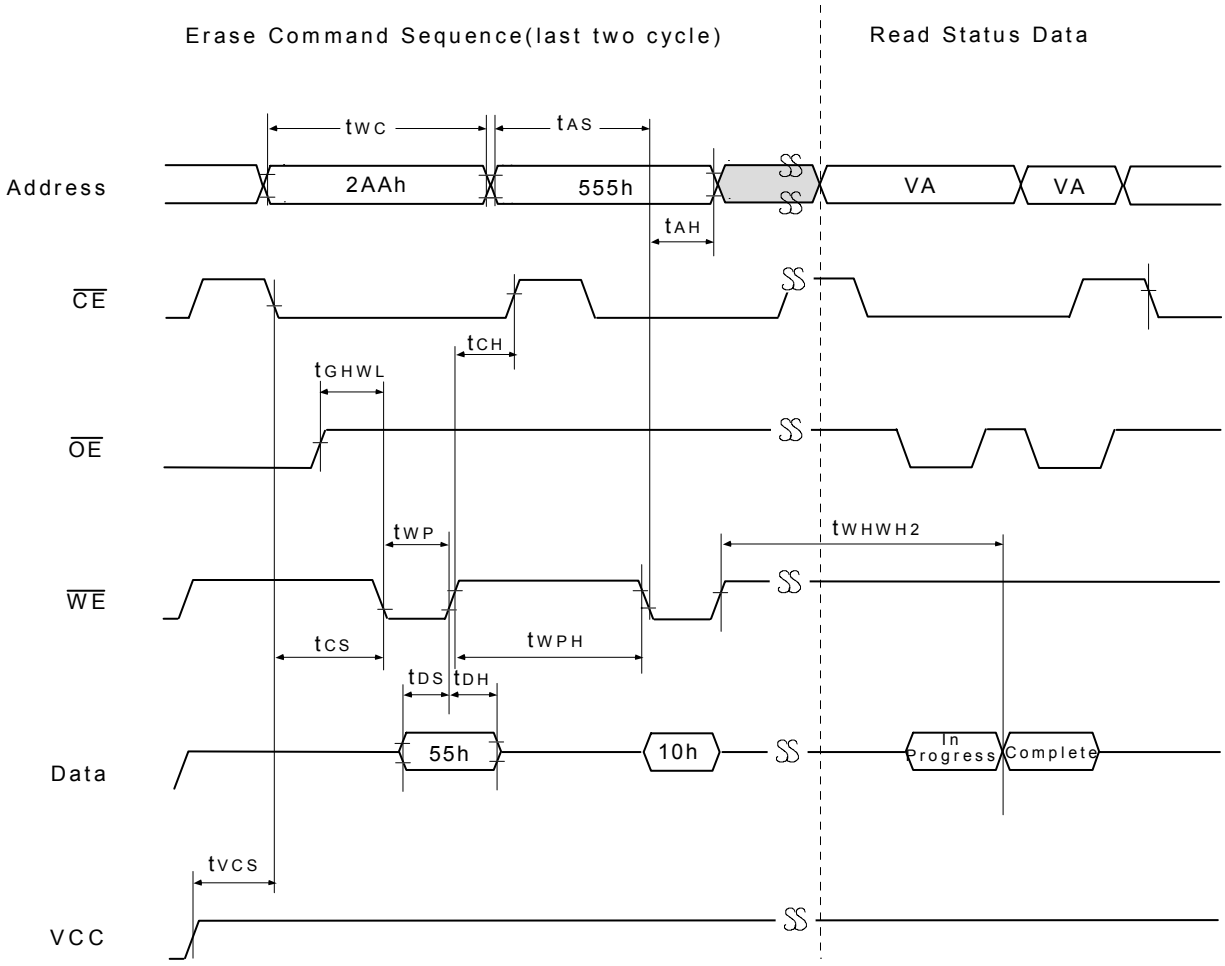
Figure 9. $\overline{CE}$ Controlled Program Timing Waveform



Notes :

1. PA = Program Address, PD = Program Data, DOUT = Data Out , DQ7 = complement of data written to device
2. Figure indicates the last two bus cycles of the command sequence.

Figure 10. Embedded Chip Erase Timing Waveform



Notes :

SA = Sector Address (for Sector Erase, VA = Valid Address for reading status data
(see "Write Operation Status")

Figure 11. Embedded Chip Erase Algorithm Flowchart

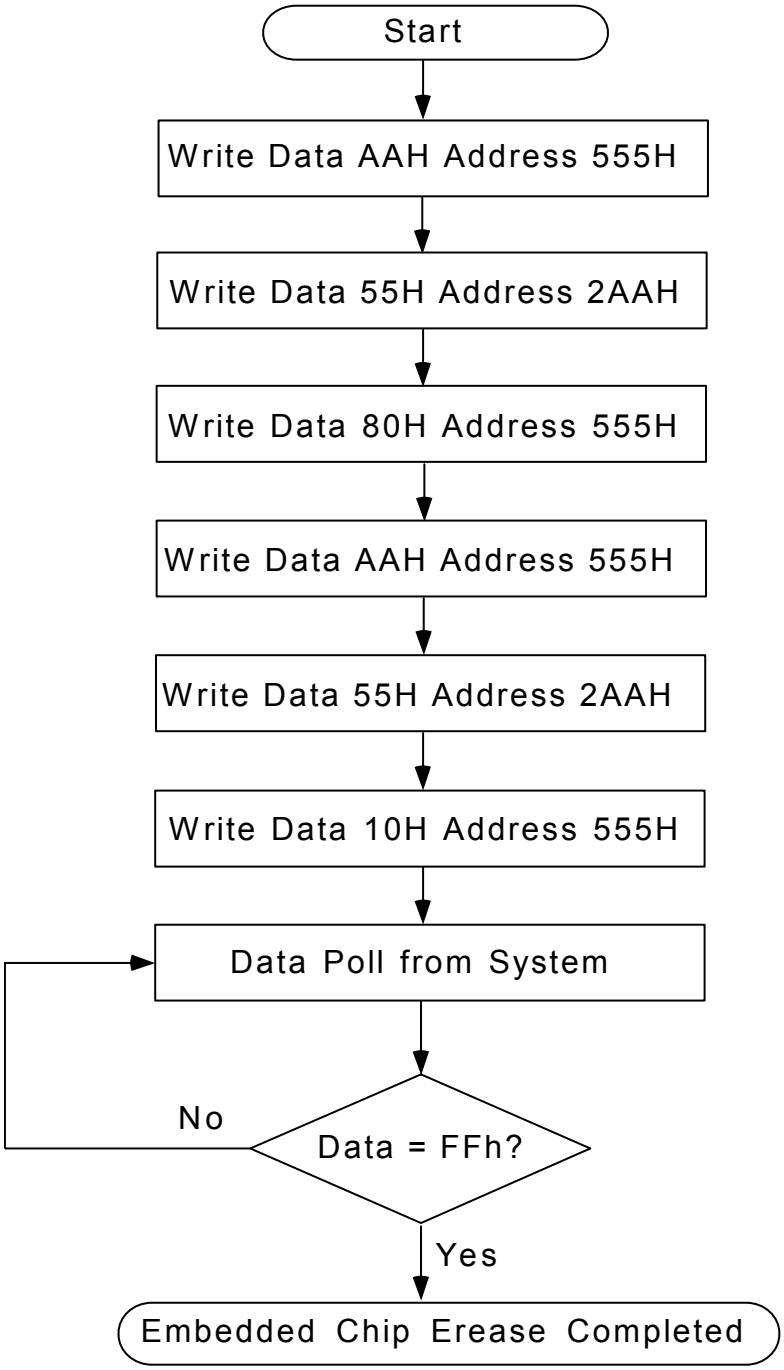
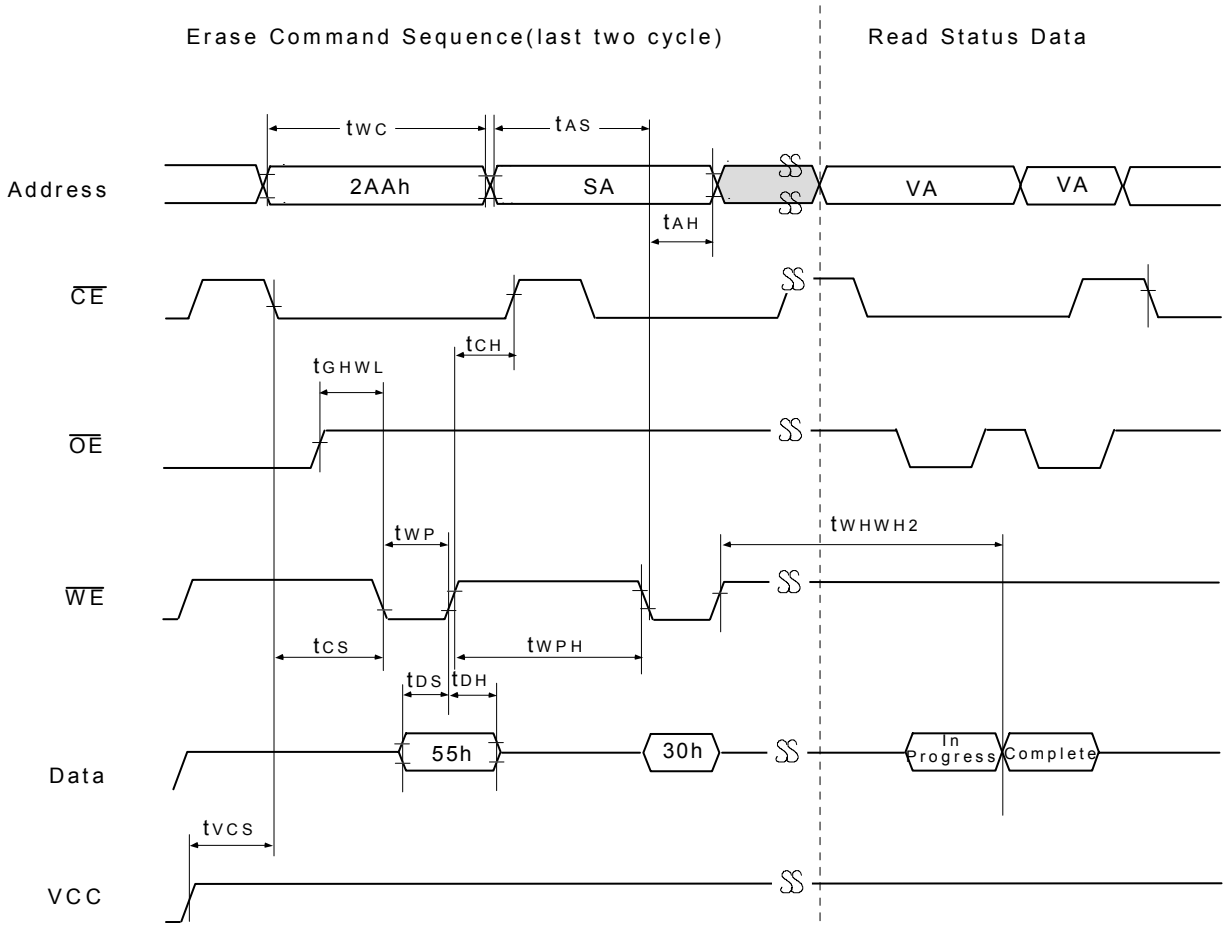


Figure 12. Embedded Sector Erase Timing Waveform



Notes :

SA = Sector Address (for Sector Erase, VA = Valid Address for reading status data (see "Write Operation Status")

Figure 13. Embedded Sector Erase Algorithm Flowchart

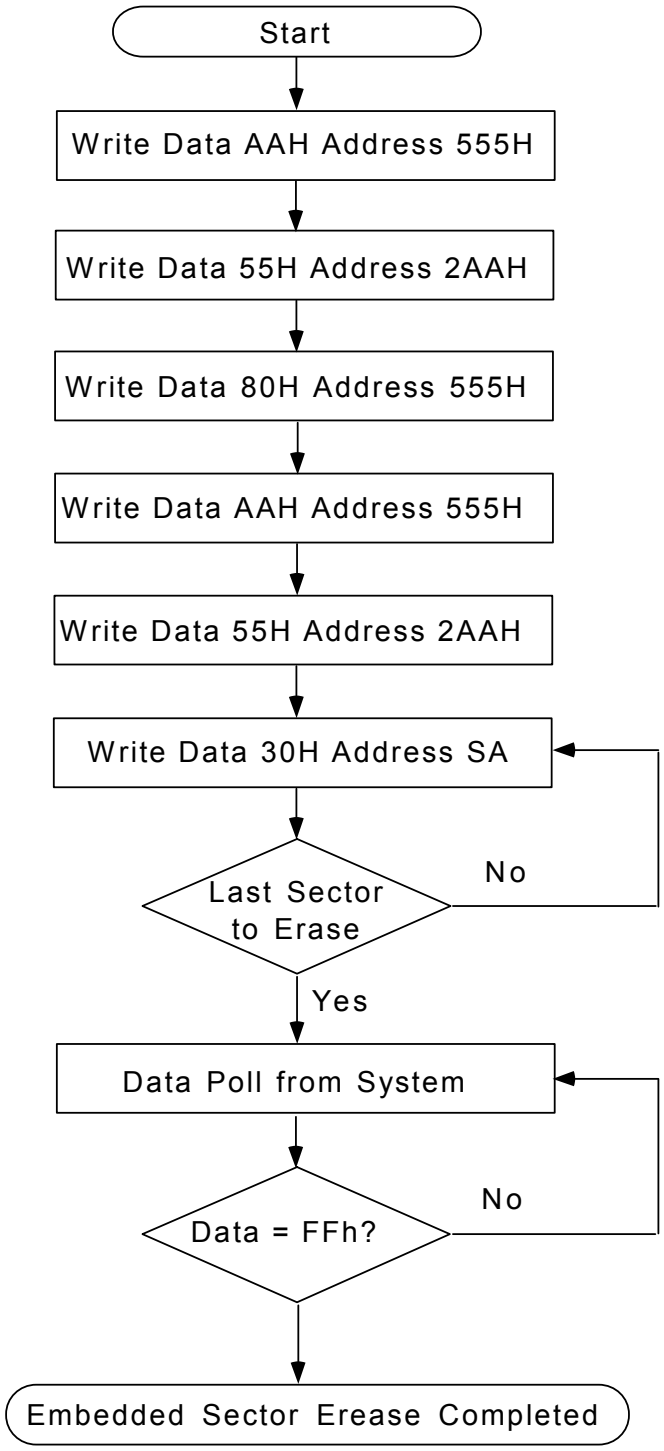


Figure 14. Erase Suspend/Erase Resume Flowchart

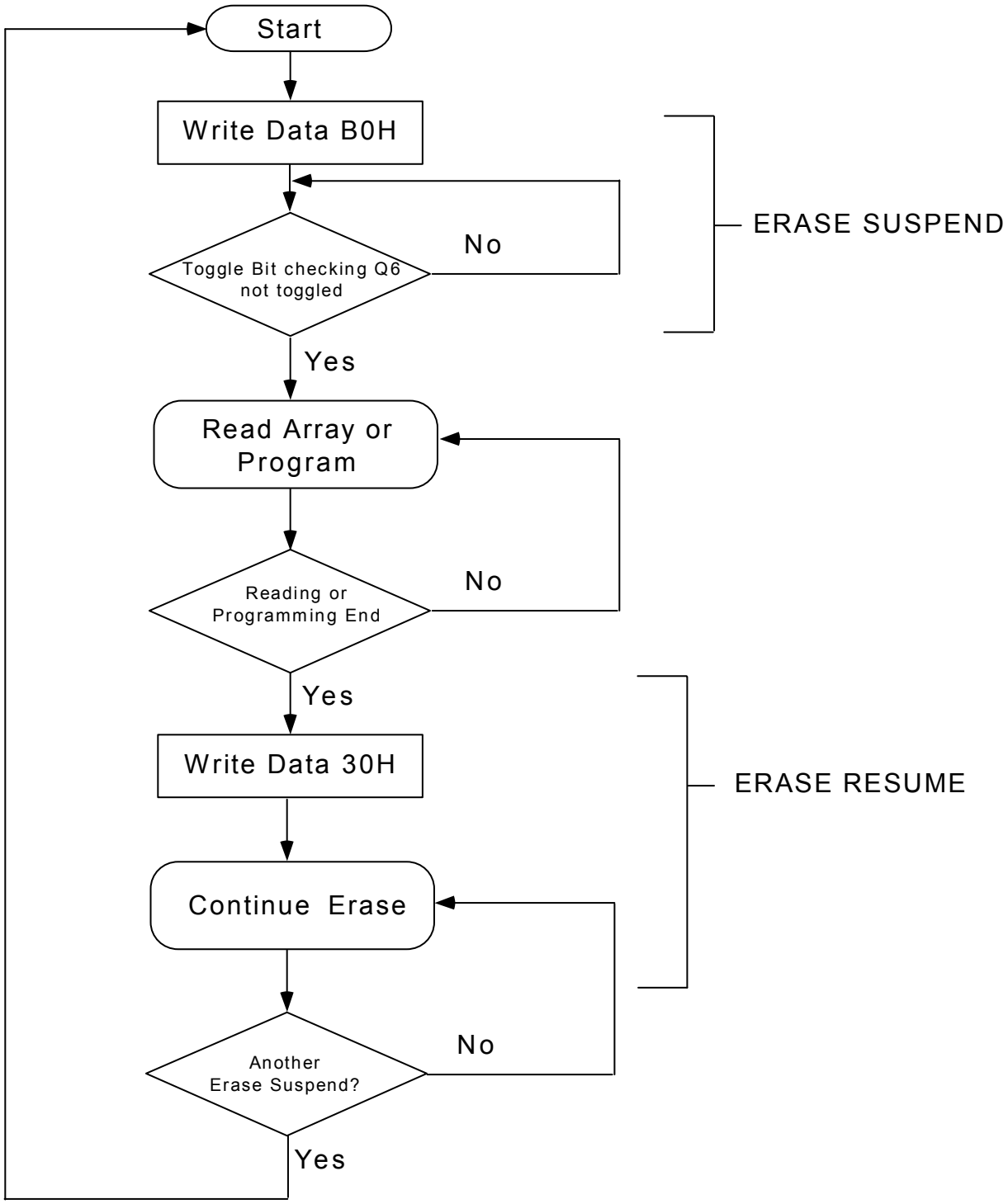


Figure 15. Sector Protect Timing Waveform (A9, $\overline{OE}$ Control)

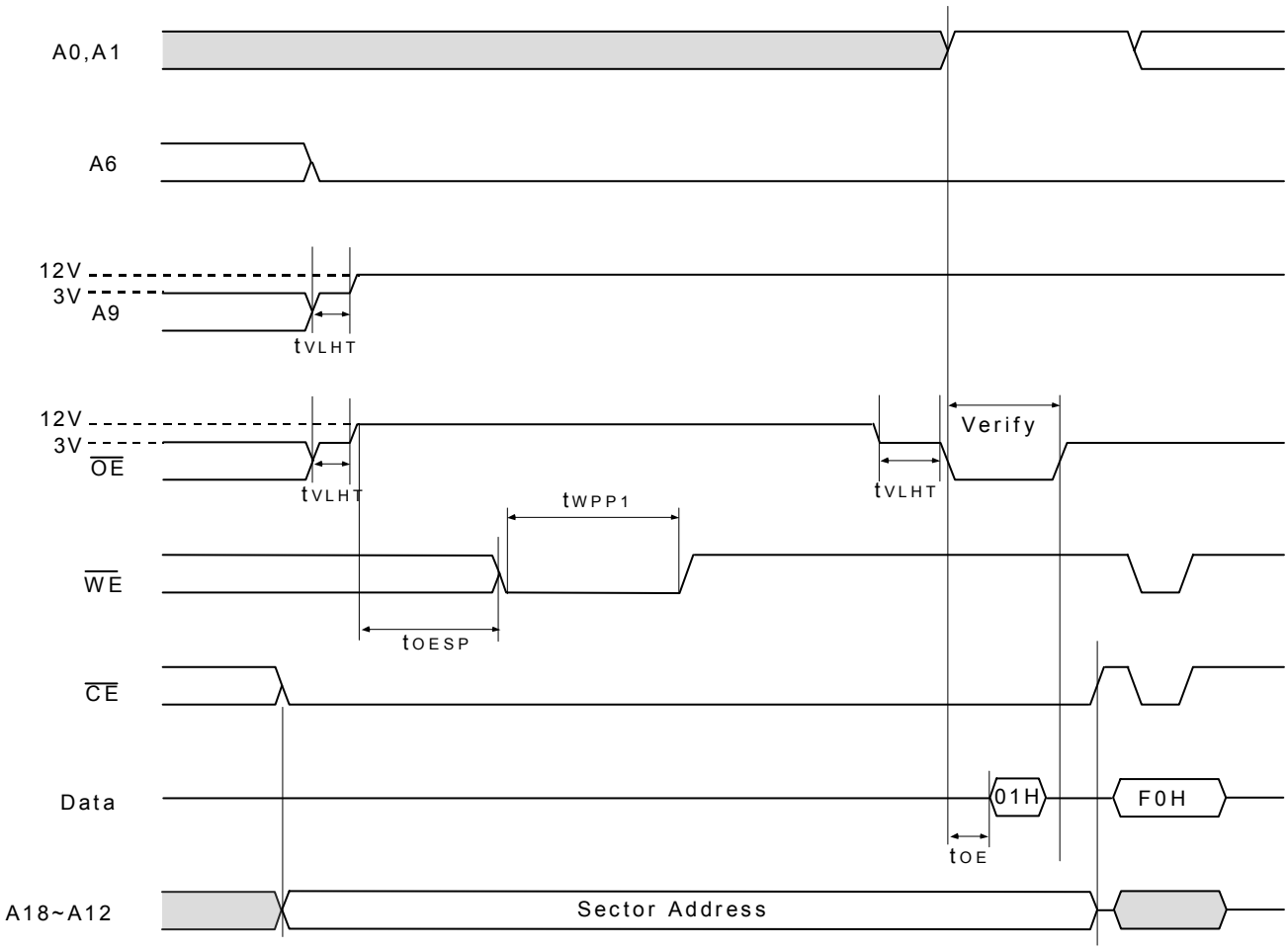
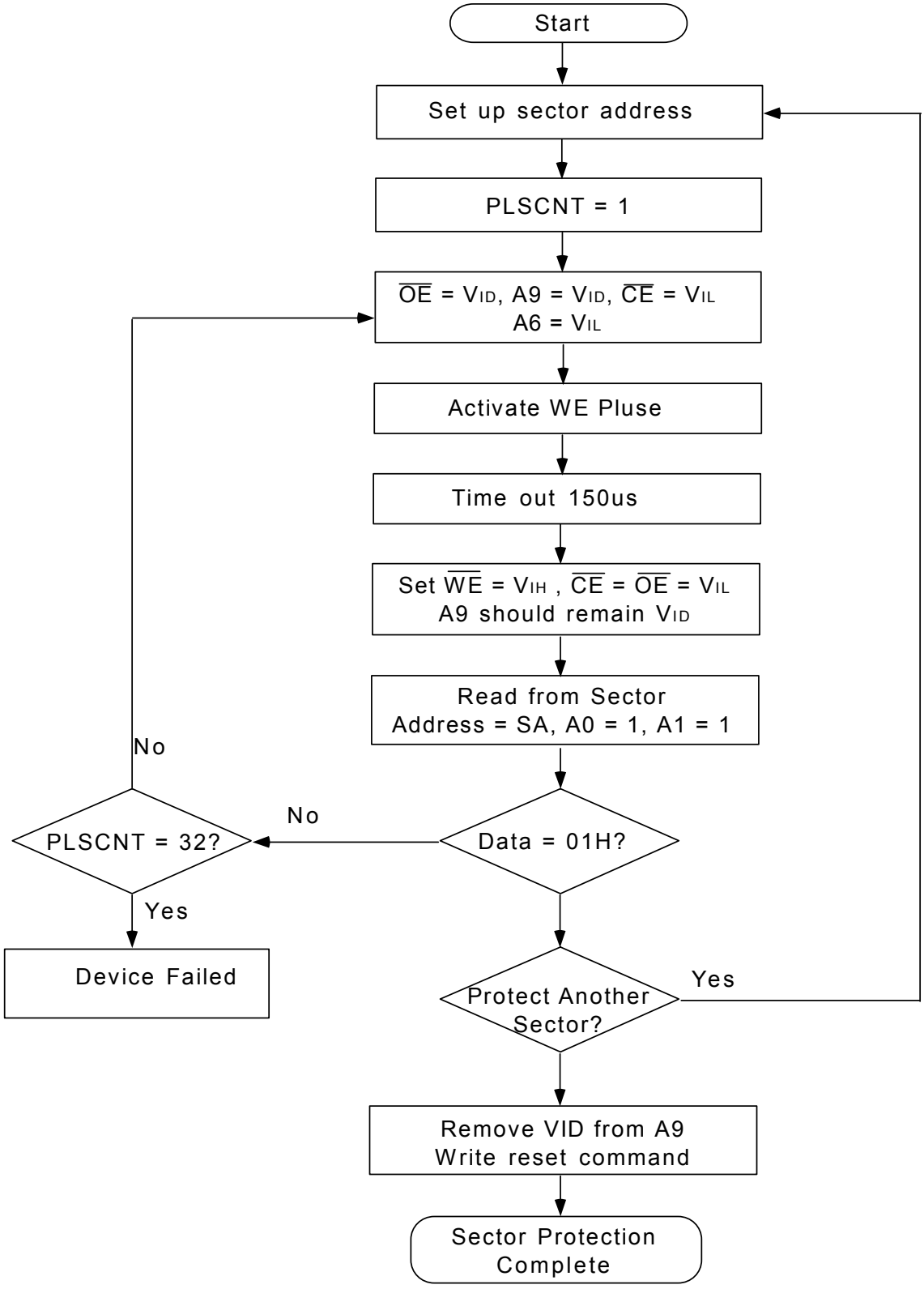
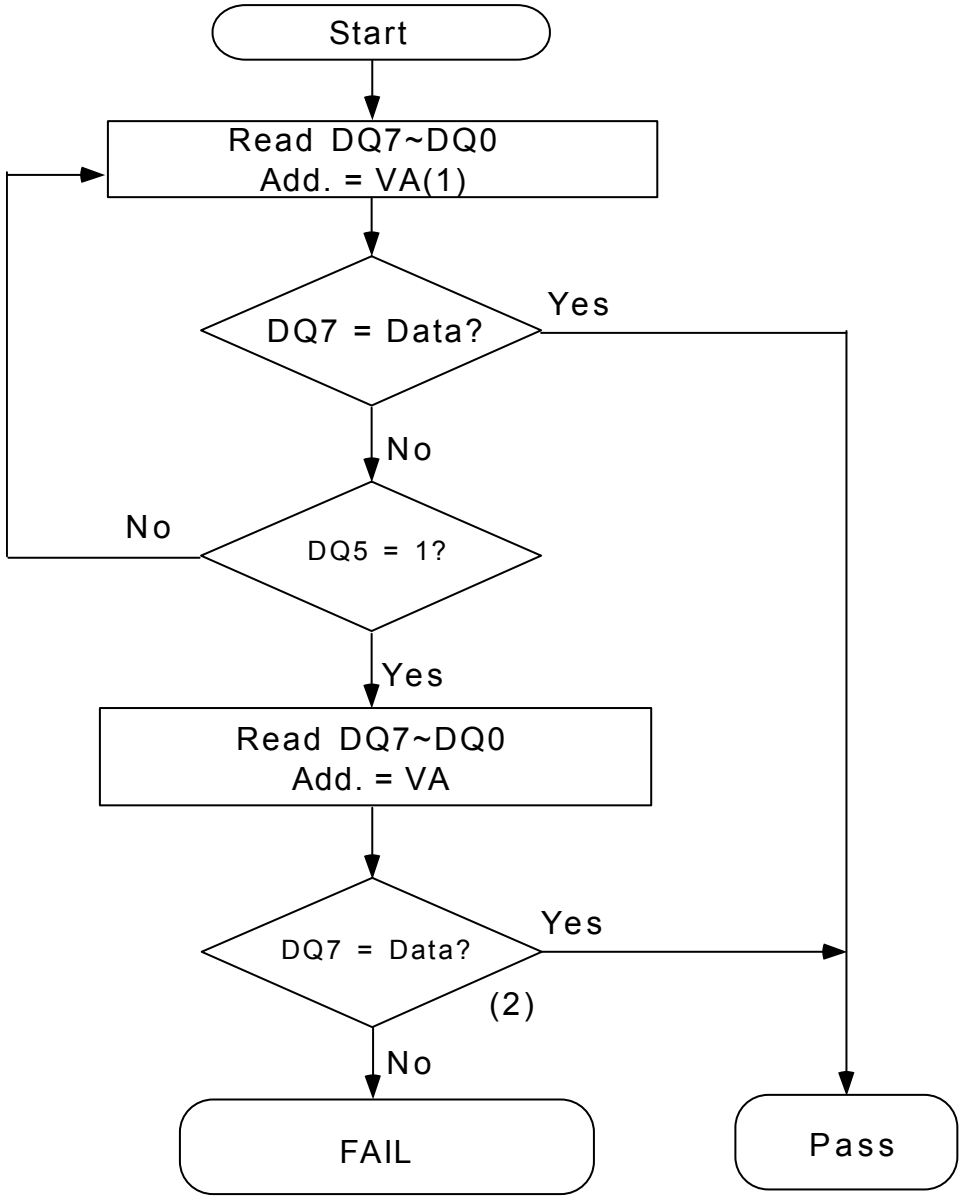


Figure 16. Sector Protection Algorithm (A9, $\overline{OE}$ Control)



WRITE OPERATION STATUS

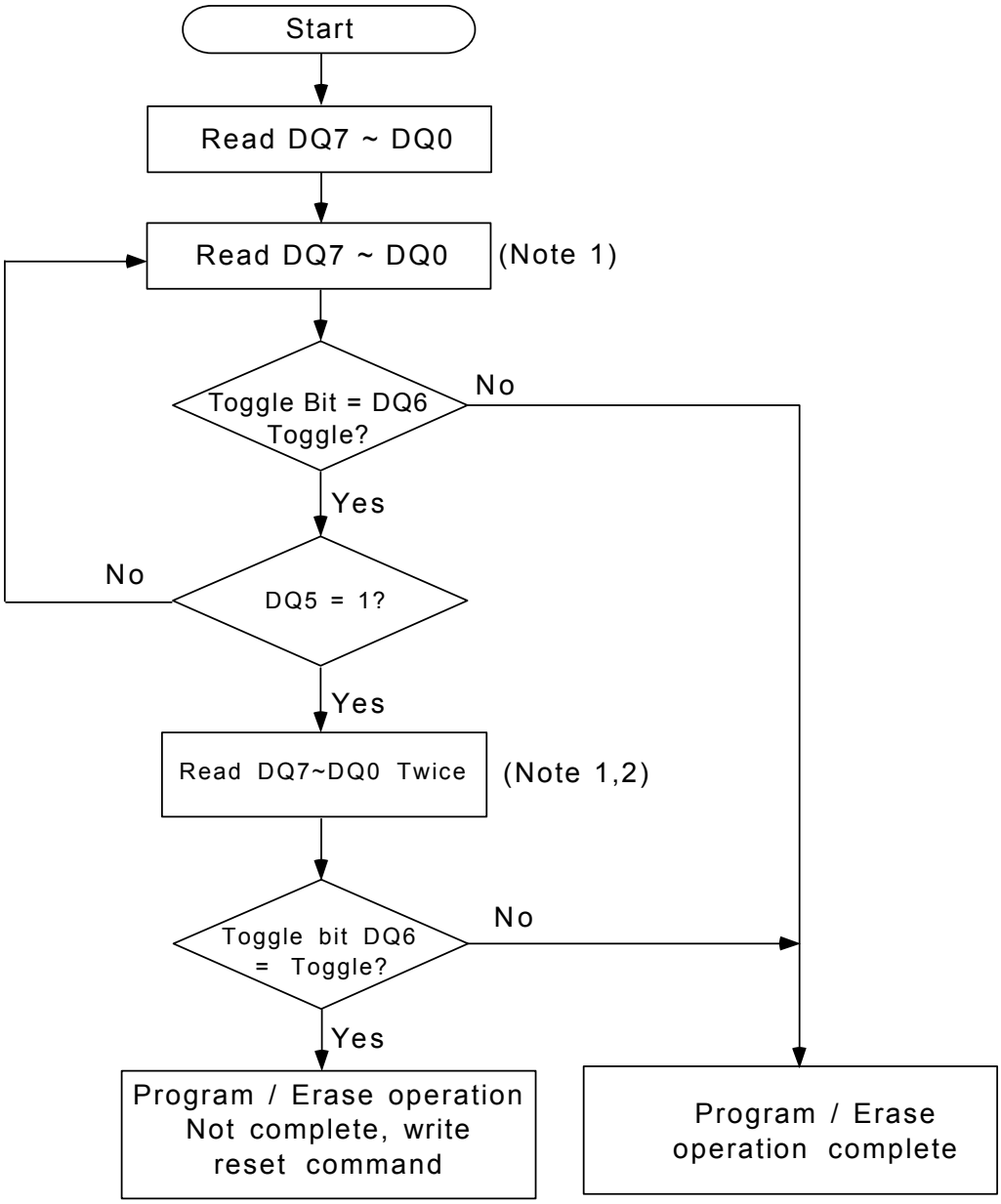
Figure 17. Data Polling Algorithm



Notes :

1. VA =Valid address for programming.
2. DQ7 should be re-checked even DQ5 = "1" because DQ7 may change simultaneously with DQ5.

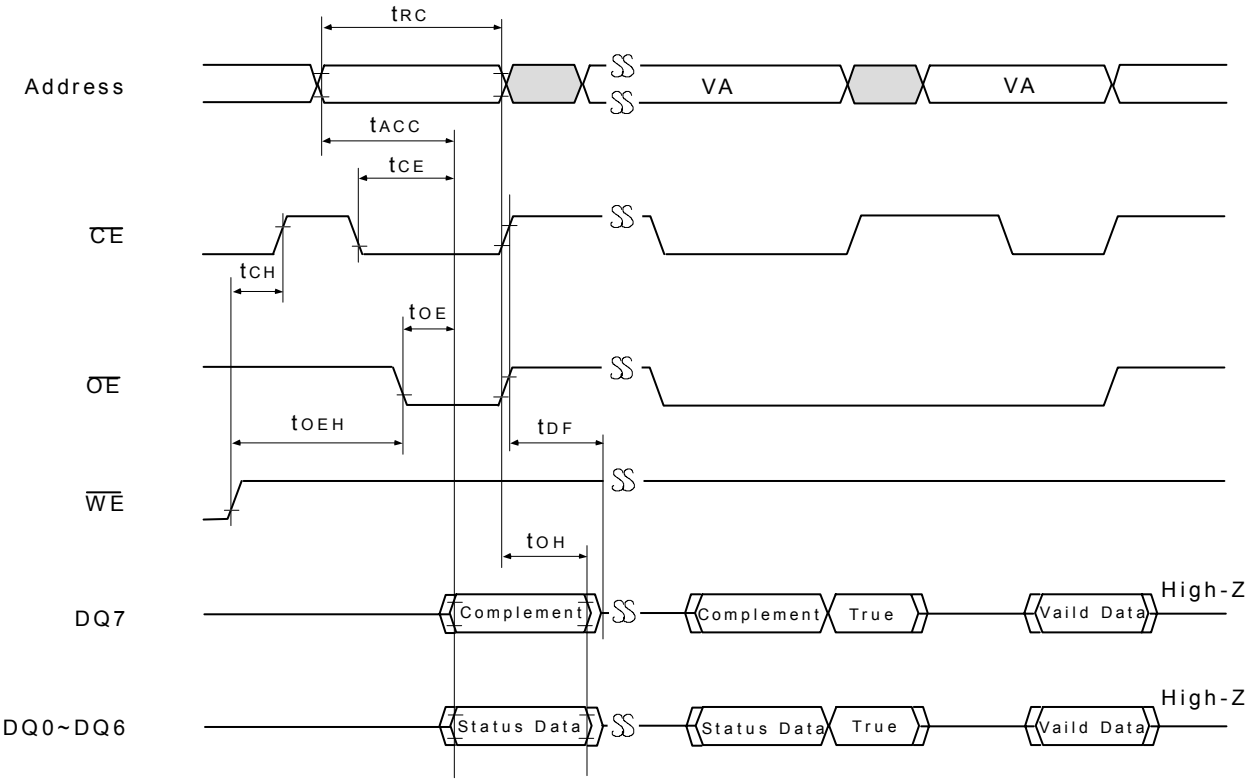
Figure 18. Toggle Bit Algorithm



Note :

1. Read toggle bit twice to determine whether or not it is toggle.
2. Recheck toggle bit because it may stop toggling as DQ5 change to "1".

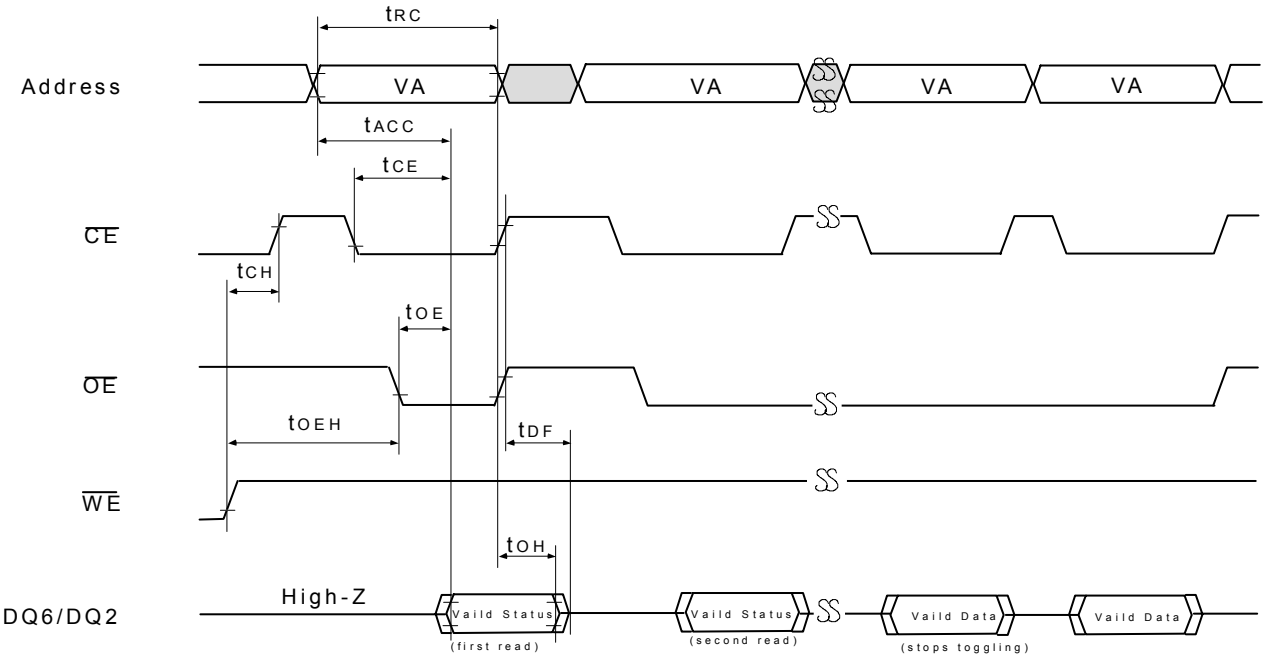
Figure 19. Data Polling Timings (During Embedded Algorithms)



Notes :

VA = Valid Address. Figure shows first status cycle after command sequence, last status read cycle, and array data read cycle.

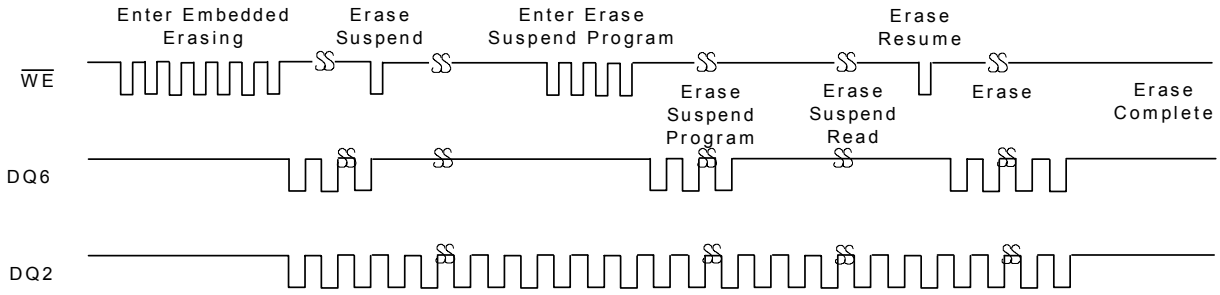
Figure 20. Toggle Bit Timing Waveforms (During Embedded Algorithms)



Notes :

VA = Valid Address; not required for DQ6. Figure shows first status cycle after command sequence, last status read cycle, and array data read cycle.

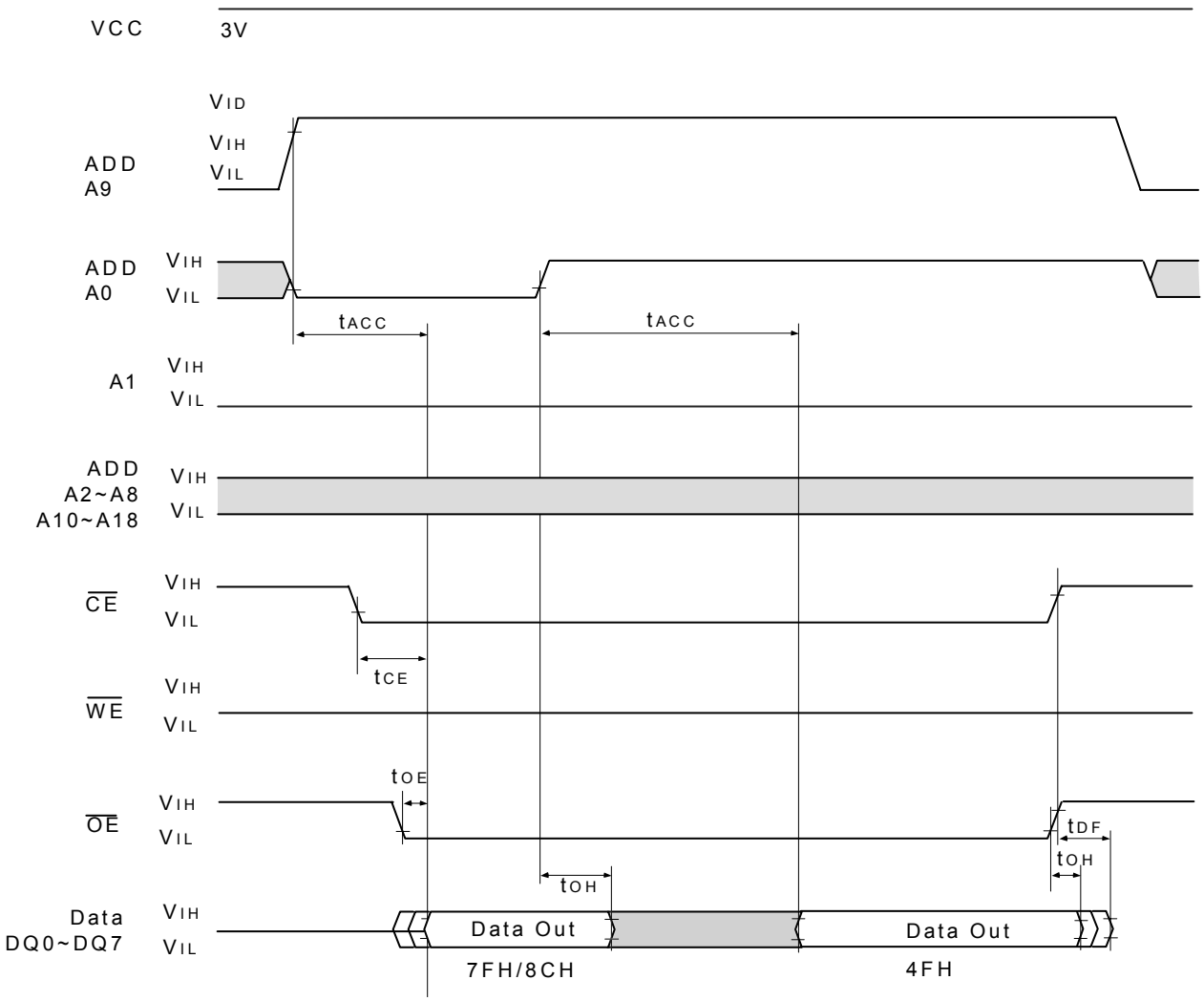
Figure 21. Q6 vs Q2 for Erase and Erase Suspend Operations



Notes :

The system can use OE or CE to toggle DQ2 / DQ6, DQ2 toggles only when read at an address within an erase-suspended.

Figure 22. ID Code Read Timing Waveform



11. ERASE AND PROGRAMMING PERFORMANCE

Table 12. Erase And Programming Performance (Note.1)

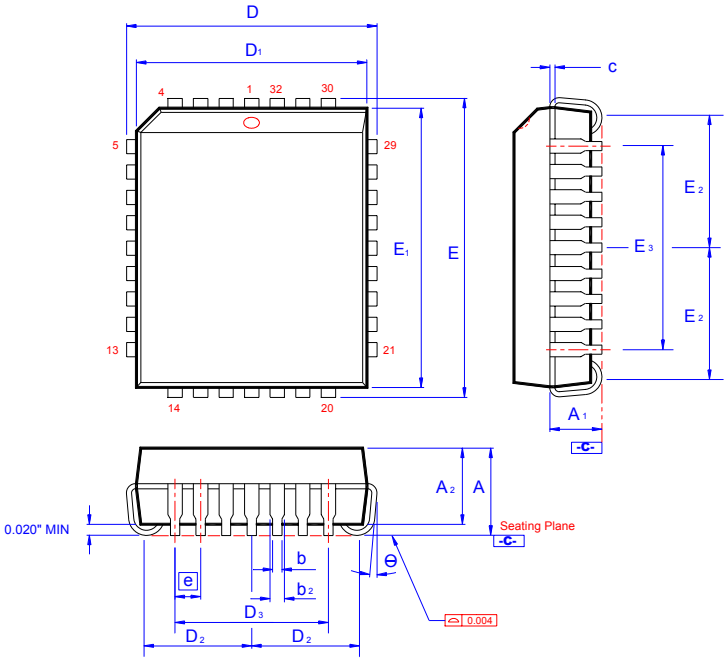
Parameter	Limits			Unit
	Min.	Typ.(2)	Max.(3)	
Sector Erase Time		0.7	15	sec
Chip Erase Time		11	50	sec
Byte Programming Time		9	300	us
Chip Programming Time		4.5	13.5	sec
Erase/Program Cycles	10,000			Cycles

Notes:

1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25°C, 3V.
3.Maximum values measured at 25°C, 3.0V.

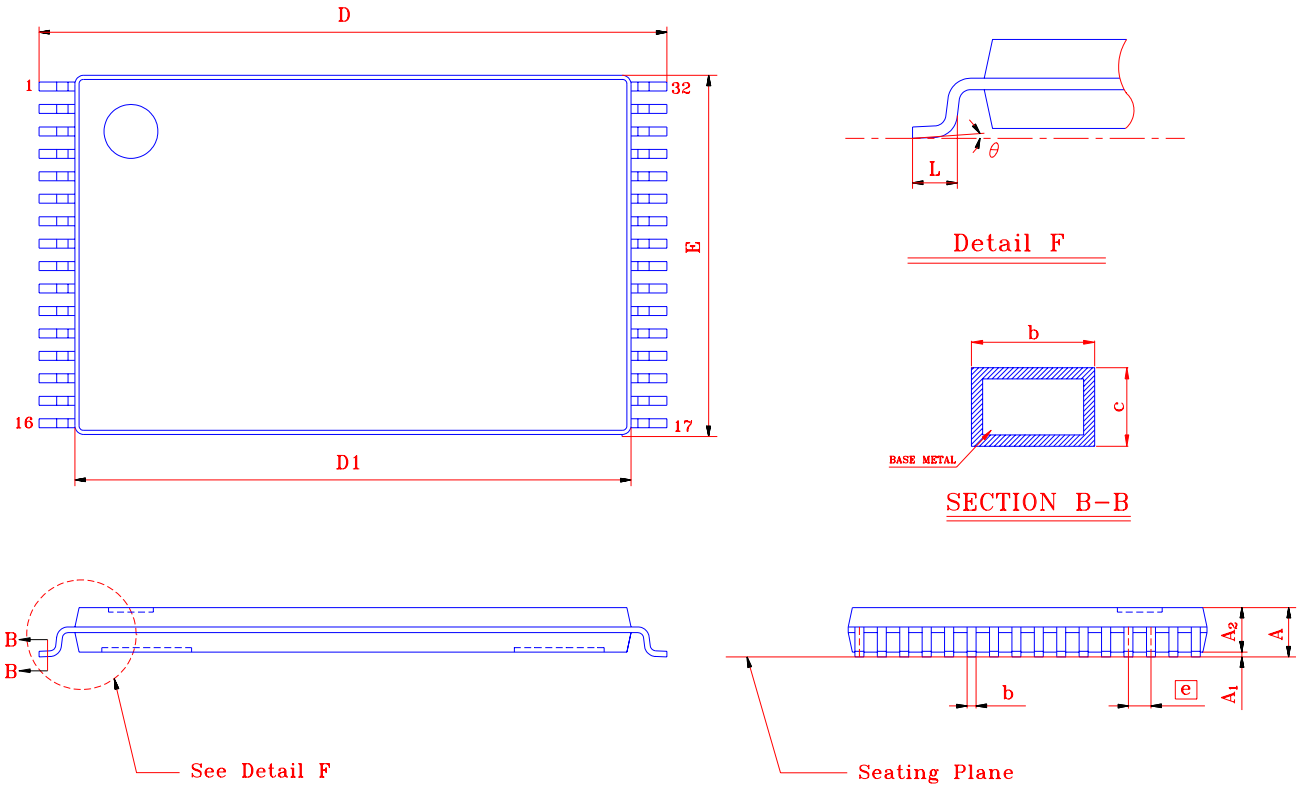
12. PACKAGE DIMENSION

1. 32-LEAD PLCC



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	3.18	-------	3.55	0.125	-------	0.140
A 1	1.53	-------	2.41	0.060	-------	0.095
A 2		2.79 REF			0.110 REF	
b	0.33	-------	0.54	0.013	-------	0.021
b2	0.66	-------	0.82	0.026	-------	0.032
c	0.20	-------	0.36	0.008	-------	0.014
e		1.27 BSC			0.050 BSC	
θ	0^o	-------	10^o	0^o	-------	10^o
E	14.86	14.99	15.11	0.585	0.590	0.595
E 1	13.90	13.97	14.04	0.547	0.550	0.553
E 2	6.05	-------	6.93	0.238	-------	0.273
E 3		10.16 BSC			0.400 BSC	
D	12.32	12.45	12.57	0.485	0.490	0.495
D 1	11.36	11.43	11.50	0.447	0.450	0.453
D 2	4.78	-------	5.66	0.188	-------	0.223
D 3		7.62 BSC			0.300 BSC	

2. 32-LEAD TSOP(I) (8x14 mm)



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	-------	-------	1.20	-------	-------	0.047	D	14.00 BSC			0.551 BSC		
A 1	0.05	-------	0.15	0.006	-------	0.002	D 1	12.40 BSC			0.488 BSC		
A 2	0.95	1.00	1.05	0.037	0.039	0.041	E	8.00 BSC			0.315 BSC		
b	0.17	0.22	0.27	0.007	0.009	0.011	e	0.50 BSC			0.020 BSC		
c	0.10	-------	0.21	0.004	-------	0.008	L	0.50	0.60	0.70	0.020	0.024	0.028
							θ	0^o	-------	5^o	0^o	-------	5^o

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