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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM6216514I Series

Wide Temperature Range Version
8 M SRAM (512-kword × 16-bit)



ADE-203-1303B (Z)
Rev. 1.0
Oct. 23, 2002

Description

The Hitachi HM6216514I Series is 8-Mbit static RAM organized 524,288-word × 16-bit. HM6216514I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.

Features

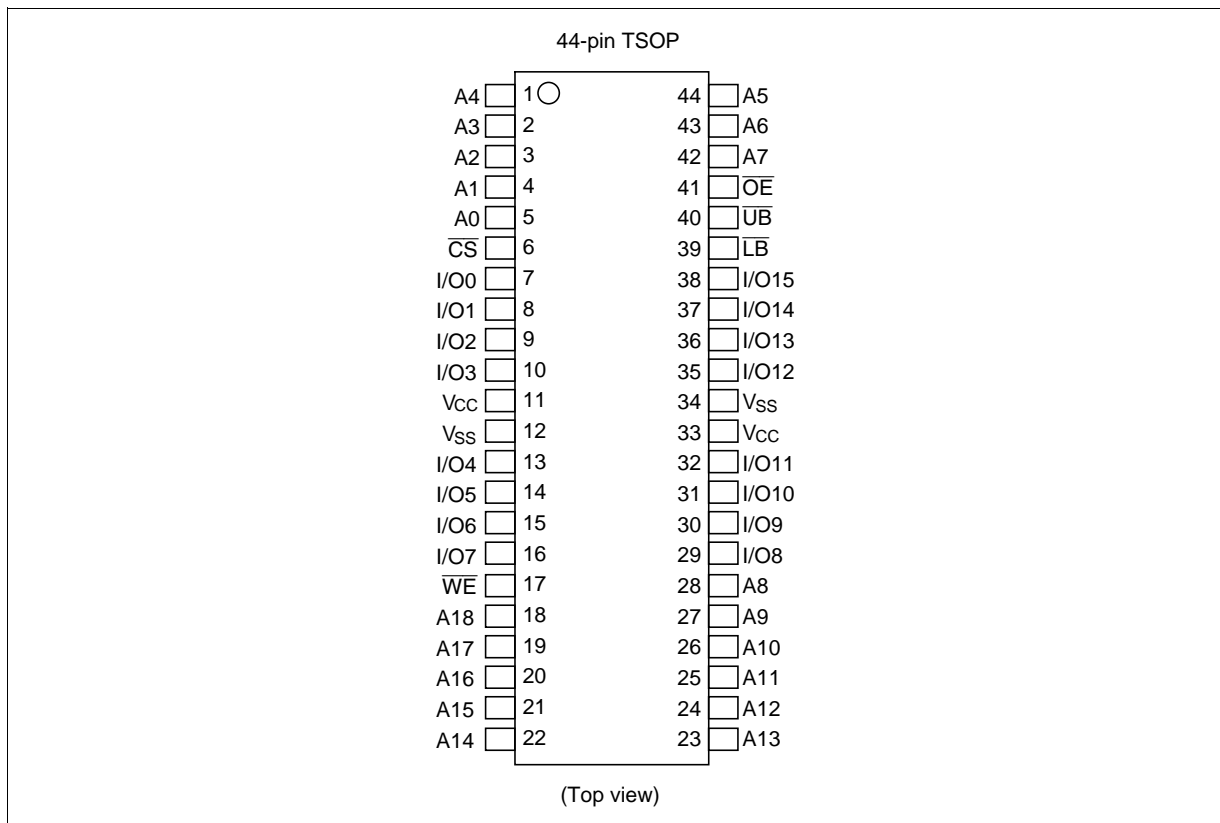
- Single 5.0 V supply: 5.0V ± 10 %
- Fast access time: 55 ns (Max)
- Power dissipation:
 - Active: 10 mW/MHz (Typ)
 - Standby: 7.5 μW (Typ)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
- Temperature range: -40 to +85°C

HM6216514I Series

Ordering Information

Type No.	Access time	Package
HM6216514LTTI-5SL	55 ns	400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DE)

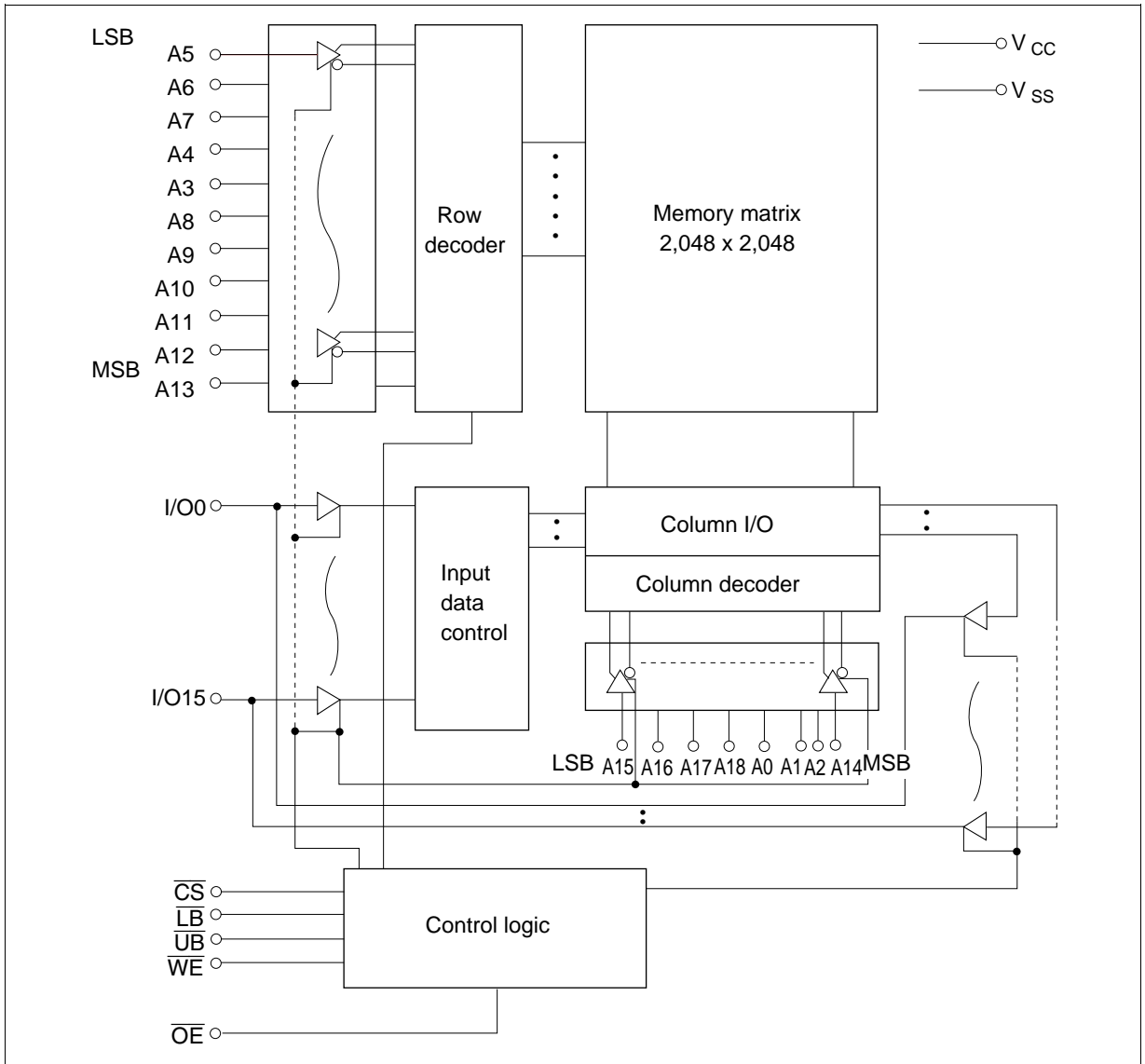
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O15	Data input/output
\overline{CS}	Chip select
\overline{WE}	Write enable
\overline{OE}	Output enable
\overline{LB}	Lower byte select
\overline{UB}	Upper byte select
V _{cc}	Power supply
V _{ss}	Ground

Block Diagram



Operation Table

\overline{CS}	\overline{WE}	\overline{OE}	\overline{UB}	\overline{LB}	I/O0 to I/O7	I/O8 to I/O15	Operation
H	x	x	x	x	High-Z	High-Z	Standby
x	x	x	H	H	High-Z	High-Z	Standby
L	H	L	L	L	Dout	Dout	Read
L	H	L	H	L	Dout	High-Z	Lower byte read
L	H	L	L	H	High-Z	Dout	Upper byte read
L	L	x	L	L	Din	Din	Write
L	L	x	H	L	Din	High-Z	Lower byte write
L	L	x	L	H	High-Z	Din	Upper byte write
L	H	H	x	x	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , x: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5 ^{*1} to $V_{CC} + 0.3$ ^{*2}	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width \leq 30 ns.

2. Maximum voltage is +7.0 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	—	0.8	V	1
Ambient temperature range	T_a	-40	—	85	°C	

Note: 1. V_{IL} min: -3.0 V for pulse half-width \leq 30 ns.

DC Characteristics

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}
Operating current	I_{CC}	—	—	20	mA	$\overline{CS} = V_{IL}$, Others = V_{IH}/V_{IL} , $I_{I/O} = 0$ mA
Average operating current	I_{CC1}	—	16	35	mA	Min. cycle, duty = 100%, $I_{I/O} = 0$ mA, $\overline{CS} = V_{IL}$, Others = V_{IH}/V_{IL}
	I_{CC2}	—	2	5	mA	Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0$ mA, $\overline{CS} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current	I_{SB}	—	0.1	0.3	mA	$\overline{CS} = V_{IH}$
Standby current	I_{SB1}	—	0.8	10	μA	$0 \text{ V} \leq V_{in}$ (1) $\overline{CS} \geq V_{CC} - 0.2$ V or (2) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2$ V, $\overline{CS} \leq 0.2$ V
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1$ mA
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1$ mA

Notes: 1. Typical values are at $V_{CC} = 5.0$ V, $T_a = +25^\circ\text{C}$ and not guaranteed.

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1.0$ MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0$ V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: $V_{IL} = 0.4\text{ V}$, $V_{IH} = 2.2\text{ V}$
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (50 pF) (Including scope and jig)

Read Cycle

Parameter	Symbol	HM6216514I		Unit	Notes
		-5			
		Min	Max		
Read cycle time	t_{RC}	55	—	ns	
Address access time	t_{AA}	—	55	ns	
Chip select access time	t_{ACS}	—	55	ns	
Output enable to output valid	t_{OE}	—	35	ns	
Output hold from address change	t_{OH}	10	—	ns	
\overline{LB} , \overline{UB} access time	t_{BA}	—	55	ns	
Chip select to output in low-Z	t_{CLZ}	10	—	ns	2, 3
\overline{LB} , \overline{UB} enable to low-z	t_{BLZ}	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ}	0	20	ns	1, 2, 3
\overline{LB} , \overline{UB} disable to high-Z	t_{BHZ}	0	20	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1, 2, 3

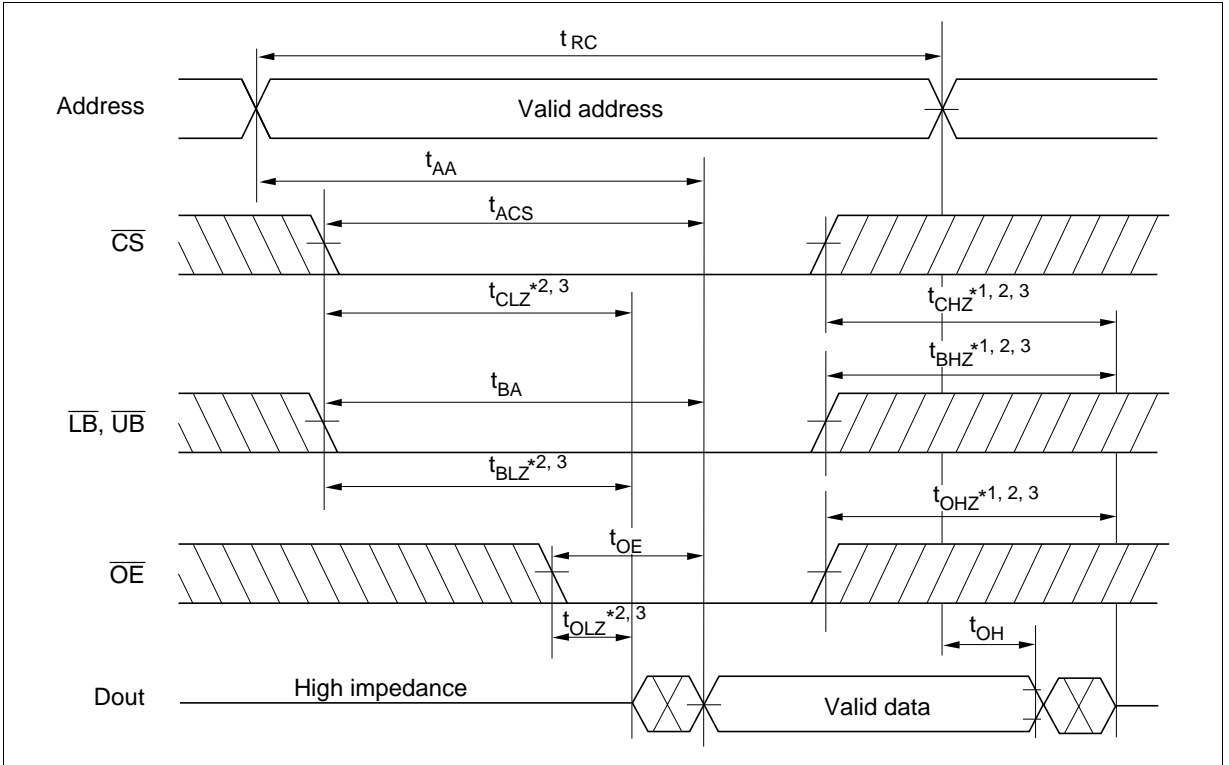
Write Cycle

Parameter	Symbol	HM6216514I		Unit	Notes
		-5			
		Min	Max		
Write cycle time	t_{WC}	55	—	ns	
Address valid to end of write	t_{AW}	50	—	ns	
Chip selection to end of write	t_{CW}	50	—	ns	5
Write pulse width	t_{WP}	40	—	ns	4
\overline{LB} , \overline{UB} valid to end of write	t_{BW}	50	—	ns	
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	0	—	ns	7
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	20	ns	1, 2

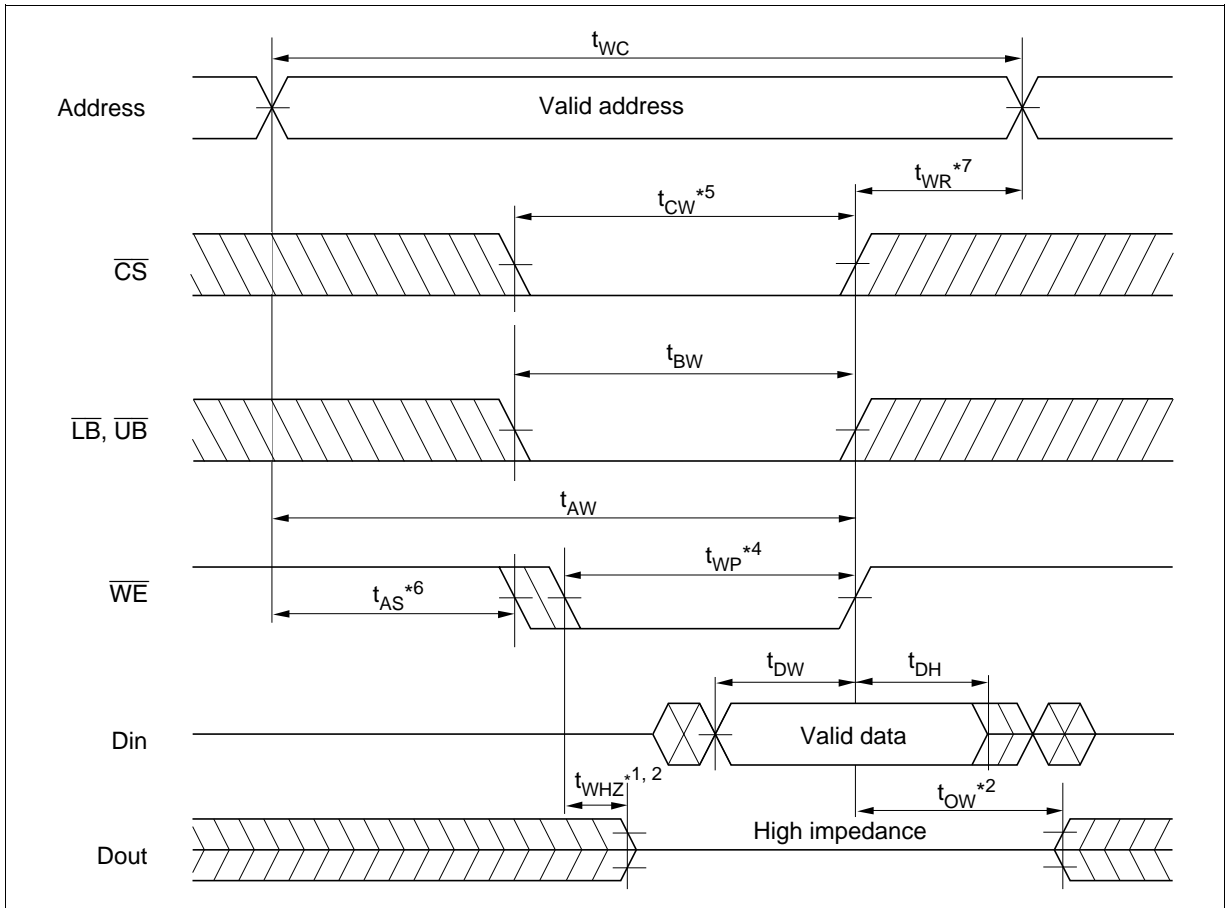
- Notes:
- t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is sampled and not 100% tested.
 - At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 - A write occurs during the overlap of a low \overline{CS} , a low \overline{WE} and a low \overline{LB} or a low \overline{UB} . A write begins at the latest transition among \overline{CS} going low, \overline{WE} going low and \overline{LB} going low or \overline{UB} going low. A write ends at the earliest transition among \overline{CS} going high, \overline{WE} going high and \overline{LB} going high or \overline{UB} going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from the later of \overline{CS} going low to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earliest of \overline{CS} or \overline{WE} going high to the end of write cycle.

Timing Waveform

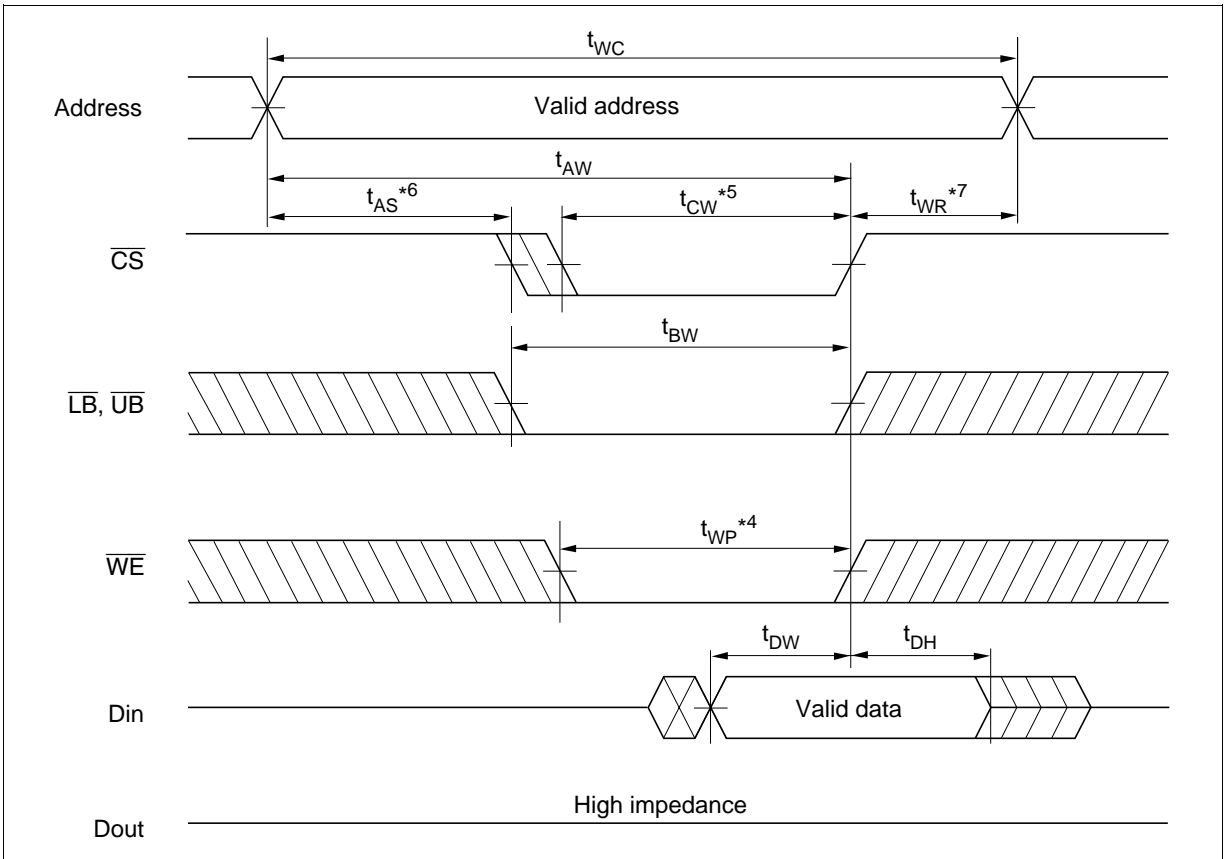
Read Cycle



Write Cycle (1) (\overline{WE} Clock)

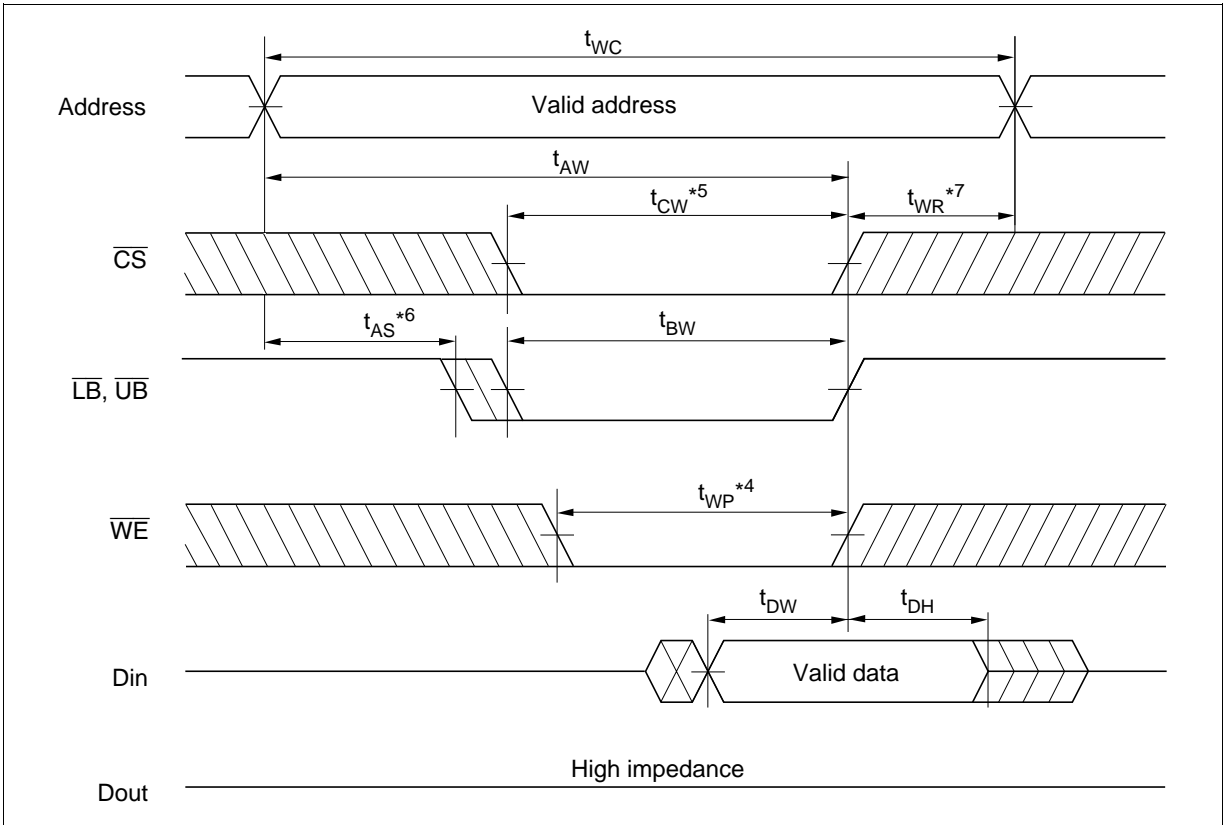


Write Cycle (2) (\overline{CS} Clock, $\overline{OE} = V_{IH}$)



HM6216514I Series

Write Cycle (3) (\overline{LB} , \overline{UB} Clock, $\overline{OE} = V_{IH}$)



Low V_{CC} Data Retention Characteristics ($T_a = -40$ to $+85^\circ\text{C}$)

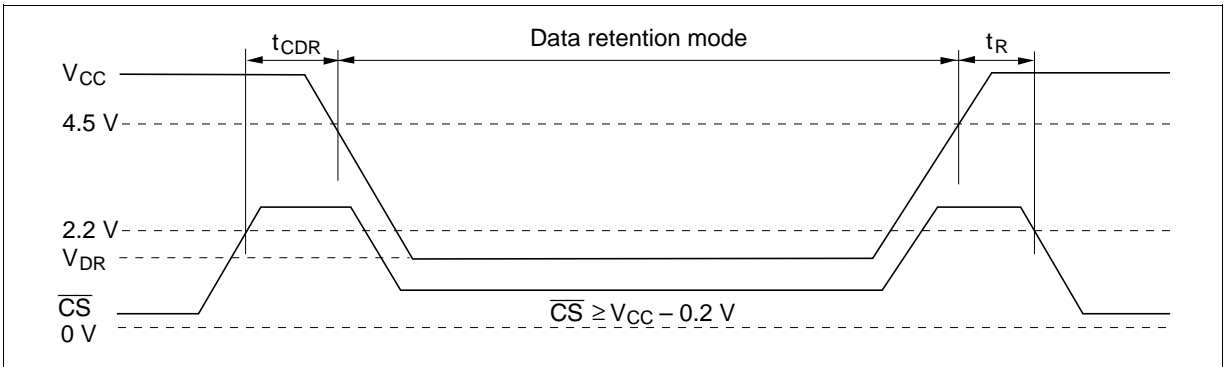
Parameter	Symbol	Min	Typ* ²	Max	Unit	Test conditions* ¹
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{in} \geq 0V$ (1) $\overline{CS} \geq V_{CC} - 0.2V$ or (2) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ $\overline{CS} \leq 0.2V$
Data retention current	I_{CCDR}	—	0.8	10	μA	$V_{CC} = 3.0V$, $V_{in} \geq 0V$ (1) $\overline{CS} \geq V_{CC} - 0.2V$ or (2) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ $\overline{CS} \leq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC} * ³	—	—	ns	

Notes: 1. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, \overline{LB} , \overline{UB} buffer and D_{in} buffer. If \overline{CS} controls data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , \overline{LB} , \overline{UB} , I/O) can be in the high impedance state. If \overline{LB} , \overline{UB} controls data retention mode, \overline{LB} , \overline{UB} must be $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$, \overline{CS} must be $\overline{CS} \leq 0.2V$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

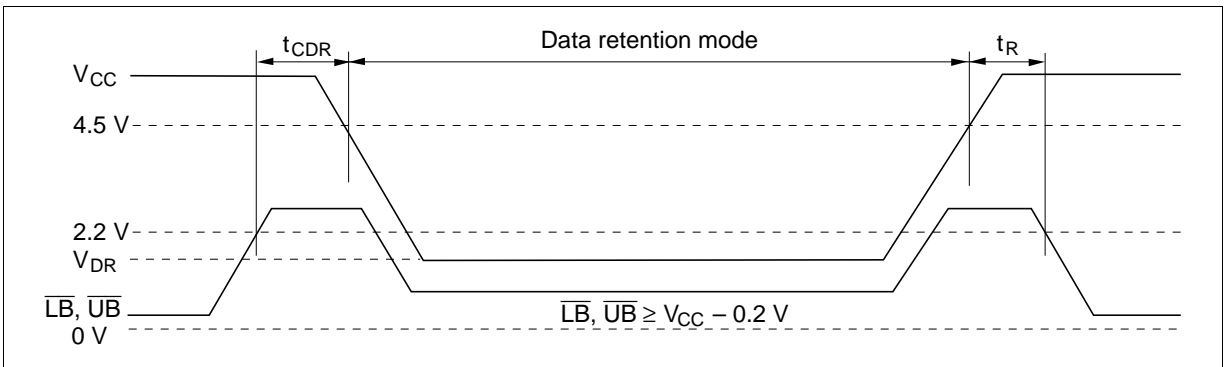
2. Typical values are at $V_{CC} = 3.0V$, $T_a = +25^\circ\text{C}$ and not guaranteed.

3. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) (\overline{CS} Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (\overline{LB} , \overline{UB} Controlled)

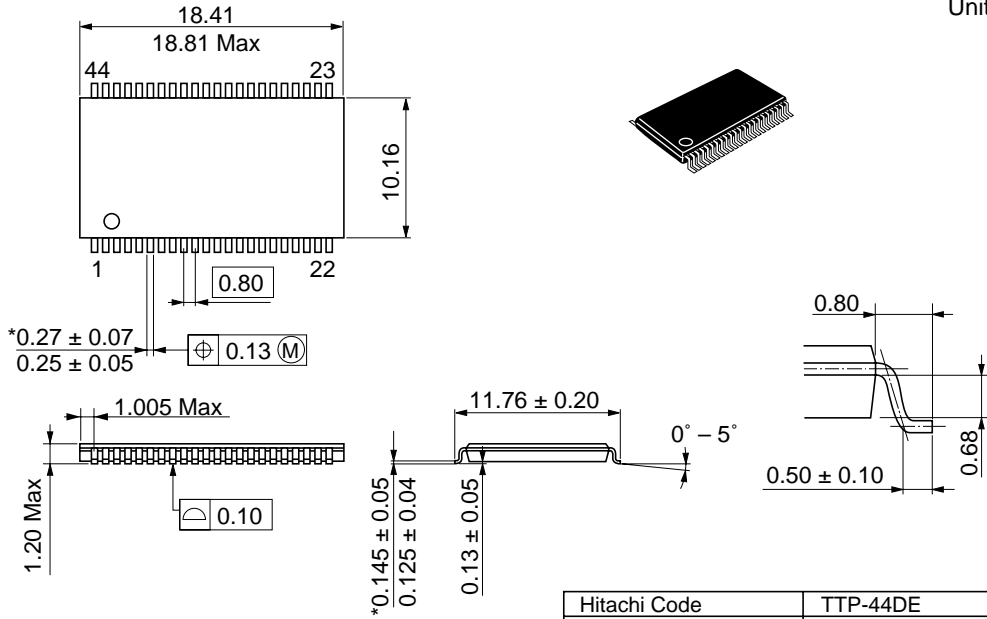


Package Dimensions

HM6216514LTTI Series (TTP-44DE)

As of January, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
JEITA	—
Mass (reference value)	0.43 g

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