Ordering number : ENN7817

SANYO Semiconductors

DATA SHEET

Monolithic Linear IC

LA6565 — Five-Channel CD Actuator Driver (BTL: 4 channels, H bridge: 1 channel)

Overview

The LA6565 is a four-channel BTL plus one-channel H bridge actuator driver developed for use in CD and DVD drives. The BTL driver channels 1 and 2 include built-in operational amplifiers allowing the LA6565 to support a wide range of applications.

Application

- Five-channel (BTL: 4 channels, H bridge: 1 channel) CD motor driver

Features and Functions

- Five power amplifier channels on a single chip (Bridge connection (BTL): 4 channels, H bridge: 1 channel)
- IO max: 1 A
- Built-in level shifters (except for the H bridge channel)
- Muting circuits (output on/off, two systems)
  (The muting circuits operate for the BTL amplifiers. They do not apply to the H bridge or regulator circuits.)
- Built-in regulator (Uses an external pnp transistor and is set with an external resistor.)
- Output voltage setting function (loading driver)
- Built-in independent operational amplifiers
- Thermal shutdown circuit

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Specified PCB*	2	W
Maximum output current	I_O max	For each of the channel 1 to 4 and H bridge outputs	1	A
Maximum input voltage	VINB		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–55 to +150	°C

Note *:Specified PCB (76.1mm × 114.3mm × 1.6mm), PCB meterial : glass epoxy

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8$ V, $V_{REF} = 2.5$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall]						
Quiescent current when on	ICC-ON	BTL amplifier output on, loading block off*1		30	50	mA
Quiescent current when off	ICC-OFF	All outputs off*1		10	15	mA
Thermal shutdown circuit operating temperature	TSD	*7	150	175	200	°C
[VREF Amplifier]						
VREF amplifier offset voltage	VREF-OFFSET		–10		+10	mV
VREF input voltage range	VREF-IN		1		V_{CC} – 1.5	V
VREF-OUT output current	I-VREF-OUT			1		mA
[Operational Amplifier] (Independent)						
Input voltage range	VIN (OP)		0		V_{CC} – 1.5	V
Output current (sink)	SINK (OP)		2			mA
Output current (source)	SOURCE (OP)		300	500		µA
Output offset voltage	VOFF (OP)		–10		+10	mV
Residual current (sink)	VCE-SINK (OP)	I_O (sink side) = 1 mA			0.6	V
[BTL Amplifier Block] (Channels 1 to 4)						
Output offset voltage	VOFF	The voltage difference between each channel outputs*2, *3	–50		+50	mV
Input voltage range	VIN	Input voltage range of the input operational amplifiers	0		V_{CC} – 1.5	V
Output voltage	V_O	Io = 0.5 A, the voltage between V_O^+ and V_O^- in each channel	5.7	6.2		V
Closed circuit voltage gain	VG	The gain from the input to the output with the input amplifier set to 0 dB*2, *3	7.2	8	9	times
Slew rate	SR	For the independent amplifier. Times 2 when between outputs.*7		0.5		V/µs
Muting on voltage	VMUTE-ON	The output on voltage, for each mute function*4	2.5			V
Muting off voltage	VMUTE-OFF	The output off voltage, for each mute function*4			0.5	V
[Input Amplifier Block] (Channels 1 and 2)						
Input voltage range	VIN-OP		0		V_{CC} – 1.5	V
Output current (sink)	SINK-OP		2			mA
Output current (source)	SOURCE-OP	*5	300	500		µA
Output offset voltage	VOFF-OP		–10		+10	mV
[Loading Block] (Channel 5, H bridge circuit)						
Output voltage	VO-LOAD	For forward/reverse operation, Io = 0.5 A, VCONT = V_{CC} *	5.7	6.5		V
Braking output saturation voltage	VCE-BREAK	The output voltage during braking*6			0.3	V
Low-level input voltage	VIN-L				1	V
High-level input voltage	VIN-H		2			V
[Power Supply Block] (Uses an external 2SB632K pnp transistor)						
Power supply output	VOUT	I_O = 200 mA	1.260	1.285	1.310	V
REG-IN sink current	REG-IN-SINK	External pnp transistor base current	5	10		mA
Line regulation	ΔVOLN	6 V ≤ V_{CC} ≤ 12 V, I_O = 200 mA		10	100	mV
Load regulation	ΔVOLD	5 mA ≤ I_O ≤ 200 mA		10	100	mV

*1: The total current dissipation for VCCP1, VCCP2, and VCCS with no load.

*2: The input amplifier is a buffer amplifier.

*3: The voltage difference between the two sides of the load (12 Ω).

*4: When the MUTE pin is high, the output will be on, and when low, the output will be off (high-impedance state).

*5: The input operational amplifier source is constant current. Since the 11 kΩ resistor between this and the next stage functions as the load, the input operational amplifier gain must be set carefully.

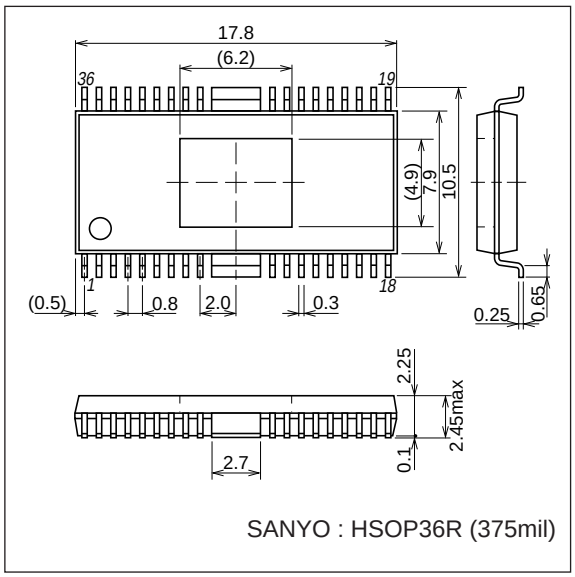
*6: The braking operation is a short (to ground) braking operation. The sink side output is on at this time.

*7: Design guarantee.

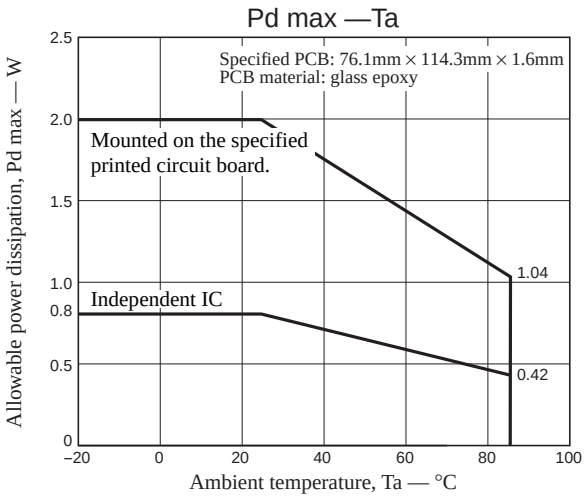
Package Dimensions

unit : mm

3251



SANYO : HSOP36R (375mil)



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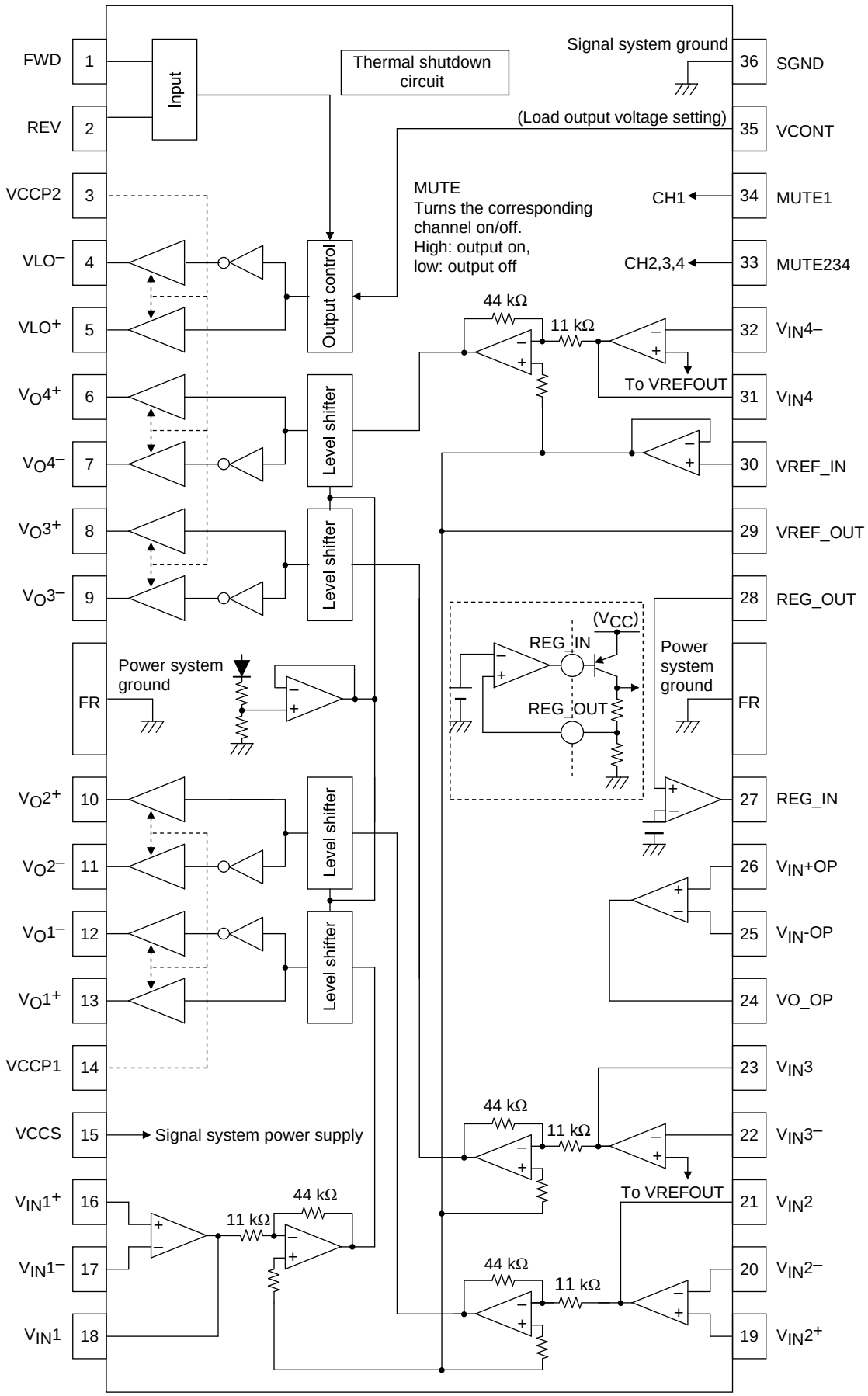
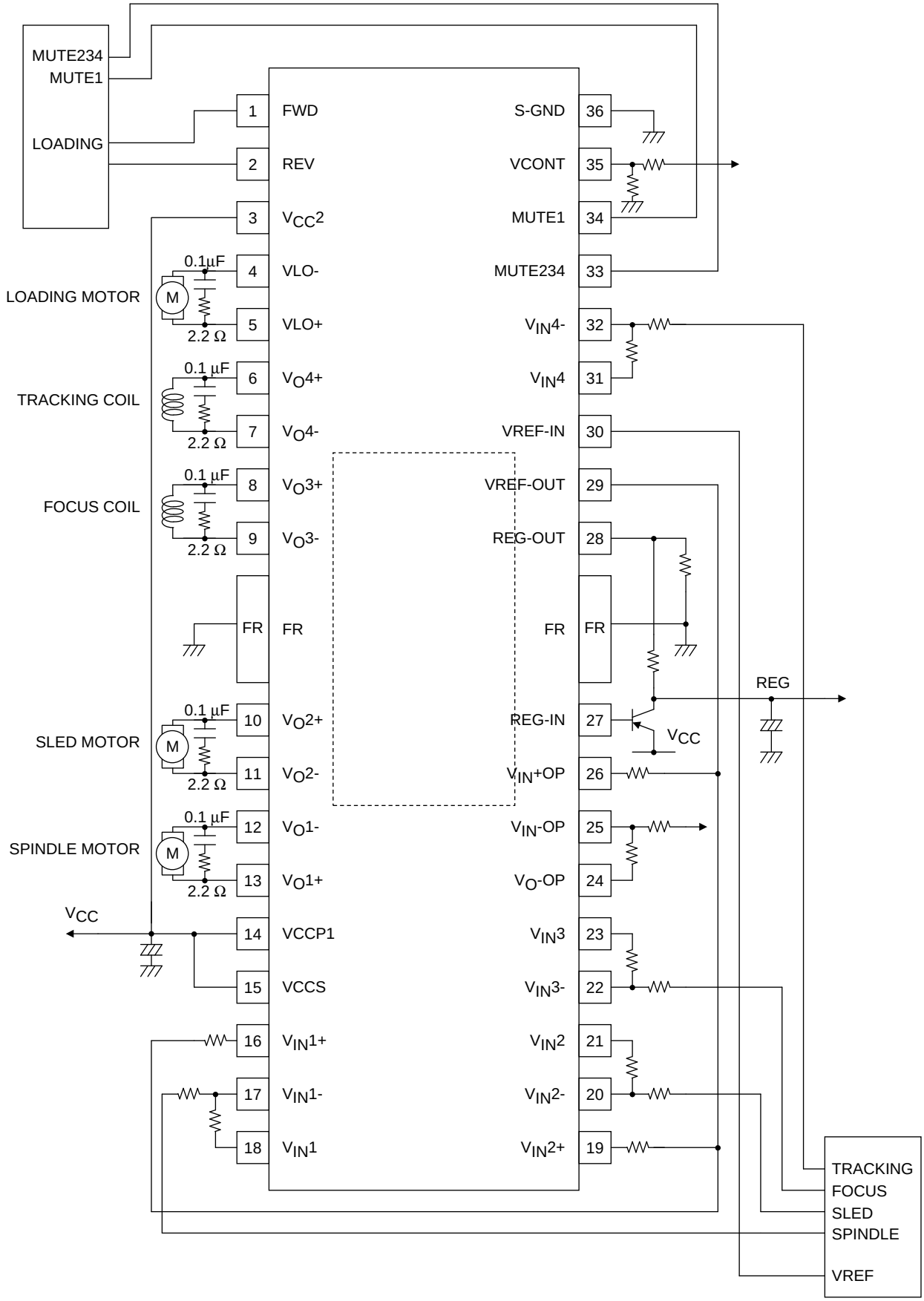
Internal Block Diagram



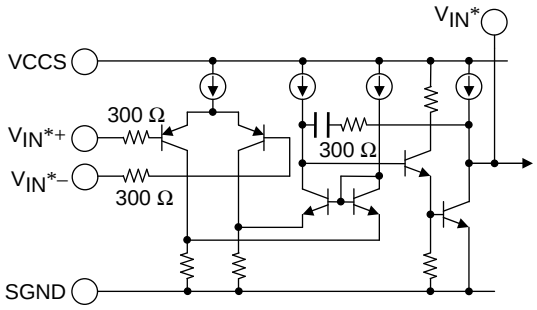
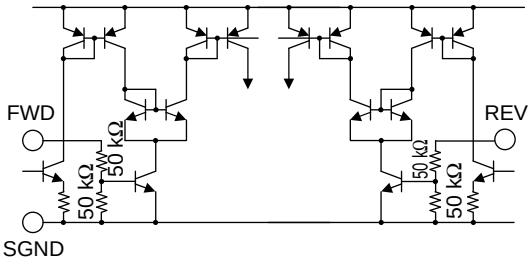
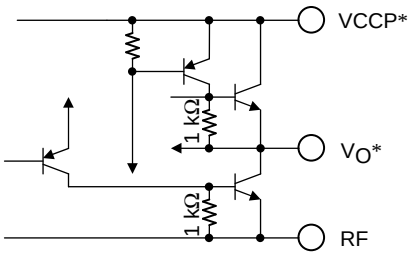
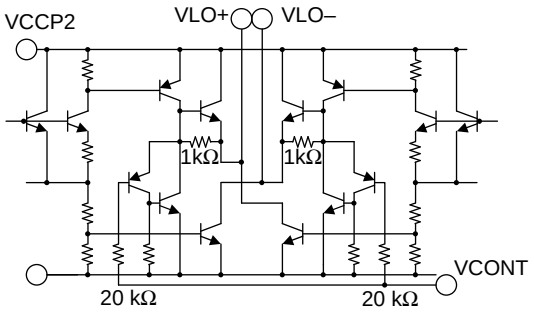
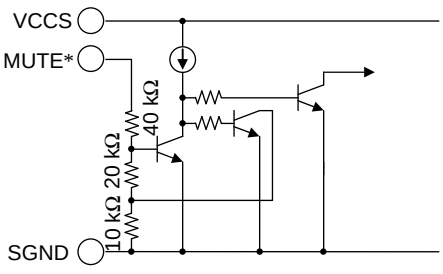
Sample Application Circuit



Pin Functions

Pin No.	Pin Name	Pin Descriptions
1	FWD	Loading output direction switching (FWD). Loading system logic input.
2	REV	Loading output direction switching (REV). Loading system logic input.
3	$V_{CC}2$	Channels 3, 4, and loading power stage power supply
4	VLO−	Loading output (–)
5	VLO+	Loading output (+)
6	VO4+	Channel 4 output (+)
7	VO4–	Channel 4 output (–)
8	VO3+	Channel 3 output (+)
9	VO3−	Channel 3 output (–)
10	VO2+	Channel 2 output (+)
11	VO2−	Channel 2 output (–)
12	VO1−	Channel 1 output (–)
13	VO1+	Channel 1 output (+)
14	VCCP1	Channels 1 and 2 power stage power supply
15	VCCS	Signal system power supply
16	VIN1+	Channel 1 input. Input operational amplifier + input.
17	VIN1−	Channel 1 input. Input operational amplifier – input.
18	VIN1	Channel 1 input. Input operational amplifier output.
19	VIN2+	Channel 2 input. Input operational amplifier + input.
20	VIN2−	Channel 2 input. Input operational amplifier – input.
21	VIN2	Channel 2 input. Input operational amplifier output.
22	VIN3–	Channel 3 input. Input operational amplifier – input.
23	VIN3	Channel 3 input. Input operational amplifier output.
24	VO_OP	Operational amplifier output
25	VIN-OP	Operational amplifier – input
26	VIN+OP	Operational amplifier + input
27	REG_IN	Regulator error amplifier output. Connect this pin to the base of the external pnp transistor.
28	REG_OUT	Regulator error amplifier input (+).
29	VREF_OUT	VREF amplifier (voltage follower) output.
30	VREF_IN	VREF input. Apply the external reference voltage to this pin.
31	VIN4	Channel 4 input. Input operational amplifier output.
32	VIN4−	Channel 4 input. Input operational amplifier – input.
33	MUTE234	Controls the on/off state of channels 2, 3, and 4.
34	MUTE1	Channel 1 output on/off control
35	VCONT	Loading block output high-level voltage setting
36	S_GND	Signal system ground

Pin Functions

Pin No.	Pin Name	Symbol	Description	Equivalent Circuit
16 17 18 19 20 21 22 23 32 31 26 25 24	Input (CH1 to 4)	VIN1+ VIN1− VIN1 VIN2+ VIN2− VIN2 VIN3− VIN3 VIN4− VIN4 VIN+OP VIN−OP VO_OP	Inputs (channels 1 to 4 and the independent operational amplifier)	
1 2	Input (H bridge)	FWD REV	Logic inputs The IC is set to one of four modes, forward, reverse, brake, and free running by the combination of high and low values applied to these pins.	
13 12 10 11 8 9 6 7	Output (BTL-AMP)	VO1+ VO1− VO2+ VO2− VO3+ VO3− VO4+ VO4−	Channel 1 to 4 outputs	
4 5 35	Output (H bridge)	VLO− VLO+ VCONT	H bridge (loading) output and loading output setting	
33 34	MUTE	MUTE234 MUTE1	BTL amplifier output on/off state setting. High: output on Low: output off	

Truth Table (Loading (H bridge) block)

FWD	REV	VLO+	VLO−	Loading output
L	L	OFF	OFF	OFF *1
	H	H	L	Forward
H	L	L	H	Reverse
	H	L	L	Short-circuit braking *2

*1. The output goes to the high-impedance state.

*2. In braking mode, the sink side transistor is turned on (for short-circuit braking).
The VLO+ and VLO− pins go to a level that is essentially the ground level.

Relationship between the MUTE pins and the power supply systems (VCCP*)