

2A, 200V, 3.500 Ohm, N-Channel Power MOSFET

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09289.

Ordering Information

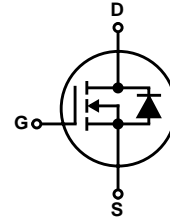
PART NUMBER	PACKAGE	BRAND
RFP2N20	TO-220AB	RFP2N20

NOTE: When ordering, include the entire part number.

Features

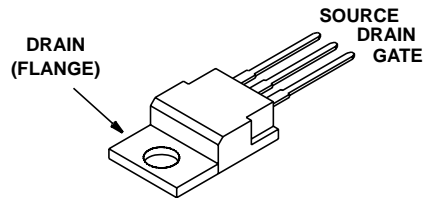
- 2A, 200V
- $r_{DS(ON)} = 3.500\Omega$

Symbol



Packaging

JEDEC TO-220AB



RFP2N20

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFP2N20	UNITS
Drain to Source Voltage (Note 1)	200	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	200	V
Continuous Drain Current	2	A
Pulsed Drain Current (Note 3)	5	A
Gate to Source Voltage	± 20	V
Maximum Power Dissipation	25	W
Linear Derating Factor	0.2	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	200	-	-	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$, (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $T_C = 125^\circ\text{C}$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 2\text{A}$, $V_{GS} = 10\text{V}$, (Figures 6, 7)	-	-	3.500	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 2\text{A}$, $V_{GS} = 10\text{V}$	-	-	7.0	V
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx 1\text{A}$, $V_{DD} = 100\text{V}$, $R_G = 50\Omega$ $V_{GS} = 10\text{V}$, $R_L = 96.5\Omega$ (Figure 10)	-	15	25	ns
Rise Time	t_r		-	20	30	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	25	40	ns
Fall Time	t_f		-	15	25	ns
Input Capacitance	C_{ISS}		$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$ $f = 1\text{MHz}$, (Figure 9)	-	-	200
Output Capacitance	C_{OSS}	-		-	60	pF
Reverse-Transfer Capacitance	C_{RSS}	-		-	25	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	-		-	5	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 1\text{A}$	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 2\text{A}$, $dI_{SD}/dt = 50\text{A}/\mu\text{s}$	-	200	-	ns

NOTES:

2. Pulsed test: width $\leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

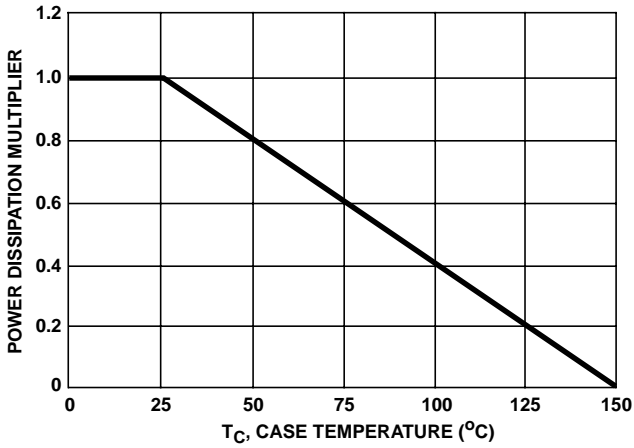


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

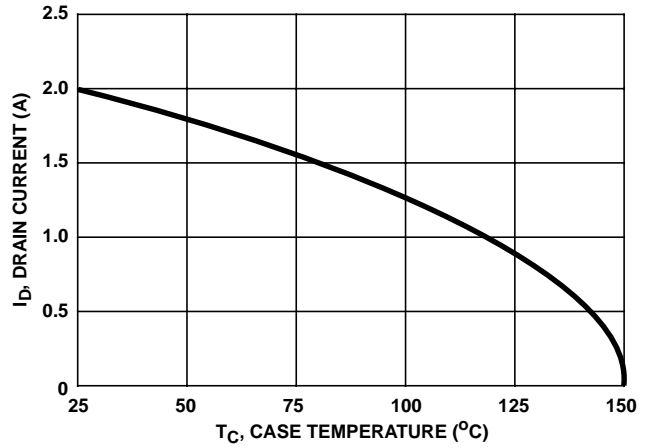


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

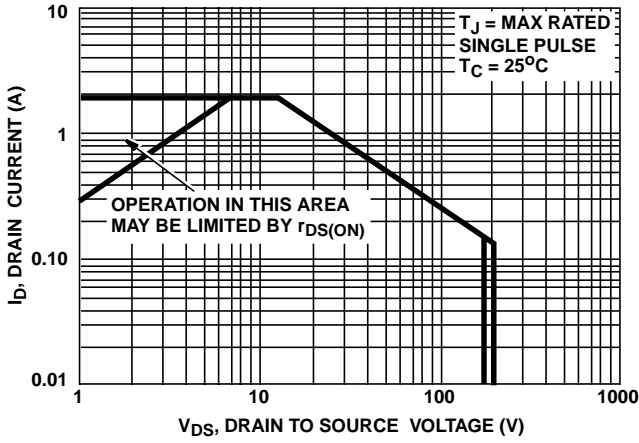


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

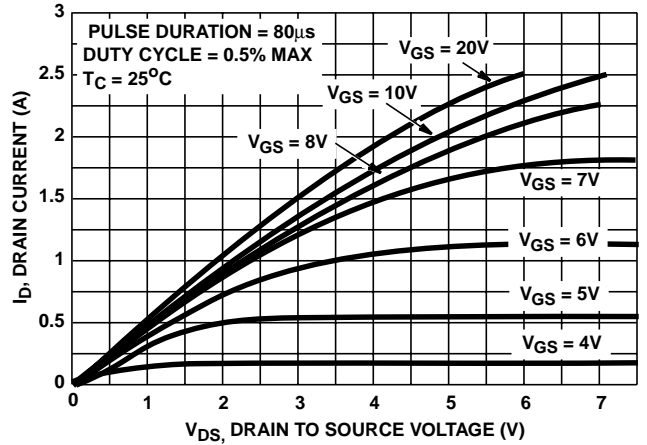


FIGURE 4. SATURATION CHARACTERISTICS

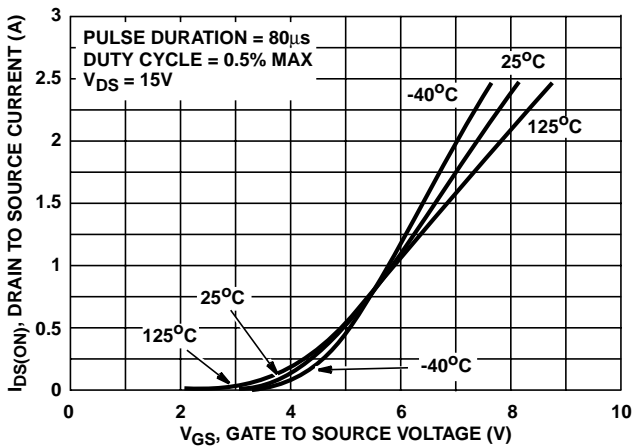


FIGURE 5. TRANSFER CHARACTERISTICS

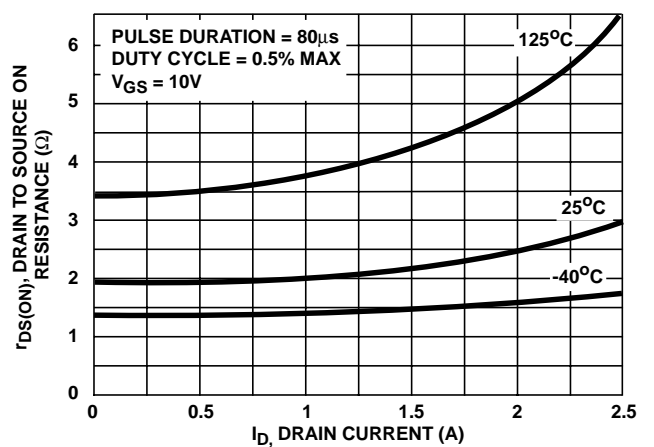


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

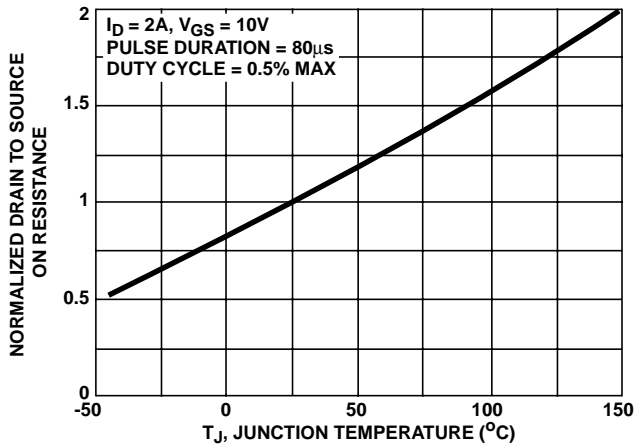


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

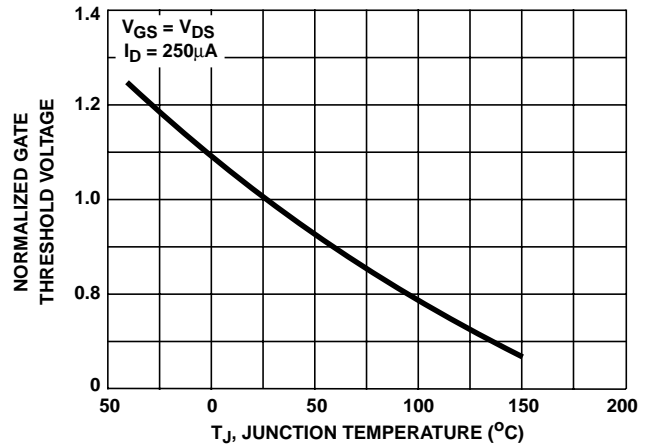


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

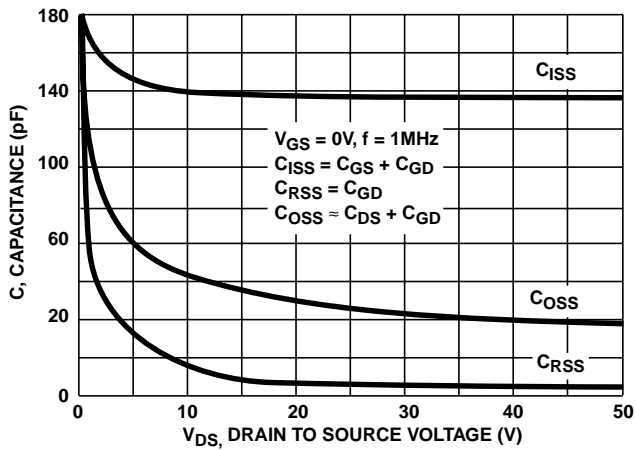
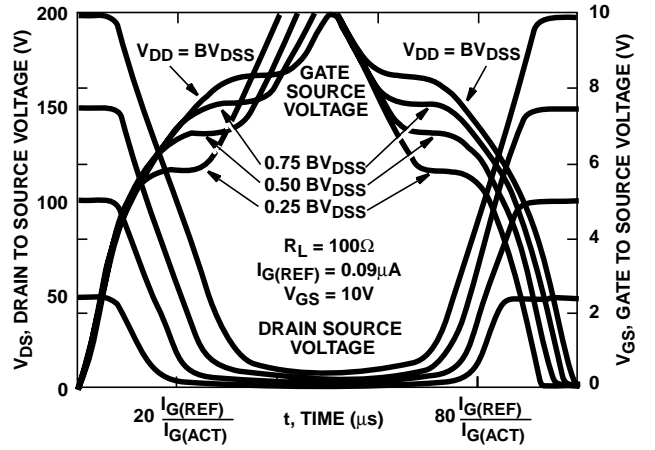


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Applications Notes AN7254 and AN7260

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

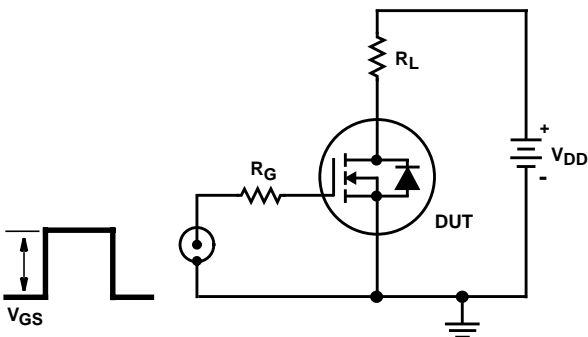


FIGURE 11. SWITCHING TIME TEST CIRCUIT

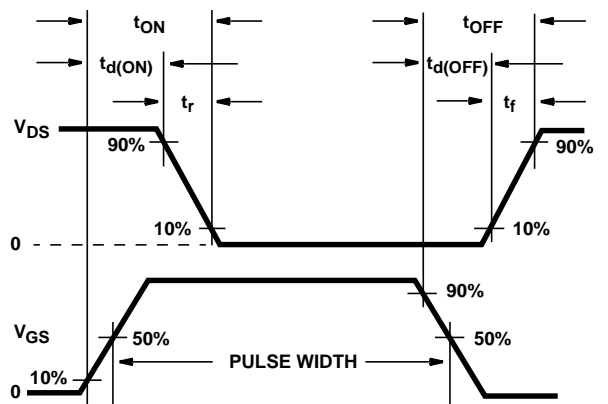


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms

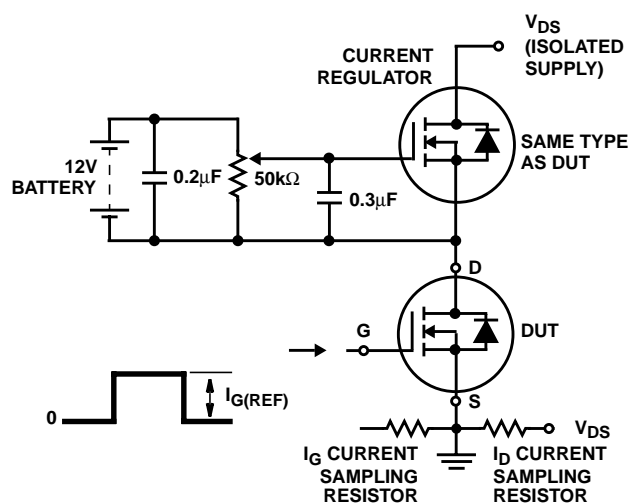


FIGURE 13. GATE CHARGE TEST CIRCUIT

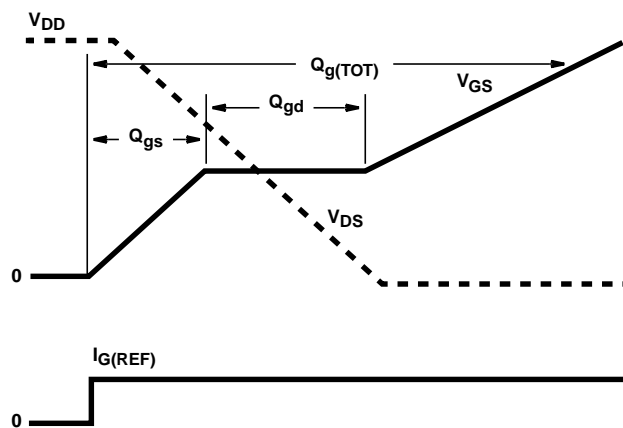


FIGURE 14. GATE CHARGE WAVEFORMS

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029