

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC7MH4040FK

## 12-Stage Ripple-Carry Binary Counter

The TC7MH4040 is an advanced high speed CMOS 12-STAGE BINARY COUNTER / DIVIDER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Setting CLR to high resets the counter to low.

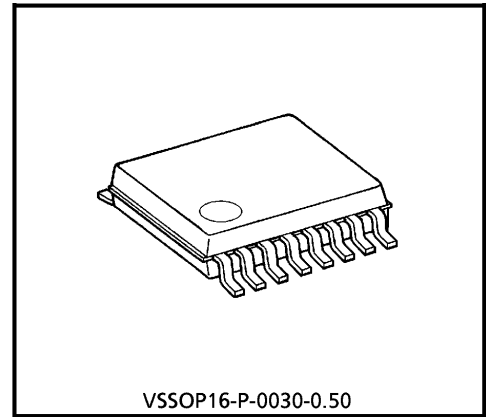
A negative transition on the  $\overline{CK}$  input brings one increment into the counter.

This counter provides all divided output stages, and at Q12, a 1/4096 divided frequency will be output.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

**Features:**

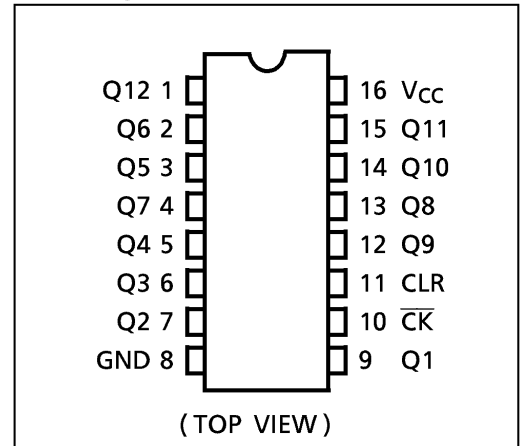
- High Speed.....  $f_{MAX} = 210\text{MHz (typ.)}$   
at  $V_{CC} = 5\text{V}$
- Low Power Dissipation.....  $I_{CC} = 4\mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity.....  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays...  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC} \text{ (opr)} = 2\text{V} \sim 5.5\text{V}$
- Low Noise .....  $V_{OLP} = 1.5\text{V (max)}$
- Pin and Function Compatible with 74HC4040



VSSOP16-P-0030-0.50

Weight: 0.02g (Typ.)

**Pin Assignment**



**Truth Table**

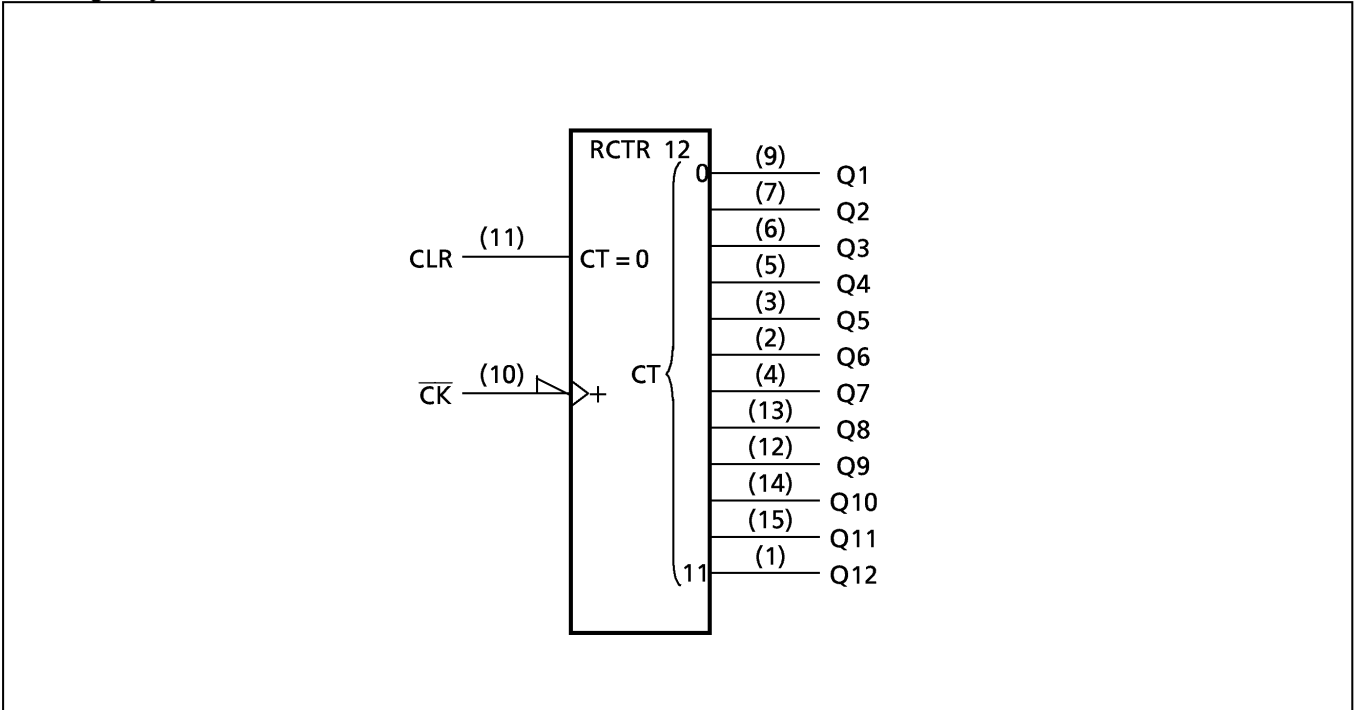
$\overline{CK}$	CLR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
	L	NO CHANGE
	L	ADOVANCE TO NEXT STATE

X: Don't Care

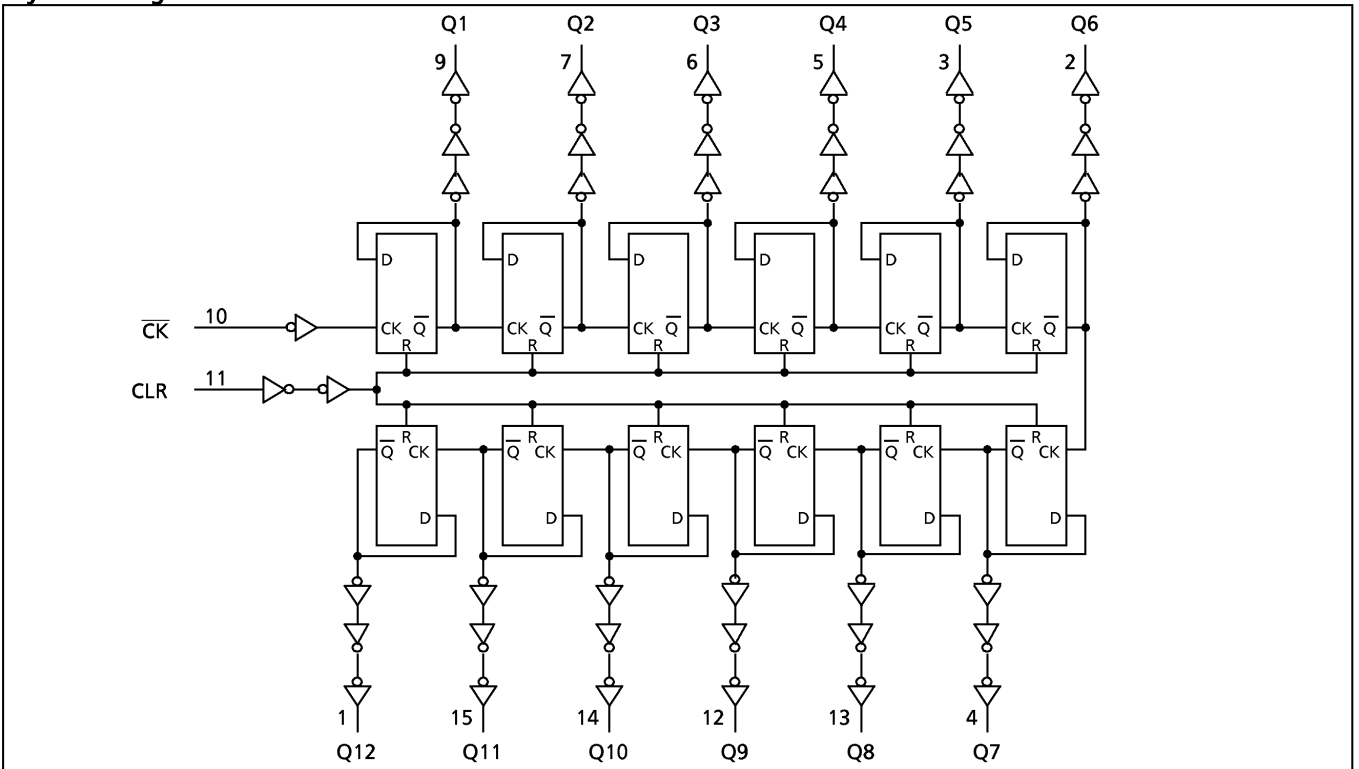
980910EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

IEC Logic Symbol



System Diagram



980910EBA2'

- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

## Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±100	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

## Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 ( $V_{CC} = 3.3 \pm 0.3V$ ) 0~20 ( $V_{CC} = 5 \pm 0.5V$ )	ns/V

## DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT	
				Min	Typ.	Max	Min	Max		
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V	
			3.0~ 5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—		
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V	
			3.0~ 5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$		
High - Level Output Voltage	$V_{OH}$	$V_{IN} =$ $V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
				3.0	2.58	—	—	2.48	—	
			$I_{OH} = -4\text{mA}$	4.5	3.94	—	—	3.80	—	
			$I_{OH} = -8\text{mA}$	4.5	—	—	—	—	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} =$ $V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
				3.0	—	—	0.36	—	0.44	
			$I_{OL} = 4\text{mA}$	4.5	—	—	0.36	—	0.44	
			$I_{OL} = 8\text{mA}$	4.5	—	—	0.36	—	0.44	
Input Leakage Current	$I_{IN}$	$V_{IN} = 5.5V$ or GND	0~5.5	—	—	±0.1	—	±1.0	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0		

Timing Requirements (Input  $t_r = t_f = 3ns$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C	UNIT
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum Pulse Width ( $\overline{CK}$ )	t <sub>W(L)</sub>		3.3 ± 0.3	—	5.0	5.0	ns
	t <sub>W(H)</sub>		5.0 ± 0.5	—	5.0	5.0	
Minimum Pulse Width (CLR)	t <sub>W(H)</sub>		3.3 ± 0.3	—	5.0	5.0	
			5.0 ± 0.5	—	5.0	5.0	
Minimum Removal Time	t <sub>rem</sub>		3.3 ± 0.3	—	5.0	5.0	
			5.0 ± 0.5	—	5.0	5.0	

AC Electrical Characteristics (Input  $t_r = t_f = 3ns$ )

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V <sub>CC</sub> (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation Delay Time ( $\overline{CK}$ -Q)	t <sub>pLH</sub> t <sub>pHL</sub>	3.3 ± 0.3	15	—	7.5	11.9	1.0	14.0	ns
			50	—	10.0	15.4	1.0	17.5	
		5.0 ± 0.5	15	—	4.8	7.3	1.0	8.5	
			50	—	6.3	9.3	1.0	10.5	
Propagation Delay Time (Qn-Qn+1)	Δt <sub>pd</sub>	3.3 ± 0.3	50	—	2.4	4.4	1.0	5.0	
		5.0 ± 0.5	50	—	1.6	3.1	1.0	3.5	
Propagation Delay Time (CLR-Q)	t <sub>pHL</sub>	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	
			50	—	10.8	16.3	1.0	18.5	
		5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0	
			50	—	7.1	10.6	1.0	12.0	
Maximum Clock Frequency	f <sub>MAX</sub>	3.3 ± 0.3	15	75	140	—	75	—	MHZ
			50	55	80	—	50	—	
		5.0 ± 0.5	15	150	210	—	125	—	
			50	95	125	—	80	—	
Input Capacitance	C <sub>IN</sub>			—	4	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 1)		—	21	—	—	—	

(Note 1): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

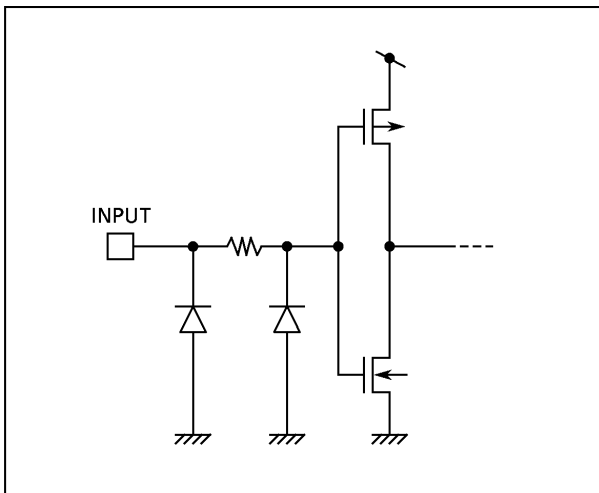
Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

**Noise Characteristics ( Input  $t_r = t_f = 3ns$  )**

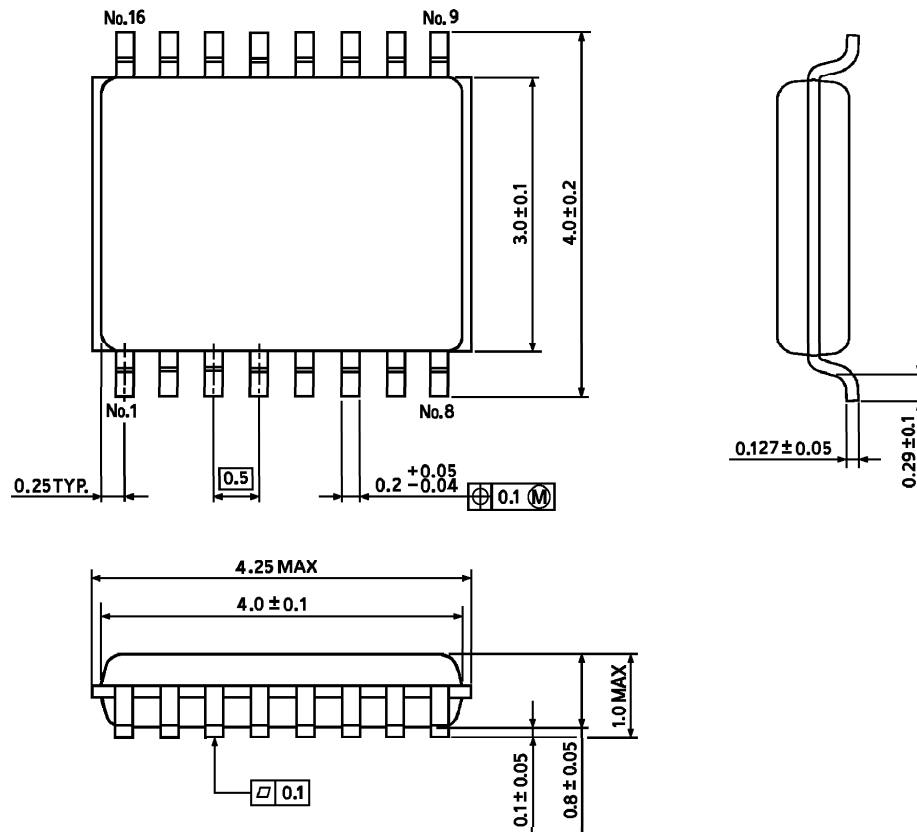
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT	
			V <sub>CC</sub> (V)	Typ.		Limit
Quiet Output Maximum Dynamic VOL	VOLP	CL = 50pF	5.0	1.2	1.5	V
Quiet Output Minimum Dynamic VOL	VOLV	CL = 50pF	5.0	- 1.2	- 1.5	V
Minimum High Level Dynamic Input Voltage	VIHD	CL = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	VILD	CL = 50pF	5.0	—	1.5	V

**Input Equivalent Circuit**



Outline Drawing  
VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02g (Typ.)