

HORIZONTAL COMBINATION

The TDA2594 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Horizontal oscillator based on the threshold switching principle.
- Phase comparison between sync pulse and oscillator voltage (φ_1).
- Internal key pulse for phase detector (φ_1) (additional noise limiting).
- Phase comparison between line flyback pulse and oscillator voltage (φ_2).
- Larger catching range obtained by coincidence detector (φ_3 ; between sync and key pulse).
- Switch for changing the filter characteristic and the gate circuit (VCR-operation).
- Sync separator.
- Noise separator.
- Vertical sync separator and output stage.
- Colour burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking.
- Phase shifter for the output pulse.
- Output pulse duration for transistor deflection systems.
- External switching off of the line trigger pulse.
- Output stage with separate supply voltage.
- Low supply voltage protection.
- Transmitter identification and muting circuit, and vertical sync switch-off.

QUICK REFERENCE DATA

Supply voltage	$V_{1-18} = V_S$	typ. 12 V
Supply current	I_1	typ. 30 mA
Input signals		
Sync separator input voltage (peak-to-peak value)	$V_{11-18(p-p)}$	typ. 3 V*
Noise separator input voltage (peak-to-peak value)	$V_{12-18(p-p)}$	typ. 3 V*
Pulse duration switch input voltage		
at $t = 14 \mu s + t_d$ (transistor driving)	V_{4-18}	0 to 3,5 V
at $t = 0$ ($V_{3-18} = 0$); input 4 open ($I_4 = 0$)	V_{4-18}	5,4 to 6,6 V
Output signals		
Vertical sync output pulse (peak-to-peak value)	$V_{8-18(p-p)}$	typ. 11 V
Burst key output pulse (peak-to-peak value)	$V_{7-18(p-p)}$	typ. 11 V
Line drive-pulse (peak-to-peak value)	$V_{3-18(p-p)}$	typ. 10 V

* Permissible range: 1 to 7 V.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

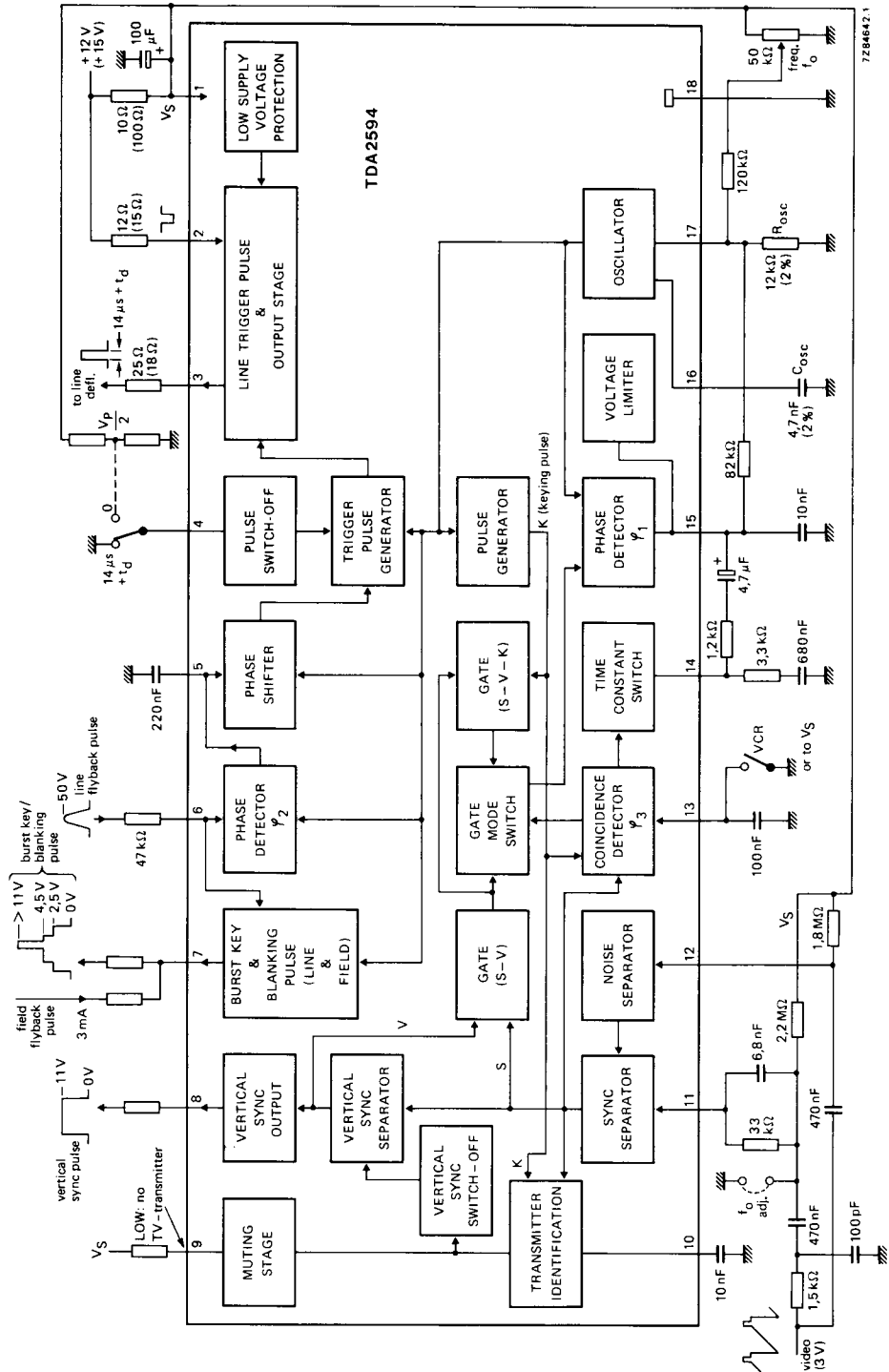


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage

at pin 1 (voltage source)

 $V_{1-18} = V_S$ max. 13,2 V

at pin 2

 V_{2-18} max. 18 V

Voltages

Pin 4

 V_{4-18} max. 13,2 V

Pin 9

 V_{9-18} max. 18 V $-V_{9-18}$ max. 0,5 V

Pin 11

 $\pm V_{11-18}$ max. 6 V

Pin 12

 $\pm V_{12-18}$ max. 6 V

Pin 13

 V_{13-18} max. 13,2 V

Currents

Pins 2 and 3 (transistor driving) (peak value)

 $I_{2M}, -I_{3M}$ max. 400 mA

Pin 4

 I_4 max. 1 mA

Pin 6

 $\pm I_6$ max. 10 mA

Pin 7

 $-I_7$ max. 5 mA

Pin 9

 I_9 max. 10 mA

Pin 13

 I_{13} max. 2 mA

Total power dissipation

 P_{tot} max. 800 mW

Storage temperature range

 T_{stg} -25 to +125 °C

Operating ambient temperature range

 T_{amb} 0 to +70 °C**CHARACTERISTICS** at $V_{1-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1**Sync separator (pin 11)**

Input switching voltage

 V_{11-18} typ. 0,8 V

Input keying current

 I_{11} 5 to 100 μ AInput leakage current at $V_{11-18} = -5$ V $I_{11} \leq 1$ μ A

Input switching current

 $I_{11} \leq 5$ μ A

Switch off current

 $I_{11} \geq 100$ μ Atyp. 150 μ A

Input signal (peak-to-peak value)

 $V_{11-18}(p-p)$ 3 to 4 V*

* Permissible range 1 to 7 V.

Noise separator (pin 12)

Input switching voltage	V_{12-18}	typ.	1,4 V
Input keying current	I_{12}		5 to 100 μA
Input switching current	I_{12}	\geq typ.	100 μA 150 μA
Input leakage current at $V_{12-18} = -5\text{ V}$	I_{12}	\leq	1 μA
Input signal (peak-to-peak value)	$V_{12-18(p-p)}$		3 to 4 V*
Permissible superimposed noise signal (peak-to-peak value)	$V_{12-18(p-p)}$	\leq	7 V

Line flyback pulse (pin 6)

Input current	I_6	\geq typ.	0,02 mA 1 mA
Input switching voltage	V_{6-18}	typ.	1,4 V
Input limiting voltage	V_{6-18}		-0,7 to +1,4 V

Switching on VCR (pin 13)

Input voltage	V_{13-18} or: V_{13-18}		0 to 2,5 V 9 to V_S V
Input current	$-I_{13}$ or: I_{13}	\leq \leq	200 μA 2 mA

Pulse switching off (pin 4)

For $t = 0$; input pin 4 open or $V_{3-18} = 0$

Input voltage	V_{4-18}		5,4 to 6,6 V
Input current	I_4	typ.	0 μA

Vertical sync pulse (positive-going) (pin 8)

Output voltage (peak-to-peak value)	$V_{8-18(p-p)}$	\geq typ.	10 V 11 V
Output resistance	R_8	typ.	2 k Ω
Delay between leading edge of input and output signal	t_{on}	typ.	15 μs
Delay between trailing edge of input and output signal	t_{off}	\geq	t_{on} μs
Switching off the vertical sync pulse	V_{10-18}	\leq	3 V

Burst key pulse (positive-going) (pin 7)

Output voltage	V_{7-18}	\geq typ.	10 V 11 V
Output resistance	R_7	typ.	70 Ω
Pulse duration; $V_{7-18} = 7\text{ V}$	t_p	typ.	4 μs 3,7 to 4,3 μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7-18} = 7\text{ V}$	t	typ.	2,65 μs 2,15 to 3,15 μs
Output trailing edge current	I_7	typ.	2 mA
Saturation voltage during line scan	V_{7-18}	\leq	1 V

* Permissible range 1 to 7 V.

Line flyback-blanking pulse (positive-going) (pin 7)

Output voltage	V ₇₋₁₈	4,1 to 4,9 V
Output resistance	R ₇	typ. 70 Ω
Output trailing edge current	I ₇	typ. 2 mA

Field flyback/blanking pulse (pin 7)

Output voltage with externally forced in current I ₇ = 2,4 to 3,6 mA	V ₇₋₁₈	2 to 3 V
Output resistance at I ₇ = 3 mA	R ₇	typ. 70 Ω

TV-transmitter identification output (pin 9; open collector)

Output voltage at I _g = 3 mA; no TV-transmitter	V ₉₋₁₈	≤ 0,5 V
Output resistance at I _g = 3 mA; no TV-transmitter	R ₉	≤ 100 Ω
Output current at V ₁₀₋₁₈ ≥ 3 V; TV-transmitter identified	I _g	≤ 5 μA

TV-transmitter identification (pin 10)

When receiving a TV signal the voltage V₁₀₋₁₈ will change from ≤ 1 V to ≥ 7 V.

Line drive pulse (positive-going)

Output voltage (peak-to-peak value)	V _{3-18(p-p)}	typ. 10 V
Output resistance		
for leading edge of line pulse	R ₃	typ. 2,5 Ω
for trailing edge of line pulse	R ₃	typ. 20 Ω
Pulse duration (transistor driving) V ₄₋₁₈ = 0 to 3,5 V; -I ₄ ≥ 200 μA; t _{fp} = 12 μs	t _p	14 + t _d μs*
Supply voltage for switching off the output pulse	V ₁₋₁₈	typ. 4 V

Overall phase relation

Phase relation between middle of sync pulse and the middle of the flyback pulse	Δt	typ. 2,6 ± 0,7 μs**
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The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ₂.

If additional adjustment is applied it can be arranged by current supply at pin 5, such that:

Supplying current	ΔI/Δt	typ. 30 μA/μs
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* t_d = switch-off delay of line output stage.

** Line flyback pulse duration t_{fp} = 12 μs.

Oscillator (pins 16 and 17)

Threshold voltage low level	V ₁₆₋₁₈	typ.	4,4 V
Threshold voltage high level	V ₁₆₋₁₈	typ.	7,6 V
Charging current	±I ₁₆	typ.	0,47 mA
Frequency; free running (C _{osc} = 4,7 nF; R _{osc} = 12 kΩ)	f _o	typ.	15,625 kHz
Spread of frequency	Δf _o	≤	± 5 % [▲]
Frequency control sensitivity	Δf _o /ΔI ₁₇	typ.	31 Hz/μA
Adjustment range of network in circuit (Fig. 1)	Δf _o	typ.	± 10 %
Influence of supply voltage on frequency; reference at V _S = 12 V	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	≤	± 0,05 % [▲]
Change of frequency when V _S drops to 5 V; reference at V _S = 12 V	Δf _o	≤	± 10 % [▲]
Temperature coefficient of oscillator frequency	TC	≤	± 10 ⁻⁴ K ⁻¹ [▲]

Phase comparison φ₁ (pin 15)

Control voltage range	V ₁₅₋₁₈	4,1 to 7,9 V	
Control current (peak value)	±I _{15M}	1,8 to 2,2 mA	
Output leakage current at V ₁₅₋₁₈ = 4,3 to 7,7 V	I ₁₅	≤	1 μA
Output resistance at V ₁₅₋₁₈ = 4,3 to 7,7 V	R ₁₃	high ohmic	*
at V ₁₅₋₁₈ ≤ 4,1 V or ≥ 7,9 V	R ₁₃	low ohmic	**
Control sensitivity		typ.	2 kHz/μs
Catching and holding range (82 kΩ between pins 15 and 17)	Δf	typ.	± 680 Hz
Spread of catching and holding range	Δ(Δf)	typ.	± 12 % [▲]

Phase comparison φ₂ and phase shifter (pin 5)

Control voltage range	V ₅₋₁₈	5,4 to 7,6 V	
Control current (peak value)	±I _{5M}	typ.	1 mA
Output resistance at V ₅₋₁₈ = 5,4 to 7,6 V	R ₅	high ohmic	*
Input leakage current at V ₅₋₁₈ = 5,4 to 7,6 V	I ₅	≤	5 μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t _{fp} = 12 μs)	t _d	≤	15,5 μs
Static control error	Δt/Δt _d	≤	0,2 %

Coincidence detector φ₃ (pin 13)

Output voltage	V ₁₃₋₁₈	0,5 to 6 V	
Output current (peak value) without coincidence	I _{13M}	typ.	0,1 mA
with coincidence	-I _{13M}	typ.	0,5 mA

* Current source.

** Emitter follower.

▲ Excluding external component tolerances.

Time constant switch (pin 14)

Output voltage	V_{14-18}	typ.	6 V
Output current (limited)	$\pm I_{14}$	typ.	1 mA
Output resistance			
at $V_{13-18} = 3,5$ to 7 V	R_{14}	typ.	0,1 k Ω
at $V_{13-18} \leq 2,5$ V or ≥ 9 V	R_{14}	typ.	60 k Ω

Internal keying pulse

Pulse duration	t_p	typ.	7,5 μ s
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