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HITACHI

Hitachi Displays, Ltd.

Date; Aug. 25, 2003

TECHNICAL DATA

TX26D01VM1CAA

CONTENTS

RECORD OF REVISION

Date	Old Sheet No. / New Sheet No.	Summary

APPLICATION

<26cm (10.4 inch) VGA>

This specification is applied to the following TFT Liquid Crystal Display Module with Back-light unit.

Note : Inverter device for Back-light is not built in and so it needs to be prepared on yourside.

・Type name	:	TX26D01VM1CAA
・Display Area	:	H211.2×V158.4 [mm]
・Display Dots	:	H(640×3)×V480 [dots]
(Display Pixels)		(H640×V480 pixels)
・Resolution	:	VGA
・Voltage of V_{DD}	:	3.3V
・Pixel Pitch	:	H0.330×V0.330 [mm]
・Color Pixel Arrangement	:	R・G・B Vertical Stripe
・Display Mode	:	Transmissive & Normally White Mode
・Color Number	:	262k Colors
・Dimensions Outlines	:	H243.0 TYP×V181.6 TYP×t12.5 MAX. [mm]
・Weight	:	(530)TYP. [g]
・Interface	:	CMOS
・Surface Polarizing Film	:	Anti-Glare Polarizing Film (Hard Coat 3H:Pencil Hardness)
・Back-light	:	Two Cold Cathode Fluorescent Lamp (Side-Light type:Both Long Side) Back-light inverter is not contained in Module.

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE		UNIT	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	-10	70	-20	70	℃	1)
Humidity	2)		2)		%RH	1)
Vibration	—	4.9 (0.5G)	—	19.6 (2G)	m/s^2	3)
Shock	—	29.4(3G)	—	490 (50G)	m/s^2	4)
Corrosive Gas	NOT ACCEPTABLE		NOT ACCEPTABLE		—	
Illuminance at LCD surface	—	50,000	—	50,000	lx	

Note 1) Environmental temperature and humidity of this unit, not of system installed with this unit.
At low temperature the brightness of CFL drop and the life time of CFL become to be short.
2) Ambient temp. Ta≦40℃ : 85%RH MAX. without condensation
Ta>40℃ : Absolute humidity must be lower than the saturated vapor of 85%RH at 40℃. without condensation
3) Vibration frequency : 20～50Hz.(Except resonance frequency)
4) 7ms of pulse width.

1.2 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

(1) TFT LIQUID CRYSTAL DISPLAY MODULE Vss=0V

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Power Supply Voltage	VDD	0	4.0	V	
Input signal Voltage for logic	VI	-0.2	VDD+0.2	V	1)
Electrostatic Durability	VESD0	±100		V	2), 3)
	VESD1	± 8		kV	2), 4)

Note 1) The specification shall be applied to pixel data signal and clock signal.
2) Discharge circuit to be connected : 200pF-250Ω,Environmental : 25℃-70%RH
3) The specification shall be applied to I/F connector pins.
4) The specification shall be applied to the surface of both a metal bezel and a LCD panel.

(2) BACK-LIGHT UNIT GND=0V

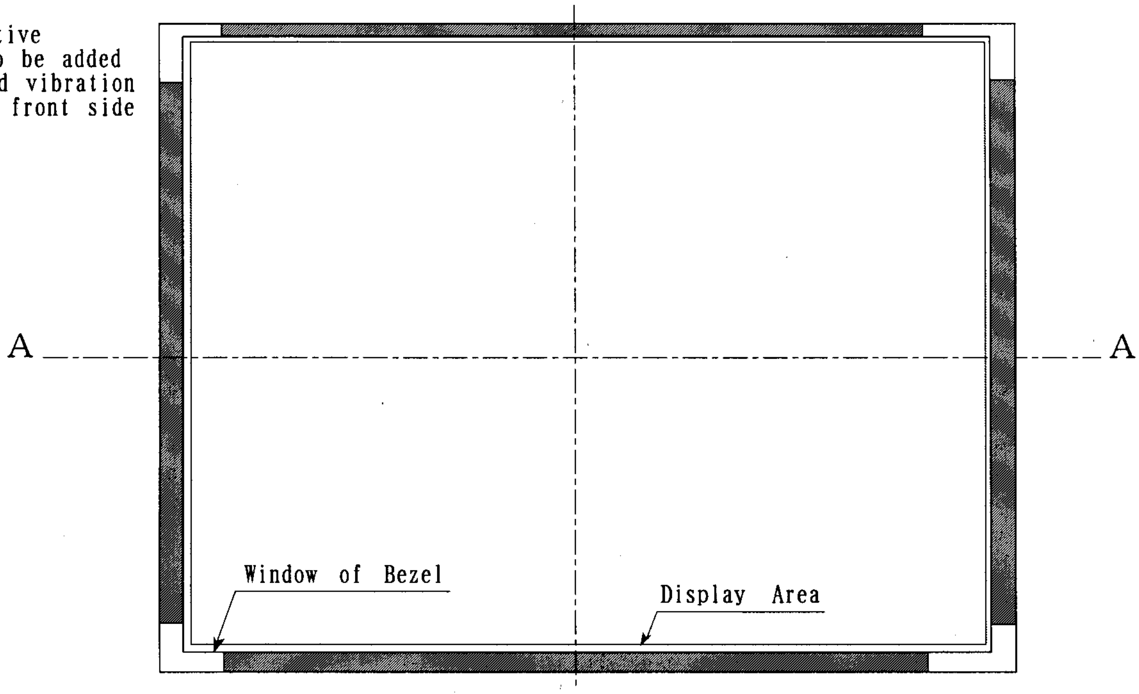
ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Lamp Current	IL	0	7.0	mArms	1)
Lamp Voltage	VL	0	1800	Vrms	2)

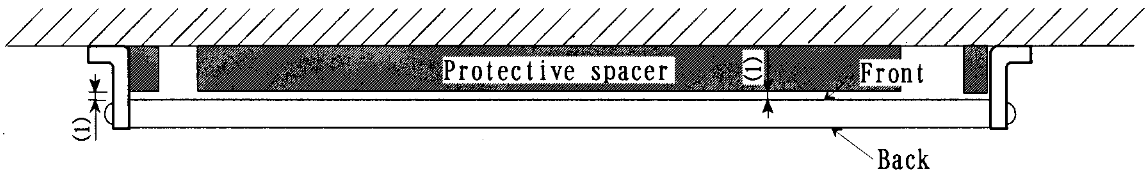
Note 1) At Lamp start-up time.
2) The specification is applicable to connector pins of Back-Light unit.

Adding protective spacer at shock & vibration test

Shaded area is to be supported with additional spacer.

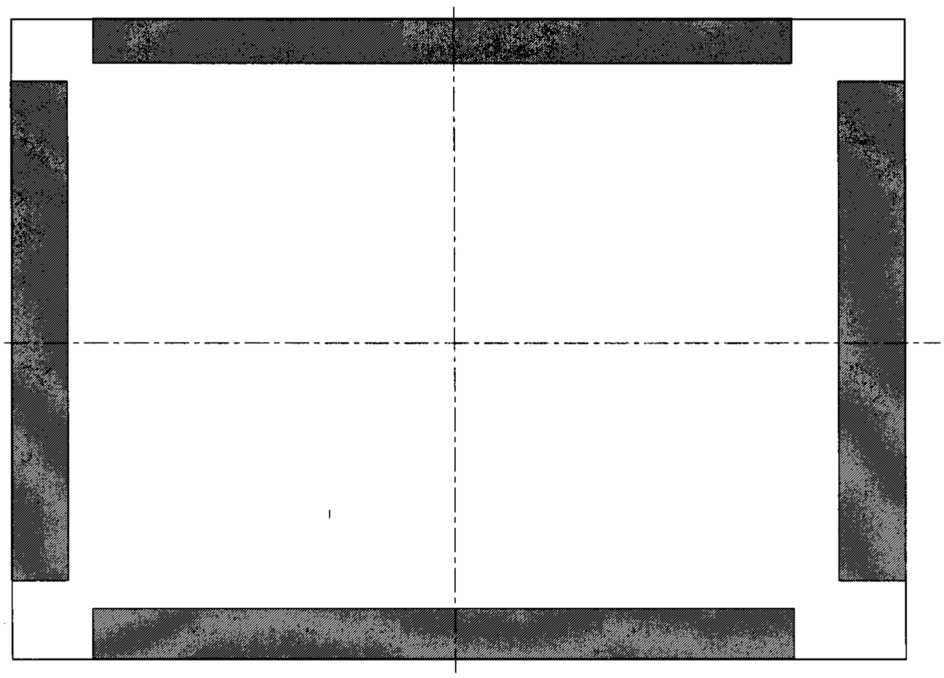
(1) This protective spacer is to be added at shock and vibration test on the front side

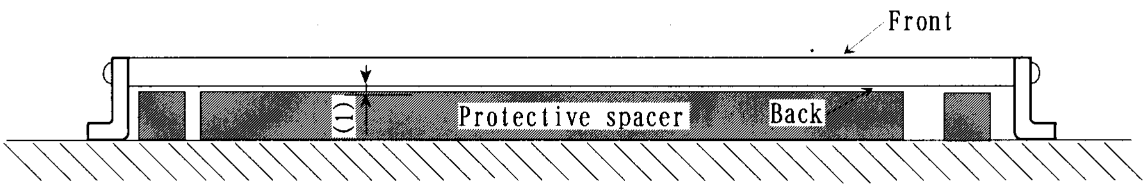




Shaded area is to be supported with additional spacer.

(2) This protective spacer is to be added shock and vibration test on the back side





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2. OPTICAL CHARACTERISTICS

The following items are measured on the conditions that this unit operation (TFT panel and Back-light) and measuring systems are stable. (more than 15minutes' operation)

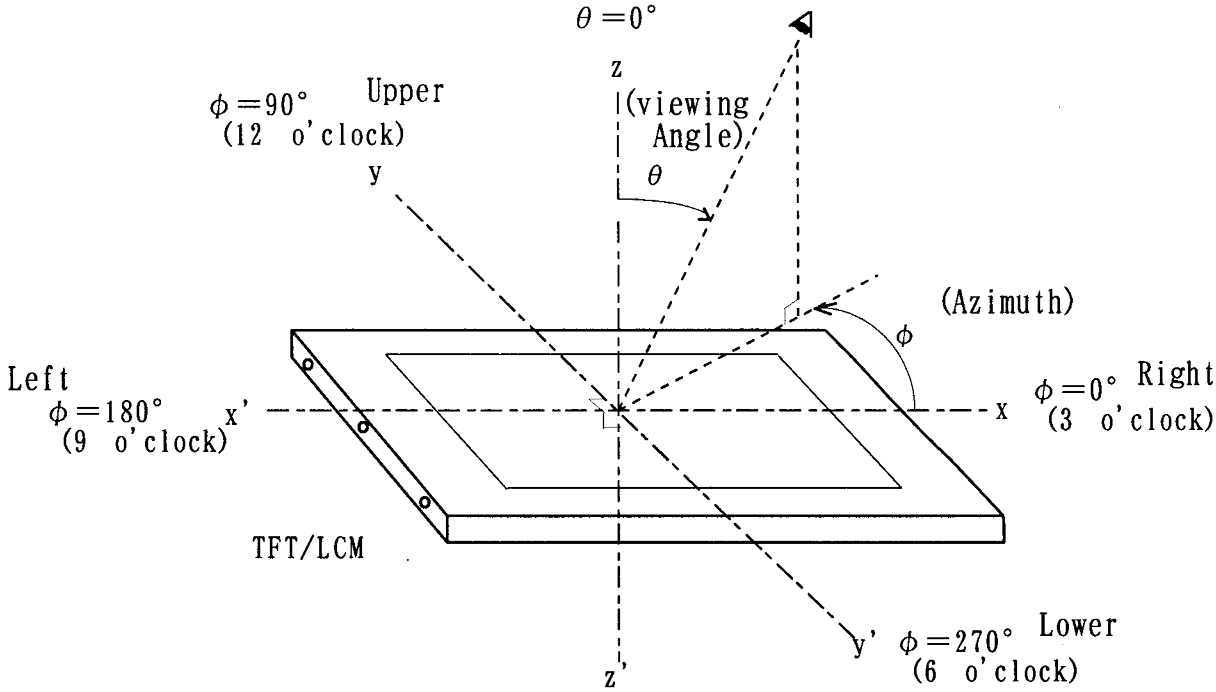
The ambient light excluding The Back-light unit is nothing.

- Measuring equipment : TOPCON BM-7, Prichard 1980A, or equivalent
- Measuring point : Active area center

Temperature of LCD=25℃, V_{DD}=3.3V, fv=60Hz, I_L=6.0mA,
Back-Light operation Frequency=50kHz

ITEM			SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Contrast Ratio			CR	$\theta=0°$ Note 1)	100	(300)	—	—	2)
Response Time	RISE		tr		—	30	—	ms	3)
	FALL		tf		—	20	—		
Brightness (White)			Bwh		—	(380)	—	cd/m²	
Brightness Uniformity			Buni		60	—	—	%	4)
Color of CIE	Red		x		—	0.58	—	—	
			y		—	0.35	—		
	Green		x		—	0.30	—		
			y		—	0.55	—		
	Blue		x		—	0.15	—		
			y		—	0.11	—		
	White		x		—	0.32	—		
			y		—	0.33	—		
Viewing Angle (CR≧5)	x-x		θx	ϕ=0°	—	65	—	deg	
			θx'	ϕ=180°	—	65	—		
	y-y		θy	ϕ=90°	—	45	—		
			θy'	ϕ=270°	—	60	—		

Note 1) Definition of Viewing Angle



Note 2) Definition of Contrast Ratio (CR)

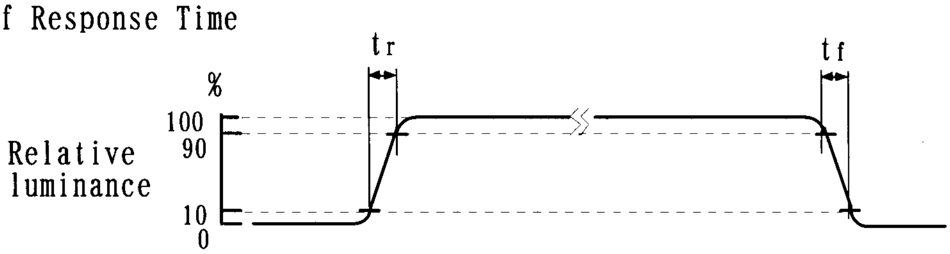
$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

These Brightness is measured on the center of screen.

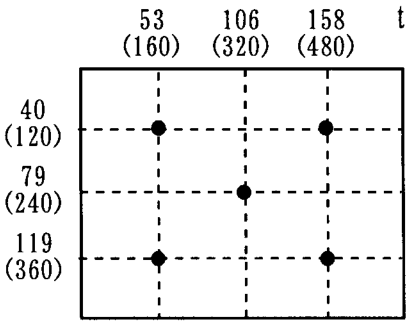
* Measurement in the darkroom.

Note 3) Definition of Response Time

Optical Response



Note 4) Definition of Brightness Uniformity



● : measuring point

The brightness uniformity (Buni) is defined as the following equation.

$$Buni = \frac{Bmin}{Bmax} \times 100$$

where, Bmax = Maximum brightness among 5 measuring points
Bmin = Minimum brightness among 5 measuring points

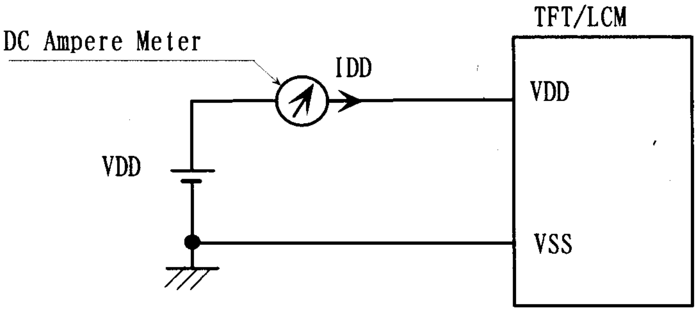
3. ELECTRICAL CHARACTERISTICS

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

Ta=25℃, Vss=0V

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	
Input Voltage for Logic Signal	Hi	V_{IH}	2.0	—	VDD	mV	1)
	Lo	V_{IL}	VSS	—	0.8		
Power Supply Current		I_{DD}	—	250	400	mA	2), 3)
Vsync Frequency		f_V	—	60	70	Hz	
Hsync Frequency		f_H	—	31.6	38	kHz	
DCLK Frequency		f_{CLK}	—	25	29	MHz	

Note 1) The specification is applicable to Display Data Signal pin, Timing Signal pin.
2) f_V=60Hz, f_{CLK}=25MHz, V_{DD}=3.3V, DC Current is measured with the method as below.



Typical value is measured when displaying Black Pattern.
Maximum is measured when displaying Vertical-stripe(Black-7 Gray scale)
3) 0.63A fuse is built in the unit. Current capacity for VDD power supply should be larger than 2A, so that the fuse built in the unit(Maximum) could appropriately work in the abnormal.

(2) BACK-LIGHT UNIT

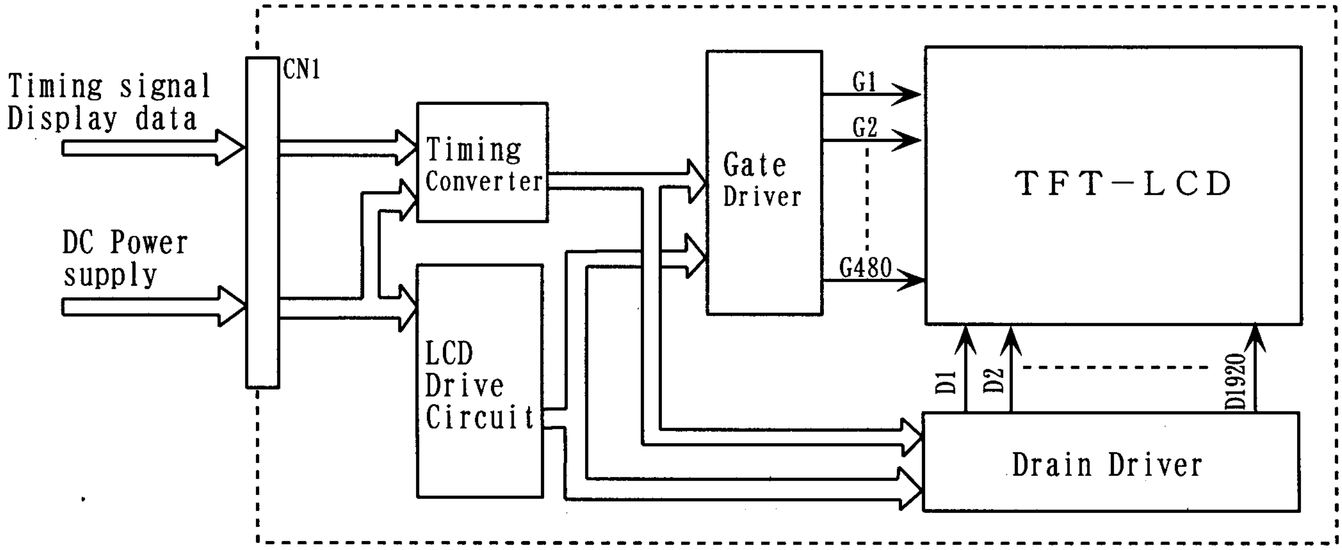
Ta=25℃, GND=0V

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT	NOTE
Lamp Current	I_L		(4.0)	(6.0)	6.5	mArms	1), 3)
Lamp Voltage	V_L		—	(450)	—	Vrms	
Frequency	f_L		50	—	70	kHz	2)
Starting Lamp Voltage	Vs	Ta=25℃	(1200)	—	—	Vrms	
		Ta=10℃	(1450)	—	—		

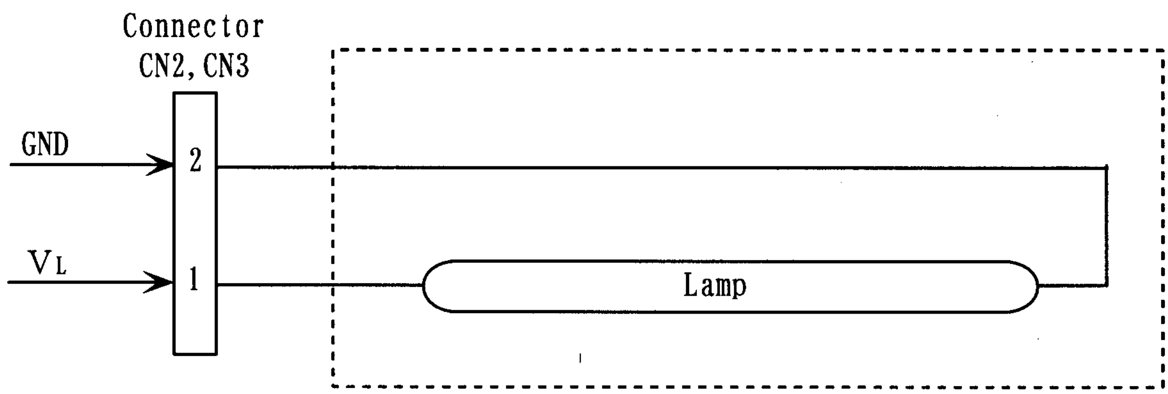
NOTE 1) Higher IL cause the short life time of CFL.
2) Lamp operation frequency may produce interference with Hsync frequency, which causes rolling or flickering screen. Therefore lamp operation frequency shall be as different as possible from Hsync frequency, to avoid interference.
3) When IL is measured, an ammeter is attached to the ground line.

4. BLOCK DIAGRAM

(1) TFT-LIQUID CRYSTAL DISPLAY MODULE



(2) BACK-LIGHT UNIT



Color of wires CFL to CN2, CN3

1	(VL)	: Pink
2	(GND)	: White

5. INTERFACE PIN CONNECTION

(1) TFT-LIQUID CRYSTAL DISPLAY MODULE

CN1 《HIROSE:DF9B-31P-1V》

Pin No.	SYMBOL	FUNCTION	NOTE
1	VSS		2)
2	DCLK	Clock Signal	
3	NC		4)
4	NC		4)
5	VSS		2)
6	R0	Red Data Signal (LSB)	
7	R1	Red Data Signal	
8	R2	Red Data Signal	
9	R3	Red Data Signal	
10	R4	Red Data Signal	
11	R5	Red Data Signal (MSB)	
12	VSS		2)
13	G0	Green Data Signal (LSB)	
14	G1	Green Data Signal	
15	G2	Green Data Signal	
16	G3	Green Data Signal	
17	G4	Green Data Signal	
18	G5	Green Data Signal (MSB)	
19	VSS		2)
20	B0	Blue Data Signal (LSB)	
21	B1	Blue Data Signal	
22	B2	Blue Data Signal	
23	B3	Blue Data Signal	
24	B4	Blue Data Signal	
25	B5	Blue Data Signal (MSB)	
26	VSS		2)
27	DTMG	Display Timing Signal	
28	VDD	Power Supply 3.3V (typical)	1)
29	VDD	Power Supply 3.3V (typical)	1)
30	TEST	TEST Pin	3)
31	NC		4)

Notes 1) All VDD pins shall be connected to +3.3V(Typ.).
2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.
3) Keep open. Hitachi test use only.
4) Unconnected to the module

(2) BACK-LIGHT UNIT

CN2, CN3 《JST:BHR-02(8.0)VS-1》

Pin No.	SYMBOL	FUNCTION	NOTE
1	VL	Power Supply	
2	GND	GND (0V)	

RELATIONSHIP BETWEEN DISPLAYED COLOR AND INPUT DATA

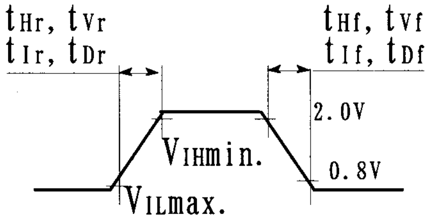
COLOR \ INPUT DATA		R DATA						G DATA						B DATA					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	YELLO	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	RED(2)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	GREEN(61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	GREEN(2)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

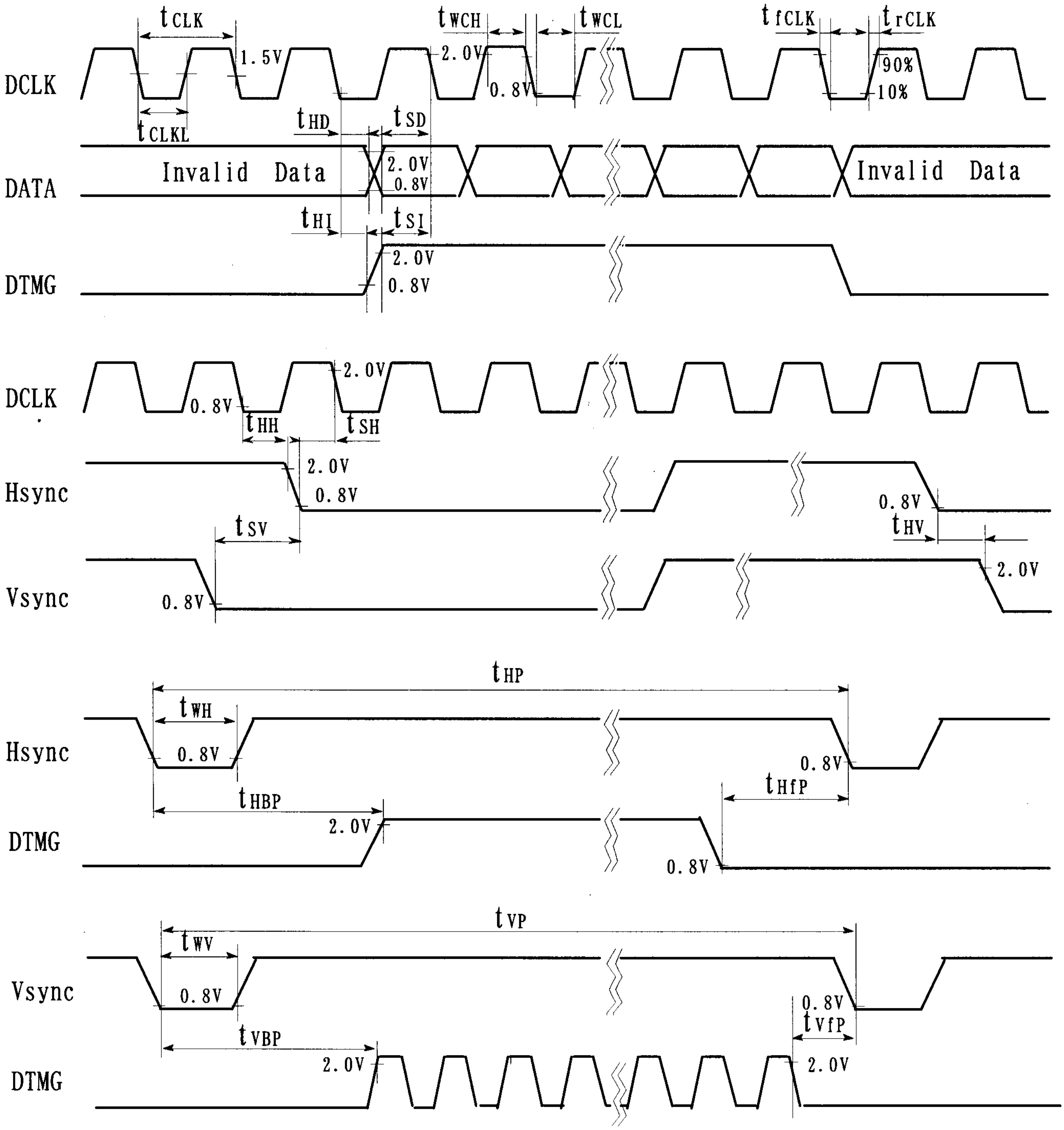
Note 1) Definition of gray scale :
Color(n) --- number in parenthesis indicates gray scale level.
Larger number corresponds to darker level.
2) Data : 1:High, 0:Low

6. INTERFACE TIMING

(1) TIMING CHART

Hsync, Vsync, DTMG, DATA
G0～5 R0～5 B0～5



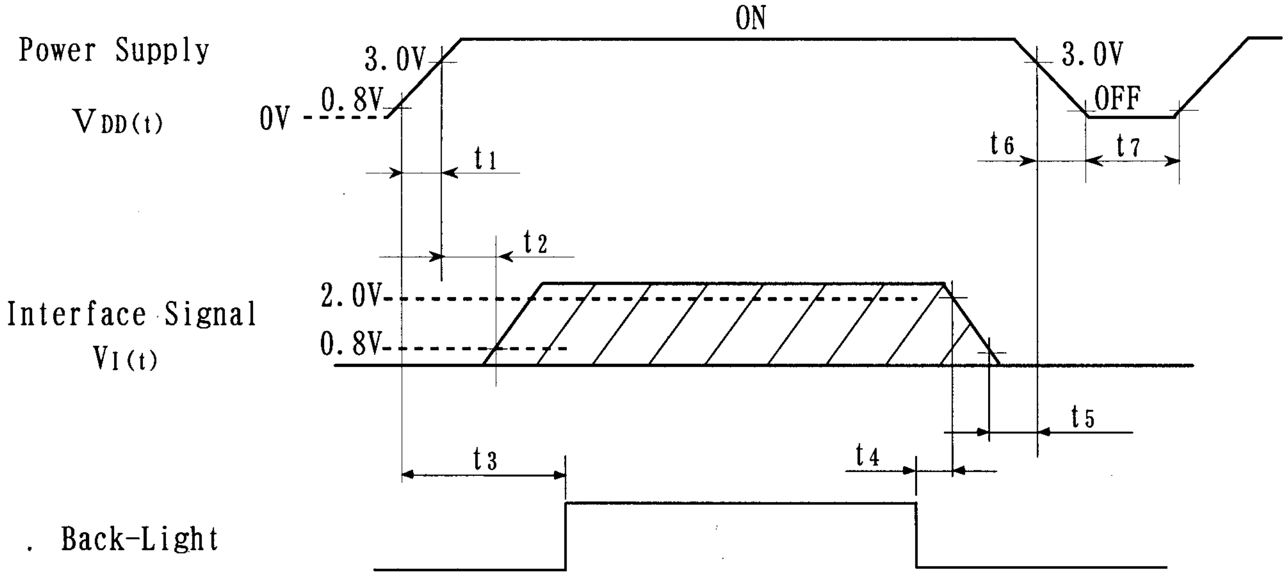


* The DTMG signal for this module is defined as above-mentioned timings for Vsync and Hsync.
This module synchronizes with only DTMG and don't require inputting Vsync and Hsync signals.
During Blanking period, DTMG should be "Low" level.

(2) INTERFACE TIMING SPECIFICATIONS

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Period	t_{CLK}	34.5	40	43	ns	
	Width-Low	t_{WCL}	12	—	—		
	Width-Hi	t_{WCH}	12	—	—		
	Rise Time	t_{rCLK}	—	—	25		
	Fall Time	t_{fCLK}	—	—	25		
	Duty	D	0.45	0.5	0.55	—	$D = t_{CLKL} / t_{CLK}$
Hsync	Set up Time	t_{SH}	5	—	—	ns	for DCLK
	Hold Time	t_{HH}	10	—	—		
	Period	t_{HP}	760	800	850	t_{CLK}	
	Width-Active	t_{WH}	5	96	—		
	Rise/Fall Time	t_{Hr}, t_{Hf}	—	—	30	ns	
Vsync	Set up Time	t_{SV}	0	—	—	t_{CLK}	for Hsync
	Hold Time	t_{HV}	2	—	—		
	Period	t_{VP}	515	525	609	t_{HP}	
	Width-Active	t_{WV}	3	—	—		
	Rise/Fall Time	t_{Vr}, t_{Vf}	—	—	50	ns	
DTMG	Set up Time	t_{SI}	5	—	—	ns	for DCLK
	Hold Time	t_{HI}	10	—	—		
	Rise/Fall Time	t_{Ir}, t_{If}	—	—	30	ns	
	Horizontal Back porch	t_{HBP}	7	144	—	t_{CLK}	
	Horizontal Front porch	t_{HFP}	—	16	—		
	Vertical Back porch	t_{VBP}	4	35	—	t_{HP}	
	Vertical Front porch	t_{VFP}	—	10	—		
DATA	Set up Time	t_{SD}	5	—	—	ns	for DCLK
	Hold Time	t_{HD}	10	—	—		
	Rise/Fall Time	t_{Dr}, t_{Df}	—	—	25	ns	

(3) TIMING BETWEEN INTERFACE SIGNAL AND POWER SUPPLY



POWER ON

t1 ≦ 15ms
0ms < t2 ≦ 45ms
0.1s ≦ t3

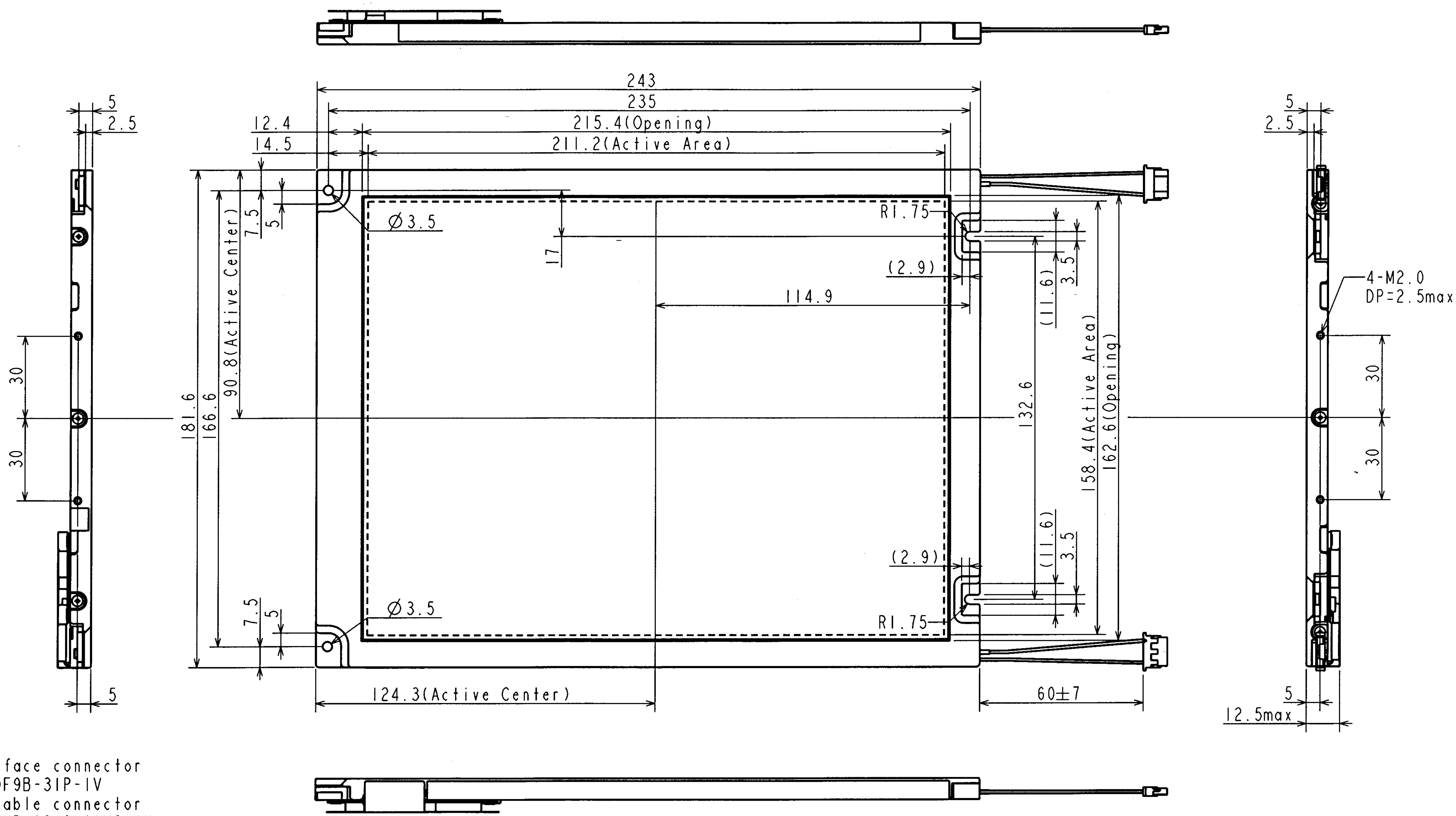
POWER OFF

5ms ≦ t4
0ms ≦ t5 ≦ 45ms
0ms ≦ t6 ≦ 20ms
0.4s ≦ t7

Note 1) Set 0V ≦ VI(t) ≦ VDD(t).
Here, VI(t), VDD(t) indicate the transitive state of VI, VDD when power supply is turned ON or OFF.

Note 2) Do not keep interface signal high-impedance when power on.

7. DIMENSIONAL OUTLINE
Front-Side



NOTE1) Interface connector
HRS:DF9B-31P-1V
2) CFL cable connector
JST:BHR-02(8.0)VS-1N
3) The unspecified tolerance : ±0.5mm
4) Holes for mounting LCD MODULE
top mounting : 4 holes
side mounting : 4 holes
5) Maximum torque of the screws for mounting LCD MODULE
0.196[N·m](2.0[kgf·cm])
6) The screws mounted in the side of LCD MODULE : 6 points

UNIT:mm

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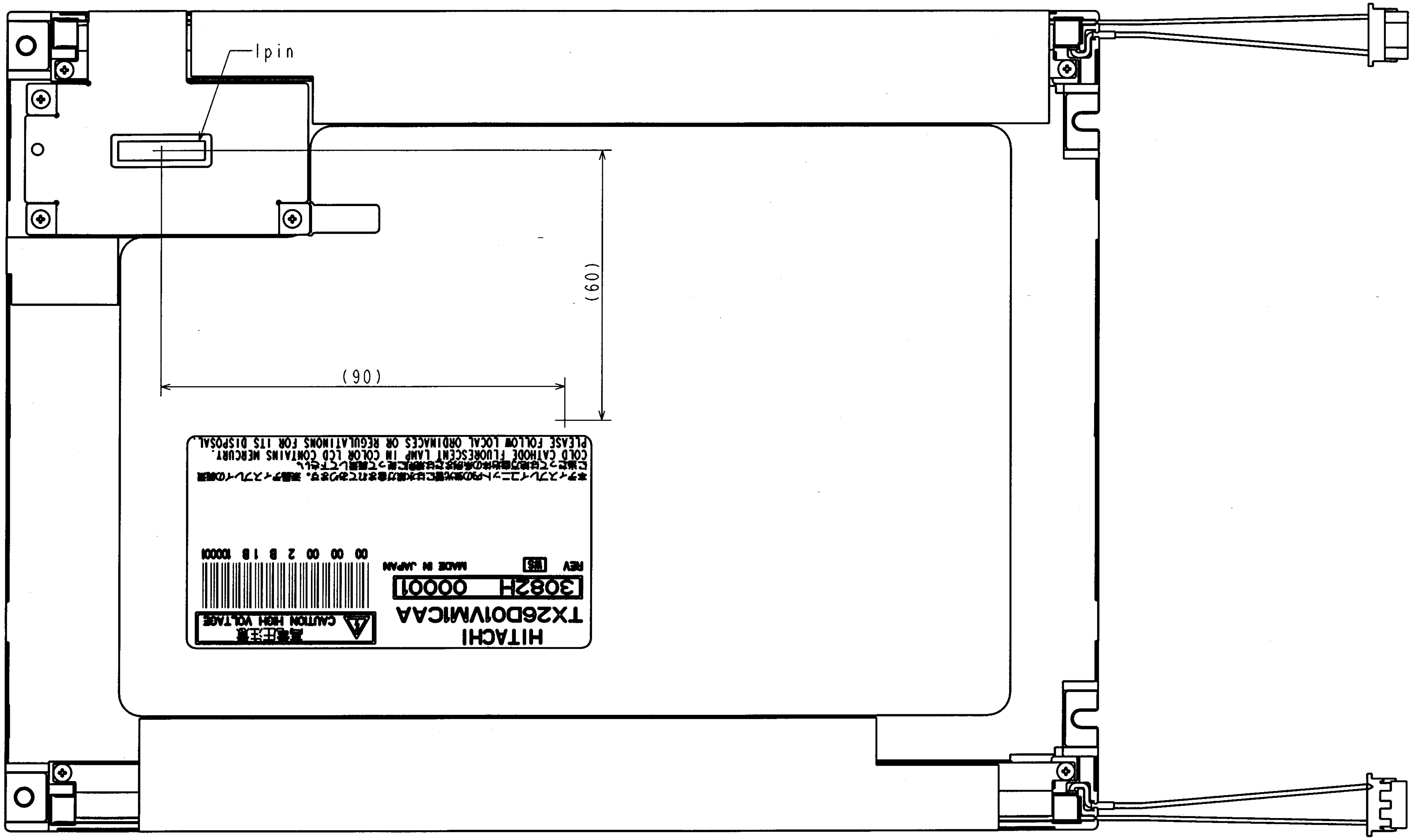
Back-Side



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