IXYS

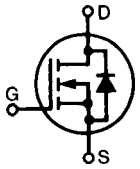
High Voltage Power MOSFETs

IXTA/IXTP 3N120
IXTA/IXTP 3N110

V_{DSS}	I_{D25}	$R_{DS(on)}$
1200 V	3 A	4.5 Ω
1100 V	3 A	4.0 Ω

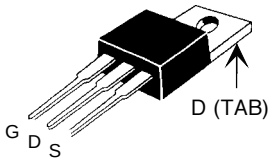
N-Channel Enhancement Mode
Avalanche Rated, High dv/dt

Preliminary Data Sheet

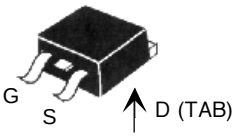


Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	3N120	1200	V
		3N110	1100	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	3N120	1200	V
		3N110	1100	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C		3	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}		12	A
I_{AR}	T_C = 25°C		3	A
E_{AR}	T_C = 25°C		20	mJ
E_{AS}			700	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		150	W
T_J			-55 to +150	°C
T_{JM}			150	°C
T_{stg}			-55 to +150	°C
T_L	1.6 mm (0.063 in) from case for 10 s		300	°C
M_d	Mounting torque (TO-220)		1.13/10	Nm/lb.in.
Weight	TO-220		4	g
	TO-263		2	g

TO-220 (IXTP)



TO-263 (IXTA)



G = Gate D = Drain
S = Source TAB = Drain

Features

- International standard packages
- Low $R_{DS\ (on)}$
- Rated for unclamped Inductive load Switching (UIS)
- Molding epoxies meet UL 94 V-0 flammability classification

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 1 mA	3N120	1200			V
		3N110	1100			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA		2.5		4.5	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	V_{DS} = 0.8 V_{DSS}	T_J = 25°C			25	µA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 0.5 I_{D25}	3N120			4.5	Ω
	Note 1	3N110			4.0	Ω

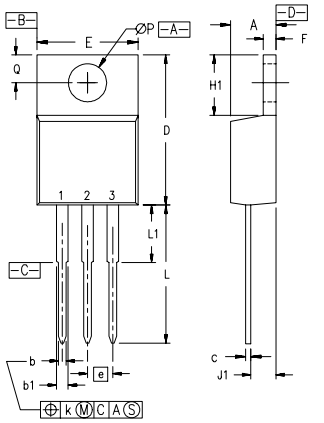
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 • I_{D25}, Note 1	1.5	2.2		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1050	1300	pF
C_{oss}			100	125	pF
C_{rss}			25	50	pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25} R_G = 4.7 Ω (External),		17		ns
t_r			15		ns
$t_{d(off)}$			32		ns
t_f			18		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		39		nC
Q_{gs}			9		nC
Q_{gd}			22		nC
R_{thJC}				0.8	K/W
R_{thCK}	(TO-220)		0.25		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V			3	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			12	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = I_S, -di/dt = 100 A/µs, V_R = 100 V		700		ns

Notes: 1. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %

TO-220 (IXTP) Outline

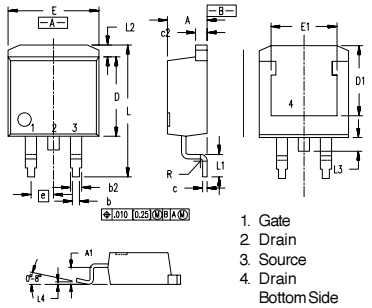


Pins: 1 - Gate 2 - Drain
3 - Source 4 - Drain
Bottom Side

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-220 AB.

TO-263 (IXTA) Outline



1. Gate
2. Drain
3. Source
4. Drain
Bottom Side

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.06	4.83	.160	.190
A1	2.03	2.79	.080	.110
b	0.51	0.99	.020	.039
b2	1.14	1.40	.045	.055
c	0.46	0.74	.018	.029
c2	1.14	1.40	.045	.055
D	8.64	9.65	.340	.380
D1	7.11	8.13	.280	.320
E	9.65	10.29	.380	.405
E1	6.86	8.13	.270	.320
e	2.54	BSC	.100	BSC
L	14.61	15.88	.575	.625
L1	2.29	2.79	.090	.110
L2	1.02	1.40	.040	.055
L3	1.27	1.78	.050	.070
L4	0	0.38	0	.015
R	0.46	0.74	.018	.029

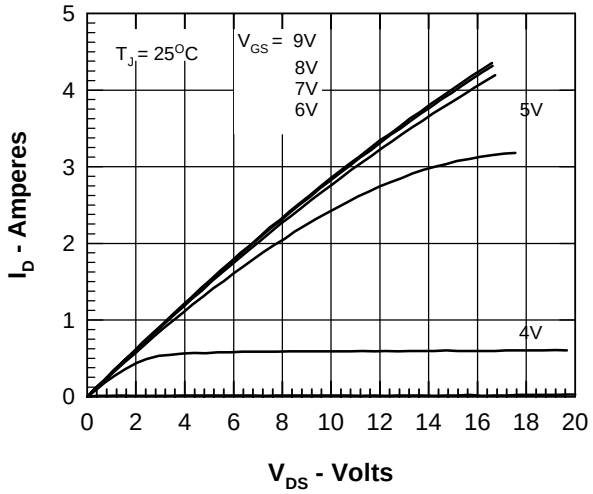


Fig.1 Output Characteristics @ T_j = 25°C

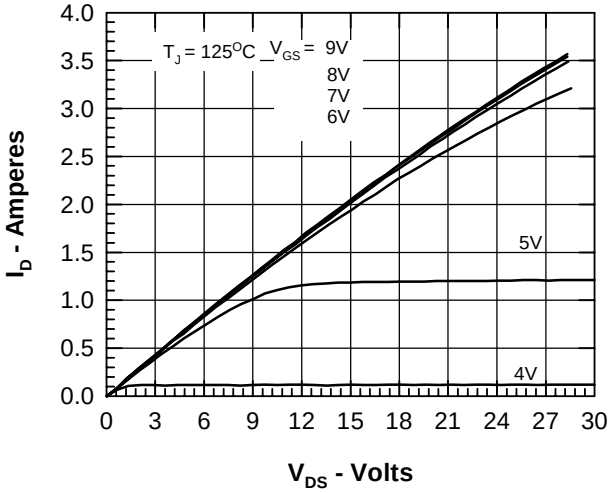


Fig. 2 Output Characteristics @ T_j = 125°C

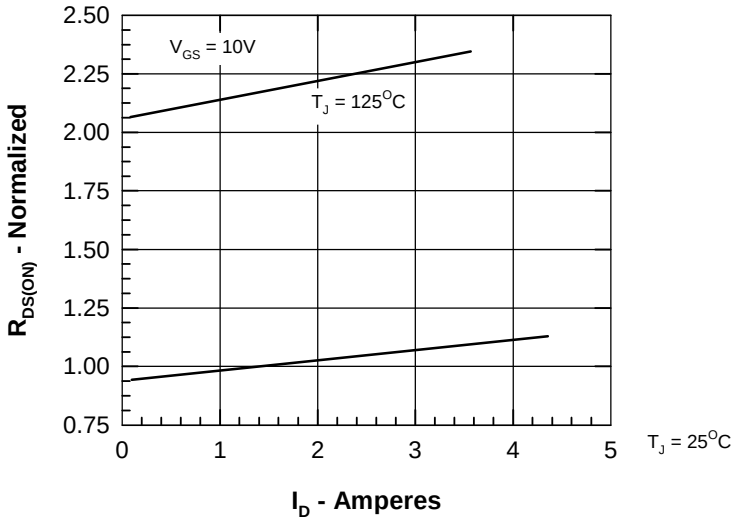


Fig. 3 $R_{DS(on)}$ vs. Drain Current

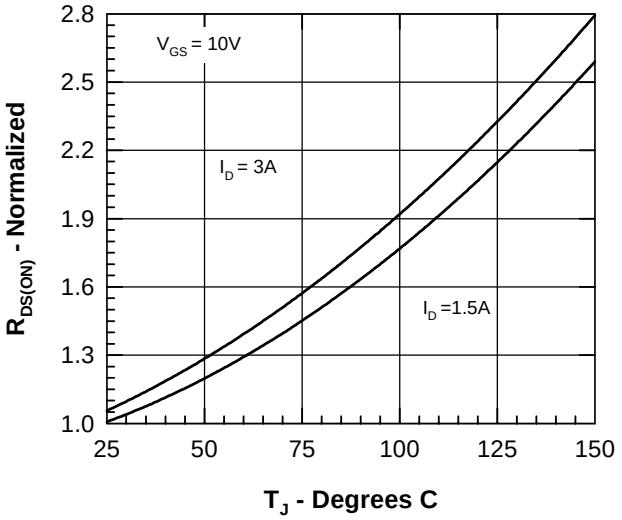


Fig. 4 Temperature Dependence of Drain to Source Resistance

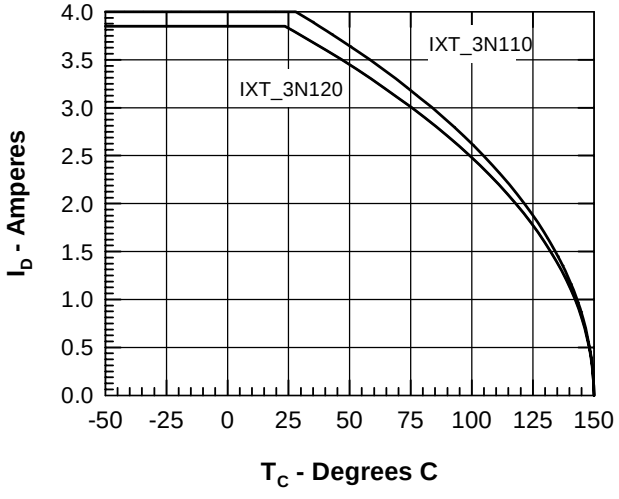


Fig. 5 Drain Current vs. Case Temperature

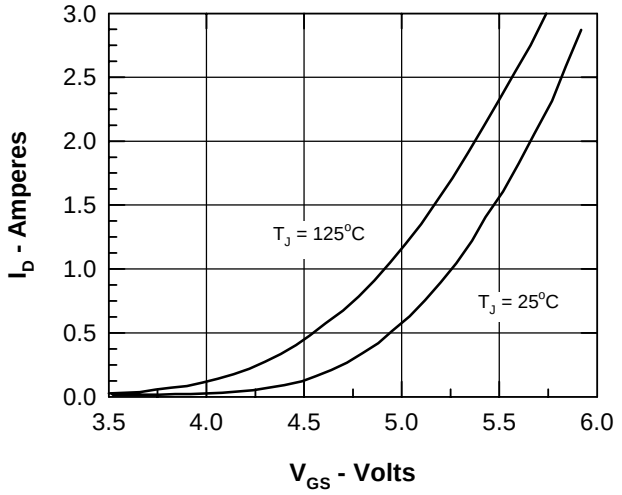


Fig. 6 Drain Current vs Gate Source Voltage

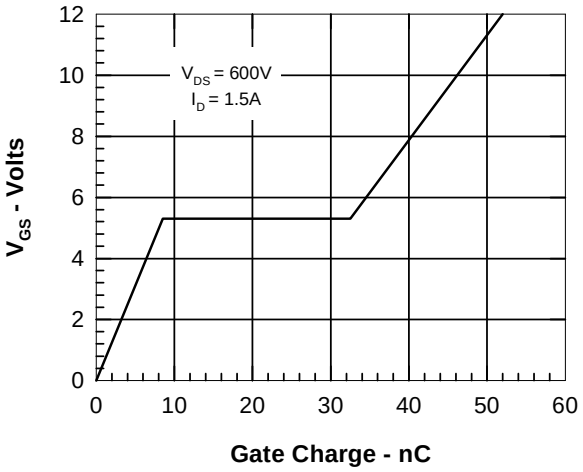


Fig. 7 Gate Charge Characteristic Curve

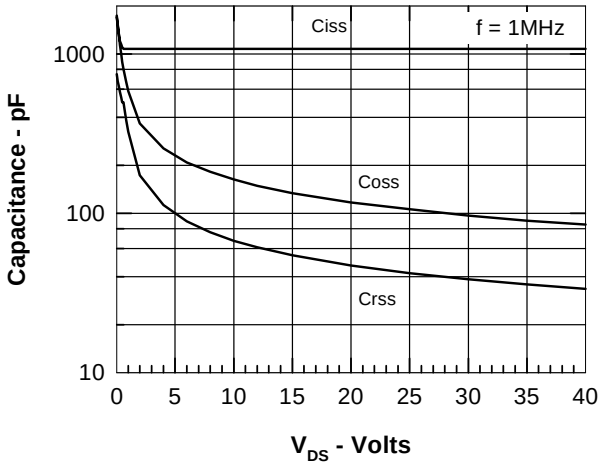


Fig. 8 Capacitance Curves

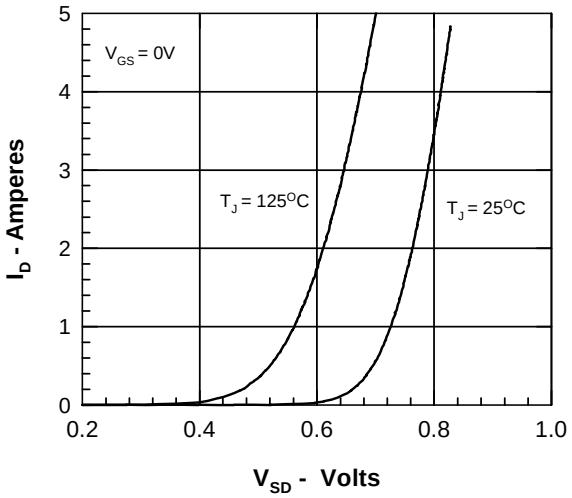


Fig. 9 Drain Current vs Drain to Source Voltage

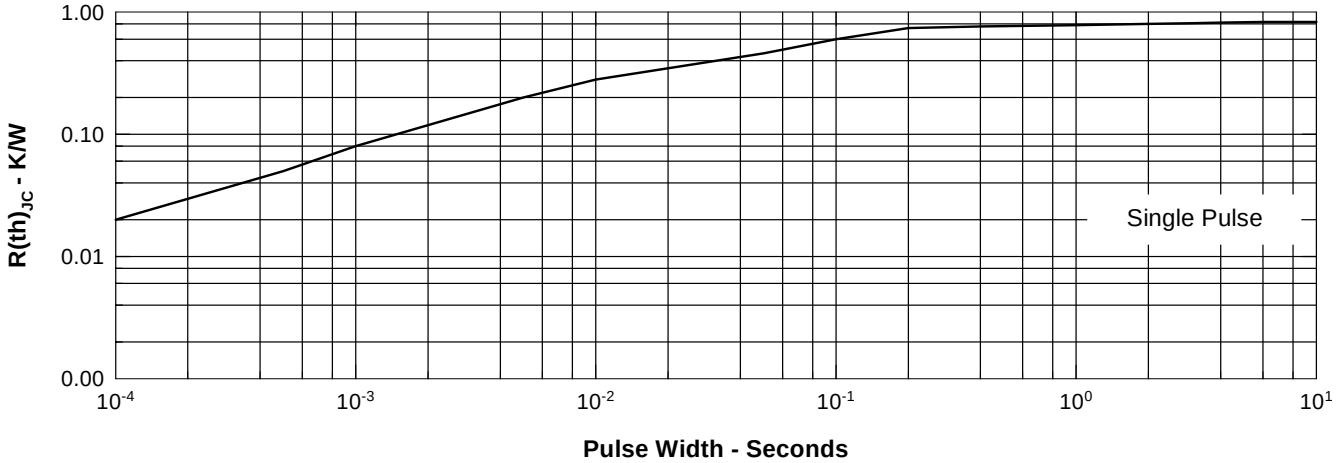


Fig. 10 Transient Thermal Impedance