STK18TA8

nvTime™ Event Data Recorder
Serial Peripheral Interface nvSRAM
QuantumTrap™ CMOS
Nonvolatile Static RAM

Preliminary

FEATURES

- **Data integrity of Simtek nvSRAM Combined with Full-Featured Real-Time Clock**
- **40 MHZ SPI interface with compatible commands to industry standards 1 Mbit SPI EEPROMs**
- ***STORE* to *QuantumTrap*™ Nonvolatile Elements is Initiated by Software , device pin or *AutoStore*™ on Power Down**
- ***RECALL* to SRAM Initiated by Software or Power Restore**
- **Unlimited *READ* and *WRITE* and *RECALL* Cycles**
- **Watchdog Timer**
- **Clock Alarm with programmable Interrupts**
- **Capacitor or battery backup for RTC**
- **Single 3V +20%, -10% Operation**
- **Commercial and Industrial Temperatures**
- **High-reliability**
  - **Endurance to 1 Million Cycles**
  - **Retention to 100 years at 85 ºC**
- **Package: 48-Pin SSOP**

DESCRIPTION

The Simtek STK18TA8 combines a 1 Mbit nonvolatile static RAM and a full-featured real-time clock, in a reliable, monolithic integrated circuit. A Serial Peripheral Interface (SPI) makes system integration simple. The embedded nonvolatile elements incorporate Simtek's *QuantumTrap*™ technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable *QuantumTrap*™ cell. Data transfers from the SRAM to the nonvolatile elements (the *STORE* operation) takes place automatically at power down. On power up, data is restored to the SRAM (the *RECALL* operation) from the nonvolatile memory. Both the *STORE* and *RECALL* operations are also available under software control.

The Real-Time Clock function provides an accurate clock with leap year tracking and a programmable, high accuracy oscillator. The Alarm function is programmable for one-time alarms or periodic seconds, minutes, hours, or days. There is also a programmable Watchdog Timer for process control.

BLOCK DIAGRAM

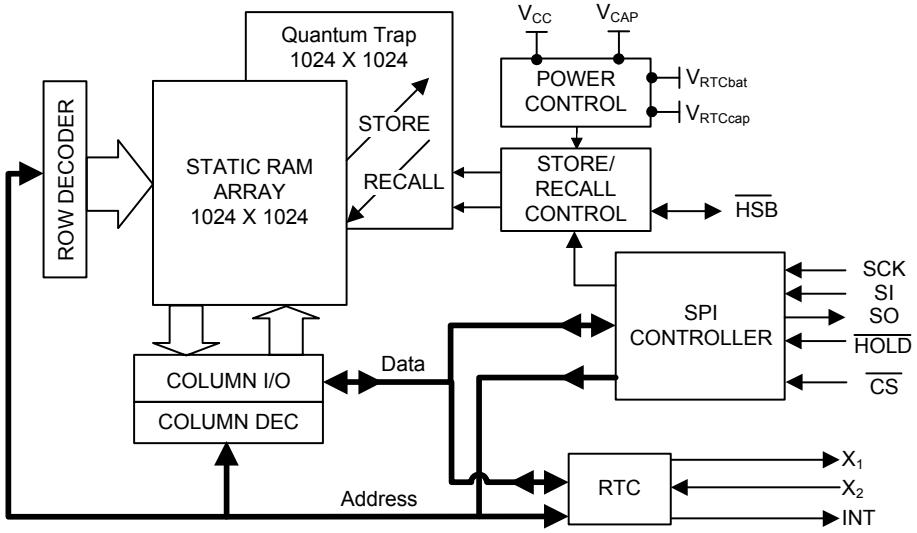
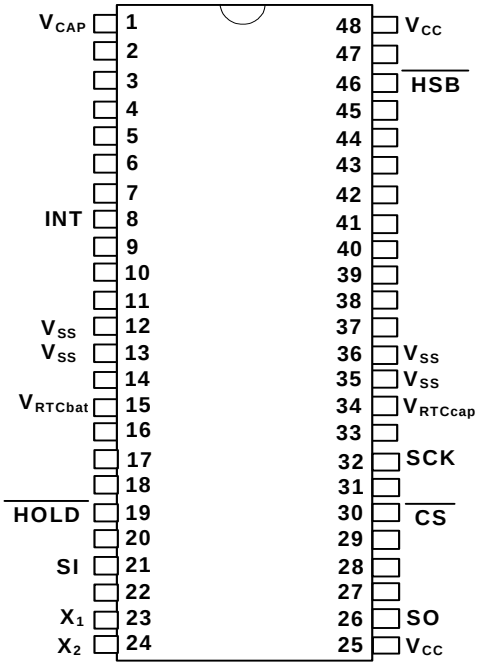


Figure 1. Block Diagram

PACKAGES



48 Pin SSOP

PCB area usage.
See website for detailed package size specifications.

PIN DESCRIPTIONS

Pin Name	I/O	Description
SI - Serial Input	Input	The SI pin is used to transfer data into the device. Data is latched from this pin on the rising edge of the SCK clock pin. Instructions, addresses and data are all transmitted over this pin.
SO - Serial Output	3-state Output	The SO pin is used to transfer data out of the STK18TA8. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.
$\overline{CS}$ - Chip Select	Input	A low level on this pin selects the device. A falling edge is required on $\overline{CS}$ before each command code. Nonvolatile operations which are already in progress will be completed regardless of the $\overline{CS}$ input signal. When the device is deselected, SO goes to the high impedance state allowing other devices to share the SPI bus. When $\overline{CS}$ is held high and all internal commands have completed the device enters the standby mode (low-power).
SCK - Serial Clock	Input	The SCK is used to synchronize the communication between a master and the STK18TA8. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data placed on the SO pin changes on the falling edge of the clock input.
$\overline{HOLD}$	Input	The $\overline{HOLD}$ pin is used to pause the serial interface. If $\overline{HOLD}$ is driven low, the chip ignores all serial input as long as $\overline{CS}$ is held low. When $\overline{HOLD}$ is again driven high, normal operation resumes on the next clock edge. If $\overline{CS}$ is driven high at any time, the hold operation is aborted. This pin has an internal pullup.
V_{CC} - Chip Power	Power	The V_{CC} pin supplies the power for the chip during normal operation.
V_{SS} - Chip Ground	Power	Ground.
V_{CAP} - Power for Non-volatile *AutoStore*™	Power	A capacitor should be connected with a minimum of 17uF, 5V minimum. Upon power down, V_{CAP} supplies the power for the *AutoStore*™ operation whereby SRAM data elements are transferred in parallel to the nonvolatile *QuantumTrap*™ elements.
V_{RTCcap}	Power	Capacitor supplied backup RTC supply voltage. (Left unconnected if V_{RTCbat} is used.)
V_{RTCbat}	Power	Battery supplied backup RTC supply voltage. (Left unconnected if V_{RTCcap} is used.)
X_1 - Crystal Out	Output	Crystal Connection, drives crystal on startup.
X_2 - Crystal in	Input	Crystal Connection, 32.768Khz crystal.
$\overline{HSB}$ - STORE request and status	In/Output	When low this output indicates a Hardware Store is in progress. When pulled low externally to the chip it will initiate a nonvolatile STORE operation. Left undriven the pin is weakly pulled up internal to the chip. STORE operation will not be started when V_{CC} is below V_{switch}.
INT - interrupt out	Output	Pin which can be programmed to respond to the clock alarm, the watchdog timer, or the power monitor. Programmable to either active high (push/pull) or active low (open-drain).
(Blank)	No Connect	Unlabeled pins should be left with no connections on the printed circuit board.

ABSOLUTE MAXIMUM RATINGS[a]

Power Supply Voltage	-0.5V to +4.1V
Voltage on Input Relative to V_{SS}	-0.5V to (V_{CC} + 0.5V)
Voltage on Outputs	-0.5V to (V_{CC} + 0.5V)
Temperature under Bias	–55°C to 125°C
Junction Temperature	–55°C to 140°C
Storage Temperature	–65°C to 150°C
Power Dissipation	1W
DC Output Current (1 output at a time, 1s duration)	15mA

Notes
a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Package Thermal Characteristics see website: http://www.simtek.com/

DC CHARACTERISTICS

Symbol	Parameter	Commercial		Industrial		Units	Notes
		MIN	MAX	MIN	MAX		
I_{CC1}	Average V_{CC} Current		10		10	mA	Based on 40MHz cycle rate. Values obtained without output loads.
I_{CC2}	Average V_{CC} Current during STORE		3		3	mA	All Inputs Don't Care, V_{CC} = max Average current for duration of *STORE* cycle (t_{STORE}).
I_{CC4}	Average V_{CAP} Current during *AutoStore*™ Cycle		3		3	mA	All Inputs Don't Care Average current for duration of *STORE* cycle (t_{STORE}).
I_{SB}	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		2		2	mA	All Others $V_{IN} \le 0.2V$ or $\ge (V_{CC} - 0.2V)$ Standby current level after nonvolatile cycle is complete.
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – 0.5	0.8	V_{SS} – 0.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4mA
T_A	Operating Temperature	0	70	–40	85	°C	
V_{CC}	Operating Voltage	2.7	3.6	2.7	3.6	V	Nominal 3.0V +20%, -10% used for tested specifications.
V_{CAP}	Storage Capacitor	17	57	17	57	µf	Between Vcap pin and Vss, 5V rated.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 2 and Figure 3

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Notes
b: These parameters are guaranteed but not tested

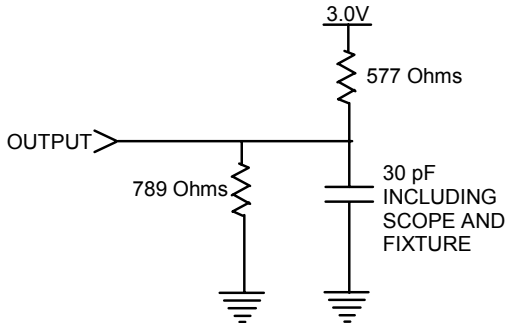


Figure 2. AC Output Loading

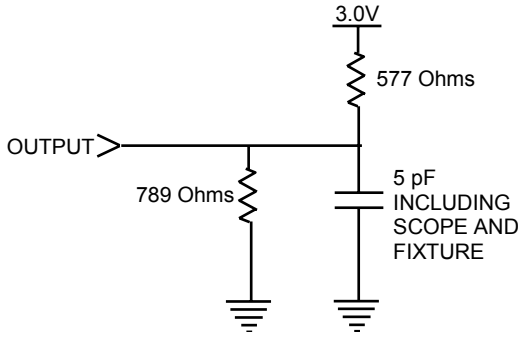
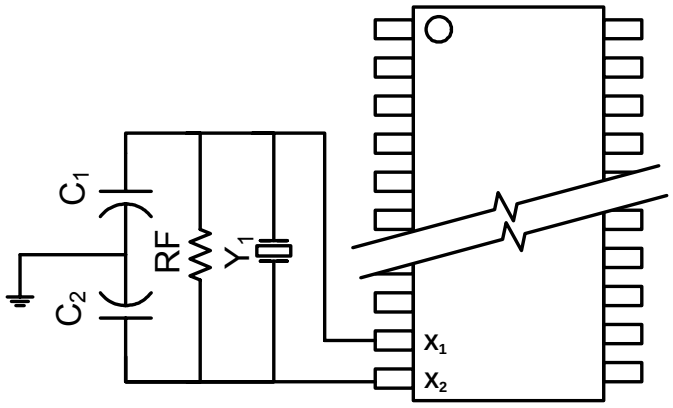


Figure 3. AC Output Loading, for tri-state specs (t_{DIS})

RTC DC CHARACTERISTICS

Symbol	Parameter	Commercial		Industrial		Units	Notes
		MIN	MAX	MIN	MAX		
I_{BAK}	RTC Backup Current	-	300	-	350	nA	From either V_{RTCcap} or V_{RTCbat}
V_{RTCbat}	RTC Battery Pin Voltage	1.8	3.3	1.8	3.3	V	Typical = 3.0 Volts during normal operation
V_{RTCcap}	RTC Capacitor Pin Voltage	1.2	2.7	1.2	2.7	V	Typical = 2.4 Volts during normal operation
t_{OSCS}	RTC Oscillator time to start	-	1	-	1	min	@ MIN Temperature from Power up or Enable
		-	10	-	10	sec	@25ºC from Power up or Enable

RTC RECOMMENDED COMPONENT CONFIGURATION



Recommended Values

Y_1 = 32.768 KHz

RF = 10M Ohm

C_1 = 2.2 pF

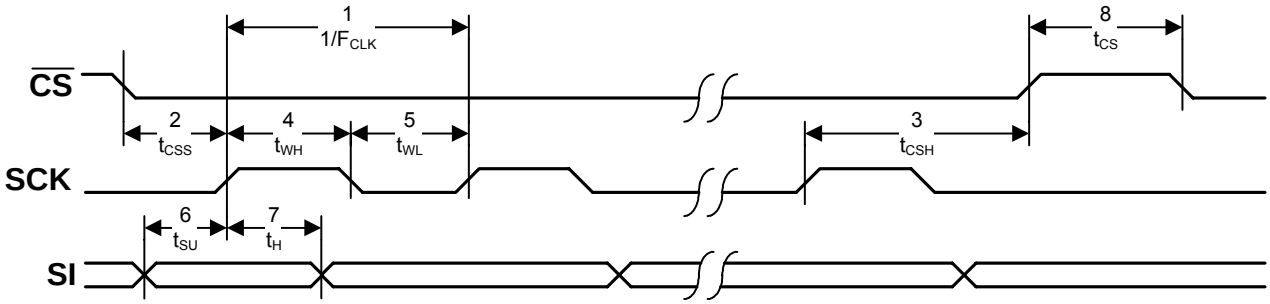
C_2 = 47 pF

Figure 4. RTC COMPONENT CONFIGURATION

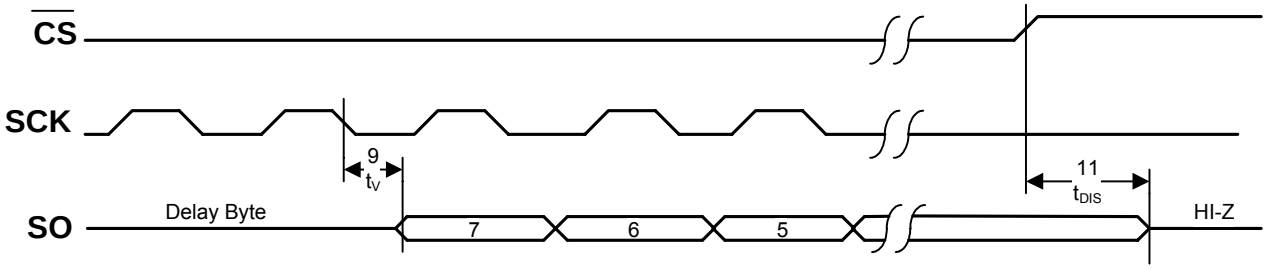
AC PARAMETERS

NO.	SYMBOLS	PARAMETER	STK18TA8		UNITS
			MIN	MAX	
1	F_{CLK}	Clock Frequency		40	MHZ
2	t_{CSS}	$\overline{CS}$ setup time	5		ns
3	t_{CSH}	$\overline{CS}$ hold time	25		ns
4	t_{WH}	SCK high time	10		ns
5	t_{WL}	SCK low time	10		ns
6	t_{SU}	SI, Setup time	3		ns
7	t_H	SI, hold time	5		ns
8	t_{CS}	$\overline{CS}$ high time	5		ns
9	t_V	Falling SCK to Output valid		7	ns
10	t_{HO}	Output hold time		3	ns
11	t_{DIS}	Output Disable time		10	ns

SPI™ Input Timing



SPI™ Output Timing



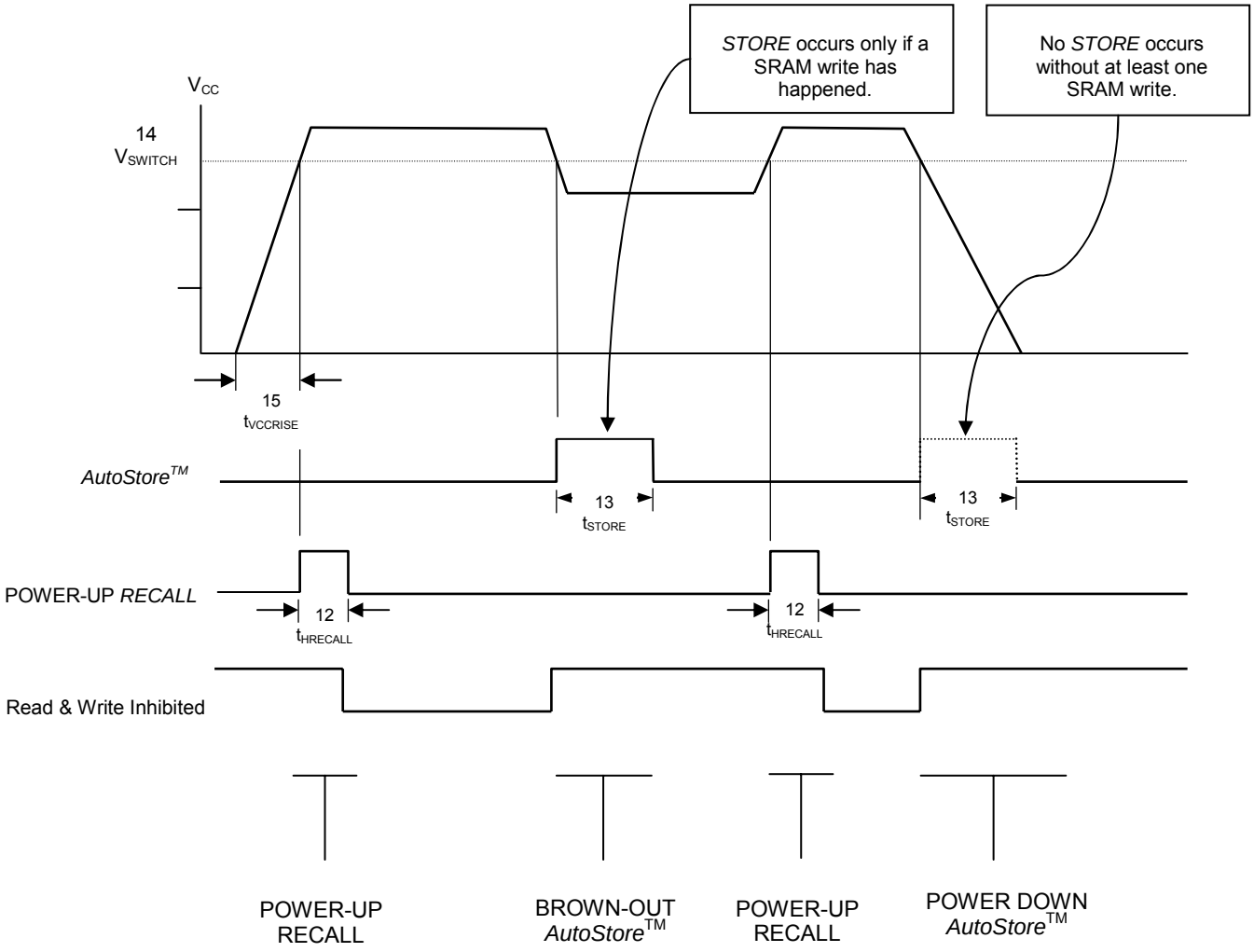
*AutoStore™ /*POWER-UP *RECALL*

NO.	SYMBOLS	PARAMETER	STK18TA8		UNITS	Notes
			MIN	MAX		
12	$t_{HRECALL}$	Power-up RECALL Duration		20	ms	c
13	t_{STORE}	STORE Cycle Duration		12.5	ms	d
14	V_{SWITCH}	Low Voltage Trigger Level	2.55	2.65	V	
15	$t_{VCCRISE}$	V_{CC} Rise Time	150		µs	

Notes

c: $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}

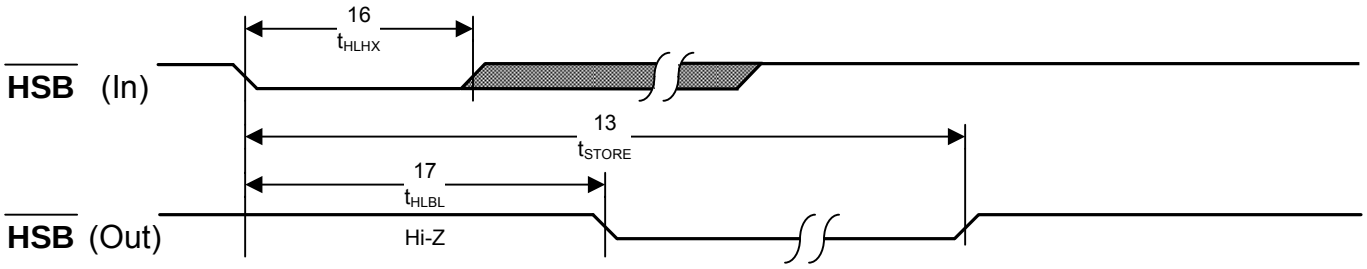
d: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place



Note: Read and Write cycles will be ignored during *STORE, RECALL* and while V_{CC} is below V_{SWITCH}.

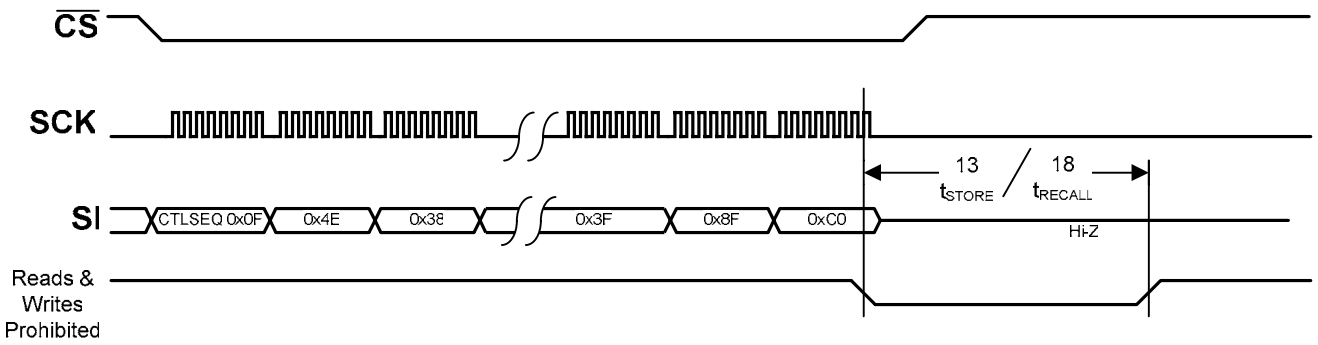
HARDWARE *STORE* CYCLE

NO.	SYMBOLS		PARAMETER	STK18TA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
16	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
17	t_{HLBL}		Hardware *STORE* Low to *STORE* Busy		300	ns	



SOFTWARE *STORE* CYCLE (CTLSEQ COMMAND)

NO.	SYMBOLS		PARAMETER	STK18TA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
18	t_{RECALL}		RECALL Duration		40	µs	



Note: The parameter t_{STORE} or t_{RECALL} are substituted for STORE or RECALL command respectively.

Endurance Parameters

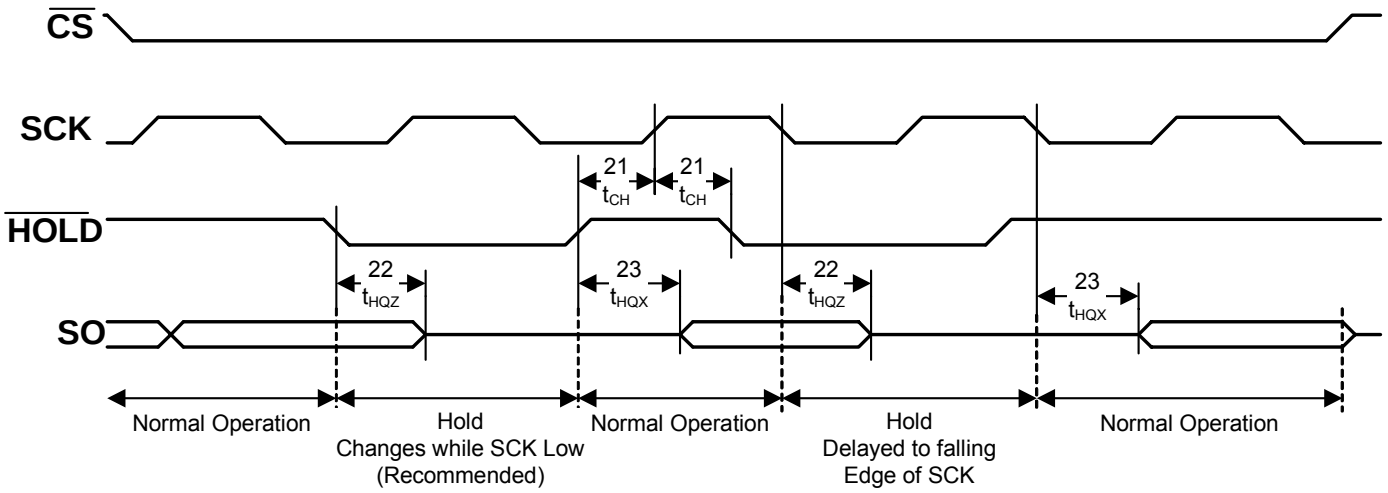
NO.	SYMBOLS		PARAMETER	STK18TA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
19			SRAM write cycles		Infinite	cycles	
20			Number of STORE cycles		1×10^6	cycles	

HOLD Signal Timing

NO.	SYMBOLS		PARAMETER	STK18TA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
21	t_{CH}		SCK to $\overline{HOLD}$ Change	5		ns	e
22	t_{HQZ}		$\overline{HOLD}$ active to Output Inactive		10	ns	
23	t_{HQX}		$\overline{HOLD}$ Inactive to Output Active	0		ns	

Notes

e: It is recommended that $\overline{HOLD}$ change on negative transitions of the SCK or while SCK is low.



SERIAL PERIPHERAL INTERFACE

Serial Interface Description

The STK18TA8 is a 1 Mbit Serial nvSRAM (SRAM + nonvolatile element in a combined cell) with 128K x 8 organization designed to interface directly with the Serial Peripheral Interface (SPI) port of many popular microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software. The STK18TA8 SPI interface contains an 8-bit instruction register. Data is clocked into the device through the SI pin on the rising edge of SCK. The $\overline{CS}$ pin must be low for the entire data transfer. Table 1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last. Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. Refer to Figure 5 which shows the connection of multiple SPI devices. The SO output is shared since only the slave selected by $\overline{CS}$ and a valid opcode is returns data to the master. If no slave is selected the SO pin is tri-stated. If the master device has a bi-directional pin capability, the SO and SI pins may be shared by having the master switch the pin to input when data is expected from one of the slave SPI devices.

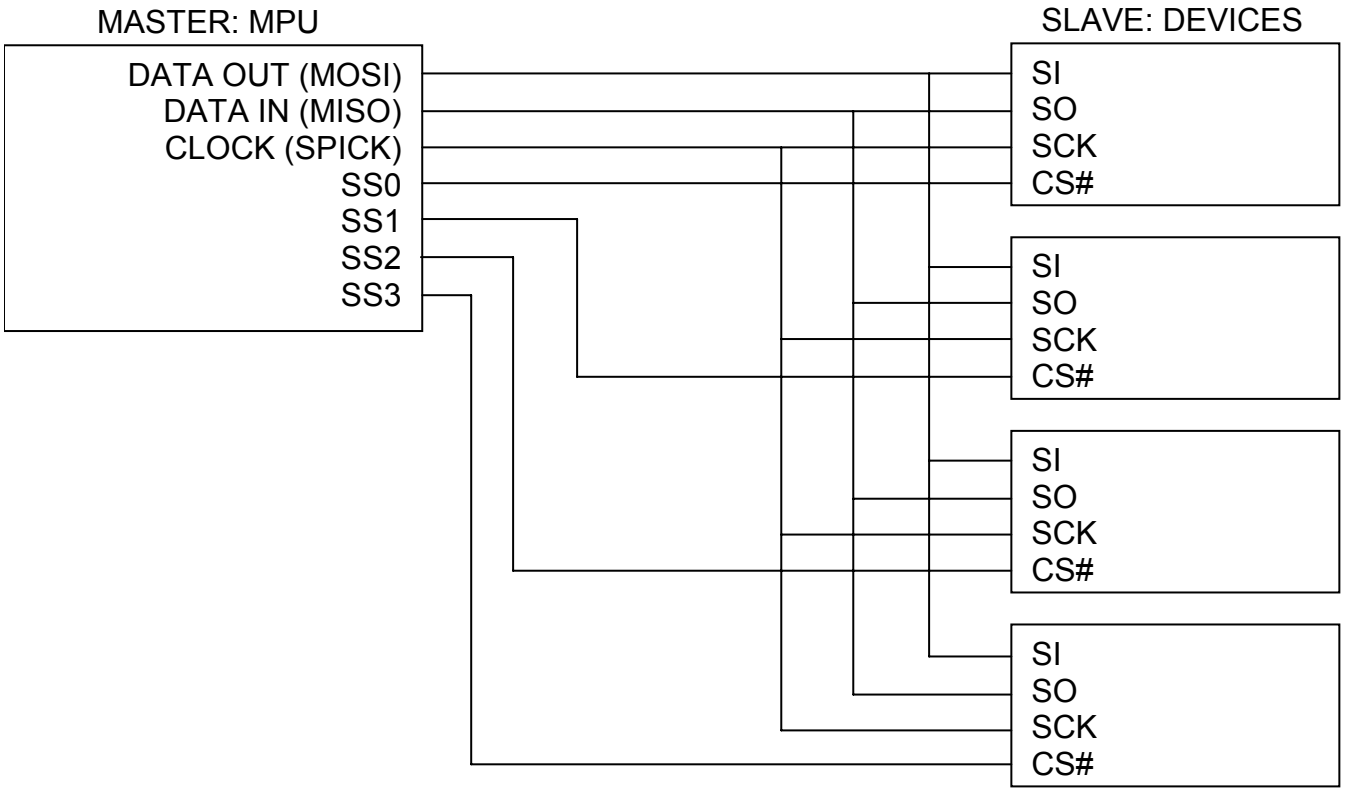


Figure 5. Multiple Device System

Table 1. SPI™ INSTRUCTION SET

Instruction Name	Code	Description
READ	0x03	Read SRAM data from selected address.
WRITE	0x02	Write SRAM data from selected address.
FREAD	0x0B	Fast read of SRAM data from selected address. (First byte is the delay byte).
CTLSEQ	0x0F	Device control command sequence.

Table 2. CONTROL COMMAND SEQUENCES

Command Name	CMD Bytes	Description
STORE	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F **0x8FC0**	Commands Device to transfer the SRAM data to the nonvolatile memory elements.
RECALL	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F **0x4C63**	Commands Device to transfer the nonvolatile memory contents to the SRAM memory.
AUTOENA	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F **0x4B46**	Turns on the AUTOSTORE™ feature of the device, enabling automatic stores to nonvolatile memory when V_{CC} drops below V_{SWITCH}.
AUTODIS	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F **0x8B45**	Turns off the AUTOSTORE™ feature of the device, disabling the automatic stores to nonvolatile memory. STORES invoked by the control command STORE sequence and stores invoked by driving the HSB pin remain enabled.

SPI modes explained

SPI mode 0 and 3 are supported for the STK18TA8 device. In both modes, data is received from the SPI master by presenting data t_{SU} ns before the rising edge of the clock. Data is driven out the SO pin on the falling edge of SCK and received by the SPI master on the rising edge. Mode 0 and mode 3 differ in the state of the SCK signal when $\overline{CS}$ falls or rises. Mode 0 has SCK=0 during SCK falls or rises. Mode 3 has SCK high when $\overline{CS}$ falls or rises. The mode is important for hardware SPI controllers and less so for firmware based control. Refer to **Figure 6** for a diagram of signal waveforms.

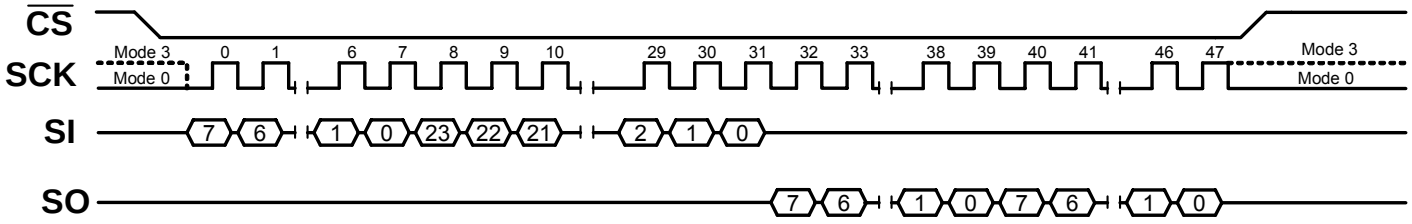


Figure 6. SPI Mode Waveforms

DEVICE OPERATION

nvSRAM

The STK18TA8 nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile *QuantumTrap*™ cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the *STORE* operation), or from the nonvolatile cell to SRAM (the *RECALL* operation). This unique architecture allows all cells to be stored and recalled in parallel. During the *STORE* and *RECALL* operations SRAM READ and WRITE operations are inhibited. The STK18TA8 supports unlimited reads and writes just like a typical SRAM. In addition, it provides unlimited *RECALL* operations from the nonvolatile cells and up to 1 million *STORE* operations.

SRAM READ

Reading the STK18TA8 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code is transmitted via the SI line clocked in on each rising edge of SCK followed by a 3 byte address to be read (Refer to Table 6). All data is sent with the most significant bit first. After the address bytes SCK must complete eight cycles. This allows time for the memory to be access and the data to be loaded into the output shift register.

On the falling edge of the 32th clock cycle (after the command, and 3 address bytes) the data at the specified address is shifted out on the SO output. Every falling edge of SCK will generate another data bit to be sampled by the master device on the next rising edge of SCK. The READ command can be continued by continuously holding the $\overline{CS}$ line low and supplying additional SCK pulses. Internally the byte address is automatically incremented and data will continue to be shifted out. The delay byte is only required on first memory access after the READ command. All subsequent READs are pipelined and are output on consecutive SCK falling edges. When the highest SRAM address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle. When the $\overline{CS}$ line goes inactive the READ command is terminated.

Please note that the top 16 bytes of the memory space represent the RTC functions. The proper method for reading these registers accurately is described in the "Real Time Clock Operation" section of this document. To logically separate the RTC registers from the SRAM accesses, READ commands wrap back to 0x0000 after accessing 0x1FFEF. READs from addresses above 0x1FFEF, which represents the RTC address space, do not advance the address counter. Only 1 byte is read. As long as $\overline{CS}$ is held low the same byte will continue be read.

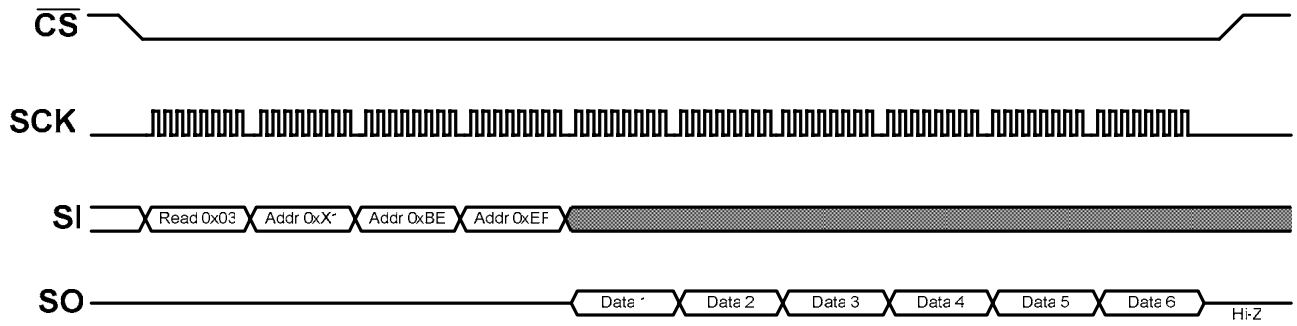


Figure 7. Read Command Multi-byte Example

SRAM FREAD

A fast READ command is also provided on the STK18TA8 SPI interface. This command operates like the standard READ command except that a delay byte is inserted between the last address bit and the first valid data bit. The master SPI controller is required to supply 8 delay byte clock cycles. On the rising edge of the 9th cycle the most significant bit of the memory byte is ready to on the SO output. This command is provided for systems that require the maximum clock frequency but are unable to provide the delay required for the SRAM access prior to valid data on SO. SO is not driven during the delay byte and data during this time period is considered invalid.

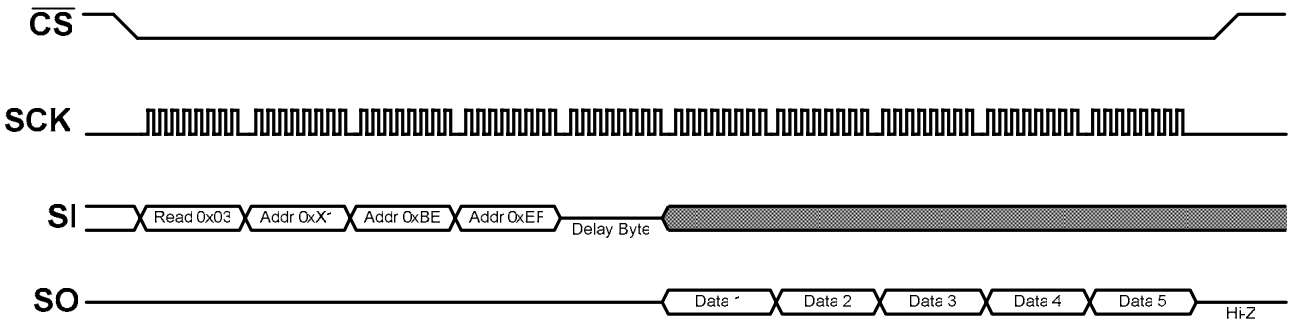


Figure 8. Fast Read Command Multi-byte Example

SRAM WRITE

Writing to the STK18TA8 requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted via the SI line (MSB first) followed by a three-byte address and the data (D7 - D0) to be programmed (Refer to Table 6). A single or unlimited number of data bytes may be sent after the first byte and the address will increment after each byte is received. The WRITE command is terminated when $\overline{CS}$ pin goes inactive.

Please note that the top 16 bytes of the memory space represent the RTC registers on the chip. The proper method for writing these registers accurately is described in the “Real Time Clock Operation” section of this document.

To logically separate the RTC registers from the SRAM access WRITE commands will wrap back to 0x0000 after writing 0x1FFEF. WRITEs targeted for addresses above 0x1FFEF which represent the RTC address space, do not advance the address counter. Only one data byte is expected in write commands targeted for the RTC. If multiple bytes are sent, later bytes will overwrite bytes sent earlier.

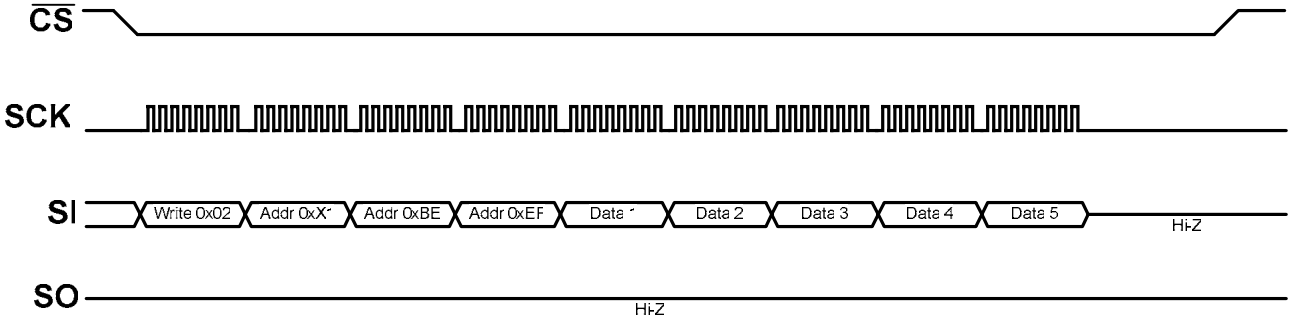


Figure 9. Write Command Multi-byte Example

AutoStore™ OPERATION

The STK18TA8 stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store, activated by $\overline{\text{HSB}}$, Software Store, activated by a SPI command, and *AutoStore*™, activated on device power down.

AutoStore™ operation is a unique feature of Simtek *QuantumTrap*™ technology and is enabled by default on the STK18TA8.

During normal operation, the device will draw current from Vcc to charge a capacitor connected to the Vcap pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the Vcc pin drops below Vswitch, the part will automatically disconnect the Vcap pin from Vcc. A STORE operation will be initiated with power provided by the Vcap capacitor.

Figure 10 shows the proper connection of the storage capacitor (Vcap) for automatic store operation. Refer to the DC CHARACTERISTICS table for the size of Vcap. The voltage on the Vcap pin is driven to 5V by a charge pump internal to the chip.

To reduce unneeded nonvolatile stores, *AutoStore*™ and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place. The $\overline{\text{HSB}}$ signal can be monitored by the system to detect a STORE cycle is in progress.

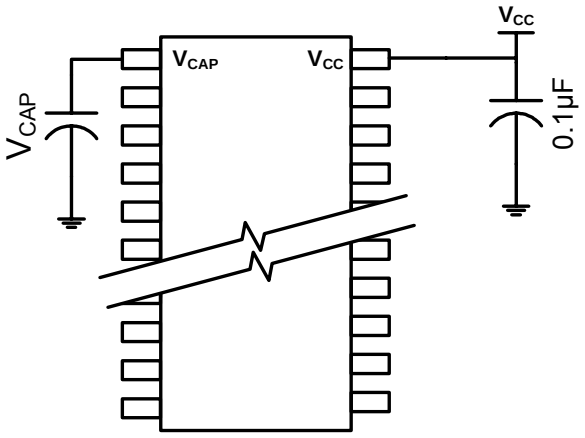


Figure 10. *AutoStore*™ Mode

HARDWARE *STORE* ($\overline{\text{HSB}}$) OPERATION

The STK18TA8 provides the $\overline{\text{HSB}}$ pin for controlling and monitoring the *STORE* operations. The $\overline{\text{HSB}}$ pin can be used to request a hardware *STORE* cycle. When the $\overline{\text{HSB}}$ pin is driven low, the STK18TA8 will conditionally initiate a *STORE* operation. An actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or *RECALL* cycle. The $\overline{\text{HSB}}$ pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress.

The SPI controller checks the state of the $\overline{\text{HSB}}$ pin just after the final bit of each byte being written. If $\overline{\text{HSB}}$ is active the WRITE operation is cancelled. However, if $\overline{\text{HSB}}$ goes low after the WRITE operation has been initiated the WRITE will complete before the *STORE* operation is started. Memory READ and incomplete SPI commands will be cancelled and/or ignored when $\overline{\text{HSB}}$ is active. During any *STORE* operation, regardless of how it was initiated, the STK18TA8 will continue to drive the $\overline{\text{HSB}}$ pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK18TA8 will remain disabled until the $\overline{\text{HSB}}$ pin returns high.

If $\overline{\text{HSB}}$ is not used, it should be left unconnected.

HARDWARE *RECALL* (POWER-UP)

During power up, or after any low-power condition (V_{CC} < V_{SWITCH}), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{HRECALL}$ to complete.

SOFTWARE *STORE*

Data can be transferred from the SRAM to the nonvolatile memory by using a SPI command. The STK18TA8 software *STORE* cycle is initiated by issuing a CTLSEQ command through the SPI interface. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a *STORE* cycle is initiated, further READ and WRITE commands are ignored until the cycle is completed. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation. Please see Table 2 and Figure 11 for details on how to issue the appropriate CTLSEQ.

SOFTWARE *RECALL*

Data can be transferred from the nonvolatile memory to the SRAM by using a SPI command. A software *RECALL* cycle is initiated by issuing a CTLSEQ command through the SPI interface. Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. Once a *RECALL* cycle is initiated, further READ and WRITE commands are ignored until the cycle is completed. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements. Please see Table 2 and Figure 11 for details on how to issue the appropriate CTLSEQ.

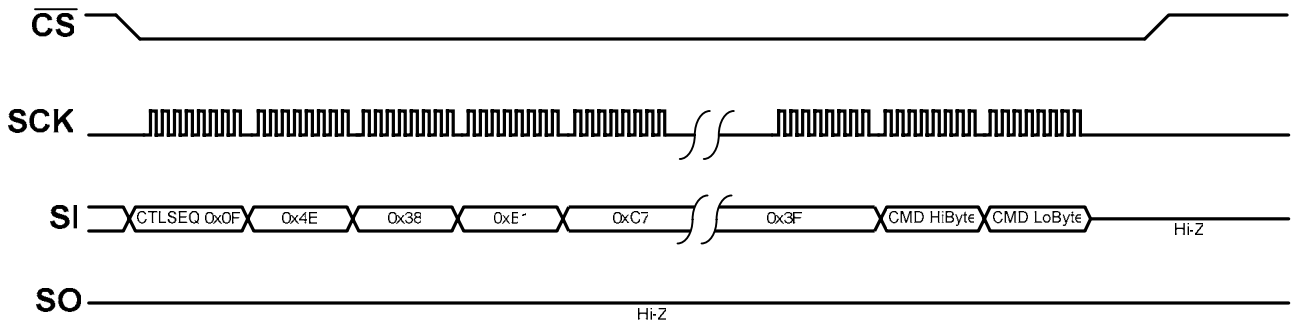


Figure 11. Control Sequence Command Example

PREVENTING *AUTOSTORE*™

The *AutoStore*™ function can be disabled by initiating an *AutoStore Disable* CTLSEQ command.

The *AutoStore*™ can be re-enabled by initiating an *AutoStore Enable* CTLSEQ command. If the *AutoStore*™ function is disabled or re-enabled a manual *STORE* operation (Hardware or Software) needs to be issued to save the *AutoStore* state through subsequent power down cycles. The part comes from the factory with *AutoStore*™ enabled. Please see Table 2 and Figure 11 for details on how to issue the appropriate CTLSEQ.

When *AutoStore*™ is disabled as described above the RTC registers are not saved on power down. If the RTC registers are changed during system operation a CTLSEQ *STORE* needs to be issued to update the non-volatile memory.

$\overline{\text{HOLD}}$ OPERATION

The $\overline{\text{HOLD}}$ pin is used to pause serial communications without aborting the command in progress. This can be useful if the SPI master is interrupted during a burst read or write to service another device. The $\overline{\text{HOLD}}$ signal is intended to be asserted while SCK is low and to be de-asserted again while SCK is low. $\overline{\text{HOLD}}$ is recognized by the STK18TA8 only when SCK is low. If $\overline{\text{HOLD}}$ changes state while SCK is high the hold state will not be recognized until the next falling edge of SCK. During the hold state SCK can toggle and devices sharing SO and SI can use these signal lines to communicate without disturbing the command in progress on this device. The STK18TA8 releases the SO pin during the duration of the hold operation so that other devices may communicate with the SPI master. $\overline{\text{CS}}$ must be held low selecting the device during the hold operation. If the $\overline{\text{CS}}$ goes high while a hold is in progress the command will be terminated.

DATA PROTECTION

The STK18TA8 protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low-voltage condition is detected when $V_{CC} < V_{SWITCH}$.

NOISE CONSIDERATIONS

The STK18TA8 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground and signals will reduce circuit noise.

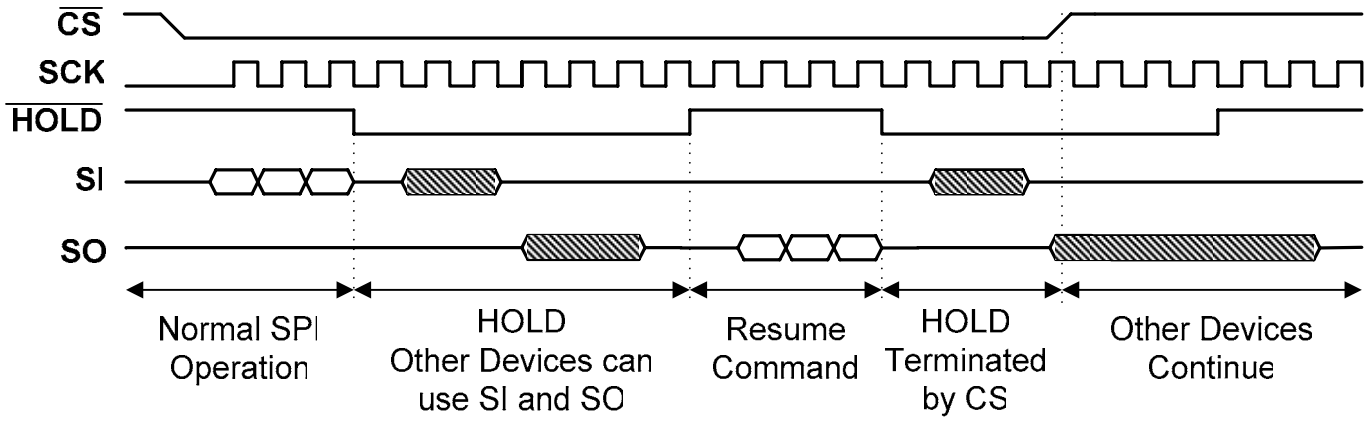


Figure 12. HOLD Operation Example

REAL TIME CLOCK OPERATION

nvTIME OPERATION

The STK18TA8 offers internal registers that contain Clock, Alarm, Watchdog, Interrupt, and Control functions. Internal double buffering of the clock and the clock/timer information registers prevents accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or clock accuracy of the internal clock while accessing clock data. Clock and Alarm Registers store data in BCD format.

CLOCK OPERATIONS

The clock registers maintain time up to 9,999 years in one second increments. The user can set the time to any calendar time and the clock automatically keeps track of days of the week and month, leap years and century transitions. There are eight registers dedicated to the clock functions which are used to set time with a write cycle and to read time during a read cycle. These registers contain the Time of Day in BCD format. Bits defined as "X" are currently not used and are reserved for future use by Simtek.

READING THE CLOCK

While the double-buffered RTC register structure reduces the chance of reading incorrect data from the clock, the user should halt internal updates to the STK18TA8 clock registers before reading clock data to prevent the reading of data in transition. Stopping the internal register updates does not affect clock accuracy.

The updating process is stopped by writing a "1" to the read bit "R" (in the flags register at 0x1FFF0), and will not restart until a "0" is written to the read bit. The RTC registers can then be read while the internal clock continues to run.

Within 20ms after a "0" is written to the read bit, all STK18TA8 registers are simultaneously updated.

SETTING THE CLOCK

Setting the write bit "W" (in the flags register at 0x1FFF0) to a "1" halts updates to the STK18TA8 registers. The correct day, date and time can then be written into the registers in 24-hour BCD format. The time written is referred to as the "Base Time." This value is stored in nonvolatile registers and used in calculation of the current time. Resetting the write bit to "0" transfers those values to the actual clock counters, after which the clock resumes normal operation.

BACKUP POWER

The RTC in the STK18TA8 is intended for permanently powered operation. Either the V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When primary power, V_{cc}, fails and drops below V_{switch} the device will switch to the backup power supply.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of clock operation with the primary source removed, the data stored in nvSRAM is secure, having been stored in the nonvolatile elements as power was lost. Factors to be considered when choosing a backup power source include: the expected duration of power outages and the cost trade-off of using a battery versus a capacitor.

During backup operation the STK18TA8 consumes a maximum of 300 nanoamps at 2 volts. Capacitor or battery values should be chosen according to the application. Backup time values based on maximum current specs are shown below. Nominal times are approximately 3 times longer.

Capacitor Value	Backup Time
0.1 F	72 hours
0.47 F	14 days
1.0 F	30 days

Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up.

If a battery is used, a 3V lithium is recommended and the STK18TA8 will only source current from the battery when the primary power is removed. The battery will not, however, be recharged at any time by the STK18TA8. The battery capacity should be chosen for total anticipated cumulative down-time required over the life of the system.

STOPPING AND STARTING THE OSCILLATOR

The $\overline{\text{OSCEN}}$ bit in calibration register at 0x1FFF8 controls the starting and stopping of the oscillator. This bit is nonvolatile and shipped to customers in the "enabled" (set to 0) state. To preserve battery life while system is in storage $\overline{\text{OSCEN}}$ should be set to a 1. This will turn off the oscillator circuit extending the battery life. If the $\overline{\text{OSCEN}}$ bit goes from disabled to enabled, it will take approximately 5 seconds (10 seconds max) for the oscillator to start.

The STK18TA8 has the ability to detect oscillator failure. This is recorded in the OSCF (Oscillator Failed bit) of the flags register at address 0x1FFF0. When the device is powered on (V_{CC} goes above V_{switch}) the $\overline{\text{OSCEN}}$ bit is checked for "enabled" status. If the $\overline{\text{OSCEN}}$ bit is enabled and the oscillator is not active, the OSCF bit is set. The user should check for this condition and then write a 0 to clear the flag. It should be noted that in addition to setting the OSCF flag bit, the time registers are reset to the “Base Time” (see the section “Setting the Clock”), which is the value last written to the timekeeping registers. The Control/Calibration register and the $\overline{\text{OSCEN}}$ bit are not affected by the oscillator failed condition.

If the voltage on the backup supply (either V_{RTCcap} or V_{RTCbat}) falls below their respective minimum level the oscillator may fail, leading to the oscillator failed condition which can be detected when system power is restored.

The value of OSCF should be reset to 0 when the time registers are written for the first time. This will initialize the state of this bit which may have become set when the system was first powered on.

CALIBRATING THE CLOCK

The RTC is driven by a quartz controlled oscillator with a nominal frequency of 32.768 KHz. Clock accuracy will depend on the quality of the crystal, usually specified to 35 ppm limits at 25°C. This error could equate to $\pm$ 1.53 minutes per month. The STK18TA8 employs a calibration circuit that can improve the accuracy to +1/-2 ppm at 25°C. The calibration circuit adds or subtracts counts from the oscillator divider circuit.

The number of times pulses are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in calibration register at 0x1FFF8. Adding counts speeds the clock up; subtracting counts slows the clock down. The Calibration bits occupy the five lower order bits in the control register 8. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit, where a “1” indicates positive calibration and a “0” indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary “1” is loaded into the register, only the first 2 minutes of the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles. That is +4.068 or -2.034 ppm of adjustment per calibration step in the calibration register.

In order to determine how to set the calibration one may set the CAL bit in the flags register at 0x1FFF0 to 1, which causes the INT pin to toggle at a nominal 512 Hz. Any deviation measured from the 512 Hz will indicate the degree and direction of the required correction. For example, a reading of 512.010124 Hz would indicate a +20 ppm error, requiring a -10 (001010) to be loaded into the Calibration register. Note that setting or changing the calibration register does not affect the frequency test output frequency.

ALARM

The alarm function compares user-programmed values to the corresponding time-of-day values. When a match occurs, the alarm event occurs. The alarm drives an internal flag, AF, and may drive the INT pin if desired.

There are four alarm match fields. They are date, hours, minutes and seconds. Each of these fields also has a Match bit that is used to determine if the field is used in the alarm match logic. Setting the Match bit to “0” indicates that the corresponding field will be used in the match process.

Depending on the Match bits, the alarm can occur as specifically as one particular second on one day of the month, or as frequently as once per second

continuously. The MSB of each alarm register is a Match bit. Selecting none of the Match bits (all 1's) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to "0" causes the logic to match the seconds alarm value to the current time of day. Since a match will occur for only one value per minute, the alarm occurs once per minute. Likewise, setting the seconds and minutes Match bits causes an exact match of these values. Thus, an alarm will occur once per hour. Setting seconds, minutes and hours causes a match once per day. Lastly, selecting all match values causes an exact time and date match. Selecting other bit combinations will not produce meaningful results; however the alarm circuit should follow the functions described.

There are two ways a user can detect an alarm event, by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0x1FFF0 will indicate that a date/time match has occurred. The AF bit will be set to 1 when a match occurs. Reading the Flags/Control register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

WATCHDOG TIMER

The watchdog timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the Watchdog Timer register.

The counter consists of a loadable register and a free running counter. On power up, the watchdog time-out value in register 0x1FFF7 is loaded into the counter load register. Counting begins on power up and restarts from the loadable value any time the Watchdog Strobe (WDS) bit is set to 1. The counter is compared to the terminal value of 0. If the counter reaches this value, it causes an internal flag and an optional interrupt output. The user can prevent the time-out interrupt by setting WDS bit to 1 prior to the counter reaching 0. This causes the counter to be reloaded with the watchdog time-out value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt and flag never occurs.

New time-out values can be written by setting the watchdog write bit to 0. When the $\overline{WDW}$ is 0 (from the previous operation), new writes to the watchdog time-out value bits D_5-D_0 allow the time-out value to be modified. When $\overline{WDW}$ is a 1, then writes to bits D_5-D_0 will be ignored. The $\overline{WDW}$ function allows a user to set the WDS bit without concern that the watchdog timer value will be modified. A logical diagram of the watchdog timer is shown below. Note that setting the watchdog time-out value to 0 would be otherwise meaningless and therefore disables the watchdog function.

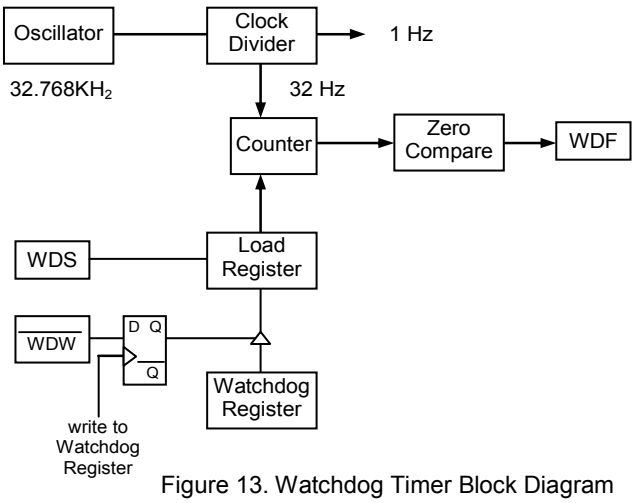


Figure 13. Watchdog Timer Block Diagram

The output of the watchdog timer is a flag bit WDF that is set if the watchdog is allowed to time-out. The flag is set upon a watchdog time-out and cleared when the Flags/Control register is read by the user. The user can also enable an optional interrupt source to drive the INT pin if the watchdog time-out occurs.

POWER MONITOR

The STK18TA8 provides a power management scheme with power-fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low-V_{CC} access. The power monitor is based on an internal band-gap reference circuit that compares the V_{CC} voltage to various thresholds.

As described in the *AutoStore*™ section previously, when V_{switch} is reached as V_{CC} decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source no data may be read or written and the clock functions are not available to the user. The clock continues to operate in the background. Updated clock data is available to

the user after $t_{HRECALL}$ delay (See *AutoStore™ /POWER-UP RECALL*) after V_{CC} has been restored to the device.

INTERRUPTS

The STK18TA8 provides three potential interrupt sources. They include the watchdog timer, the power monitor, and the clock/calendar alarm. Each can be individually enabled and assigned to drive the INT pin. In addition, each has an associated flag bit that the host processor can use to determine the cause of the interrupt.

Some of the sources have additional control bits that determine functional behavior. In addition, the pin driver has three bits that specify its behavior when an interrupt occurs. A functional diagram of the interrupt logic is shown below.

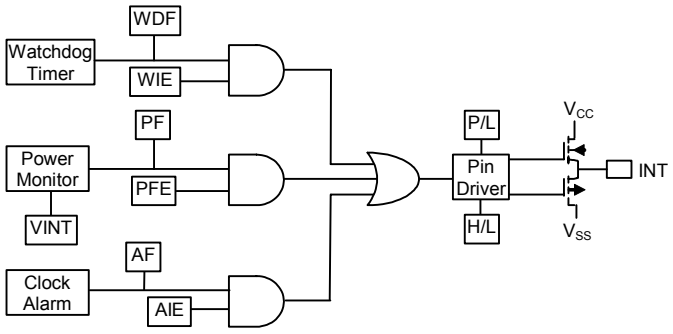


Figure 14. Interrupt Block Diagram

The three interrupts each have a source and an enable. Both the source and the enable must be active (true high) in order to generate an interrupt output. Only one source is necessary to drive the pin. The user can identify the source by reading the Flags/Control register, which contains the flags associated with each source. All flags are cleared to 0 when the register is read. The cycle must be a complete read cycle ($\overline{WE}$ high); otherwise the flags will not be cleared. The power monitor has two programmable settings that are explained in the power monitor section.

Once an interrupt source is active, the pin driver determines the behavior of the output. It has two programmable settings as shown below. Pin driver control bits are located in the Interrupts register.

According to the programming selections, the pin can be driven in the backup mode for an alarm interrupt. In addition, the pin can be an active low (open-drain) or an active high (push-pull) driver. If programmed for operation during backup mode, it can only be active low. Lastly, the pin can provide a one-shot function so that the active condition is a pulse or a level condition. In one-shot mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In level mode, the pin goes to its active polarity until the Flags/Control register is read by the user. This mode is intended to be used as an interrupt to a host microcontroller. The control bits are summarized as follows:

Watchdog Interrupt Enable - WIE. When set to 1, the watchdog timer drives the INT pin as well as an internal flag when a watchdog time-out occurs. When WIE is set to 0, the watchdog timer affects only the internal flag.

Alarm Interrupt Enable - AIE. When set to 1, the alarm match drives the INT pin as well as an internal flag. When set to 0, the alarm match only affects to internal flag.

Power Fail Interrupt Enable - PFE. When set to 1, the power fail monitor drives the pin as well as an internal flag. When set to 0, the power fail monitor affects only the internal flag.

High/Low - H/L. When set to a 1, the INT pin is active high and the driver mode is push-pull. The INT pin can drive high only when $V_{CC}>V_{switch}$. When set to a 0, the INT pin is active low and the drive mode is open-drain. Active low (open drain) is operational even in battery backup mode.

Pulse/Level - P/L. When set to a 1 and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a 0, the INT pin is driven high or low (determined by H/L) until the Flags/Control register is read.

When an enabled interrupt source activates the INT pin, an external host can read the Flags/Control register to determine the cause. Remember that all flags will be cleared when the register is read. If the INT pin is programmed for Level mode, then the condition will clear and the INT pin will return to its inactive state. If the pin is programmed for Pulse mode, then reading the flag also will clear the flag and the pin. The pulse will not complete its specified duration if the Flags/Control register is read. If the INT pin is used as a host reset, then the Flags/Control register should not be read during a reset.

During a power-on reset with no battery, the interrupt register is automatically loaded with the value 24h. This causes power-fail interrupt to be enabled with an active-low pulse.

RTC Register Map

Register	BCD Format Data								Function / Range
	D7	D6	D5	D4	D3	D2	D1	D0	
0x1FFFF	10s Years				Years				Years: 00-99
0x1FFFE	0	0	0	10s Months	Months				Months: 01-12
0x1FFFD	0	0	10s Day of Month		Day of Month				Day of Month: 01-31
0x1FFFC	0	0	0	0	0	Day of Week			Day of week: 01-07
0x1FFFB	0	0	10s Hours		Hours				Hours: 00-23
0x1FFFA	0	10s Minutes			Minutes				Minutes: 00-59
0x1FFF9		10s Seconds			Seconds				Seconds: 00-59
0x1FFF8	$\overline{\text{OSCEN}}$	0	Cal Sign	Calibration					Calibration values*
0x1FFF7	WDS	$\overline{\text{WDW}}$	WDT						Watchdog*
0x1FFF6	WIE	AIE	PFE	ABE	$\overline{\text{H/L}}$	$\overline{\text{P/L}}$	0	0	Interrupts*
0x1FFF5	$\overline{\text{M}}$	0	10s Alarm Date		Alarm Day				Alarm, Day of Month: 01-31
0x1FFF4	$\overline{\text{M}}$	0	10s Alarm Hours		Alarm Hours				Alarm, hours: 00-23
0x1FFF3	$\overline{\text{M}}$	10 Alarm Minutes			Alarm Minutes				Alarm, minutes: 00-59
0x1FFF2	$\overline{\text{M}}$	10 Alarm Seconds			Alarm Seconds				Alarm, seconds: 00-59
0x1FFF1	10s Centuries				Centuries				Centuries: 00-99
0x1FFF0	WDF	AF	PF	OSCF	0	CAL	W	R	Flags*

* - Is a binary value, not a BCD value.
0 - Not implemented, reserved for future use.

Register Map Detail

0x1FFFF	Timekeeping – Years							
	D7	D6	D5	D4	D3	D2	D1	D0
	10s Years				Years			
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99.							

0x1FFFE	Timekeeping – Months							
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	10s Month	Months			
	Contains the BCD digits of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12.							

0x1FFFD	Timekeeping – Date							
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	10s Day of month		Day of month			
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31. Leap years are automatically adjusted for.							

0x1FFFC	Timekeeping – Day							
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	Day of week		
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date.							

0x1FFFB	Timekeeping – Hours							
	D7	D6	D5	D4	D3	D2	D1	D0
	12/24	0	10s Hours		Hours			
	Contains the BCD value of hours in 24 hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23.							

0x1FFFA	Timekeeping – Minutes							
	D7	D6	D5	D4	D3	D2	D1	D0
	0	10s Minutes			Minutes			
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59.							

0x1FFF9	Timekeeping – Seconds							
	D7	D6	D5	D4	D3	D2	D1	D0
	0	10s Seconds			Seconds			
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59.							

0x1FFF8	Calibration / Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{\text{OSCEN}}$	0	Calibration Sign	Calibration				

$\overline{\text{OSCEN}}$	Oscillator Enable. When set to 1, the oscillator is halted. When set to 0, the oscillator runs. Disabling the oscillator saves battery/capacitor power during storage. On a no-battery power-up, this bit is set to 0.
Calibration Sign	Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base.
Calibration	These five bits control the calibration of the clock.

0x1FFF7	Watchdog Timer							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDS	$\overline{\text{WDW}}$	WDT					

WDS	Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no affect. The bit is cleared automatically once the watchdog timer is reset. The WDS bit is write only. Reading it always will return a 0.
$\overline{\text{WDW}}$	Watchdog Write Enable. Setting this bit to 1 masks the watchdog time-out value (WDT5-WDT0) so it cannot be written. This allows the user to strobe the watchdog without disturbing the time-out value. Setting this bit to 0 allows bits 5-0 to be written on the next write to the Watchdog register. The new value will be loaded on the next internal watchdog clock after the write cycle is complete. This function is explained in more detail in the watchdog timer section.
WDT	Watchdog time-out selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The minimum range or time-out value is 31.25 ms (a setting of 1) and the maximum time-out is 2 seconds (setting of 3Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the WDW bit was cleared to 0 on a previous cycle.

0x1FFF6	Interrupt Status / Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	WIE	AIE	PFIE	*ABE*	$\overline{\text{H/L}}$	$\overline{\text{P/L}}$	0	0

WIE	Watchdog Interrupt Enable. When set to 1 and a watchdog time-out occurs, the watchdog timer drives the INT pin as well as the WDF flag. When set to 0, the watchdog time-out affects only the WDF flag.
AIE	Alarm Interrupt Enable. When set to 1, the alarm match drives the INT pin as well as the AF flag. When set to 0, the alarm match only affects the AF flag.
PFIE	Power-Fail Enable. When set to 1, the alarm match drives the INT pin as well as the AF flag. When set to 0, the power-fail monitor affects only the PF flag.
ABE	Alarm Battery-backup Enable. When set to 1, the alarm interrupt (as controlled by AIE) will function even in battery backup mode. When set to 0, the alarm will occur only when V_{CC}>V_{switch}.
$\overline{\text{H/L}}$	High/Low. When set to a 1, the INT pin is driven active high. When set to 0, the INT pin is open drain, active low.
$\overline{\text{P/L}}$	Pulse/Level. When set to a 1, the INT pin is driven active (determined by $\overline{\text{H/L}}$) by an interrupt source for approximately 200 ms. When set to a 0, the INT pin is driven to an active level (as set by $\overline{\text{H/L}}$) until the Flags/Control register is read.

0x1FFF5	Alarm – Day							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{M}$	0	10s Alarm Date		Alarm Date			
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
$\overline{M}$	Match. Setting this bit to 0 causes the date value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.							

0x1FFF4	Alarm – Hours							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{M}$	0	10s Alarm Hours		Alarm Hours			
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
$\overline{M}$	Match. Setting this bit to 0 causes the hours value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hours value.							

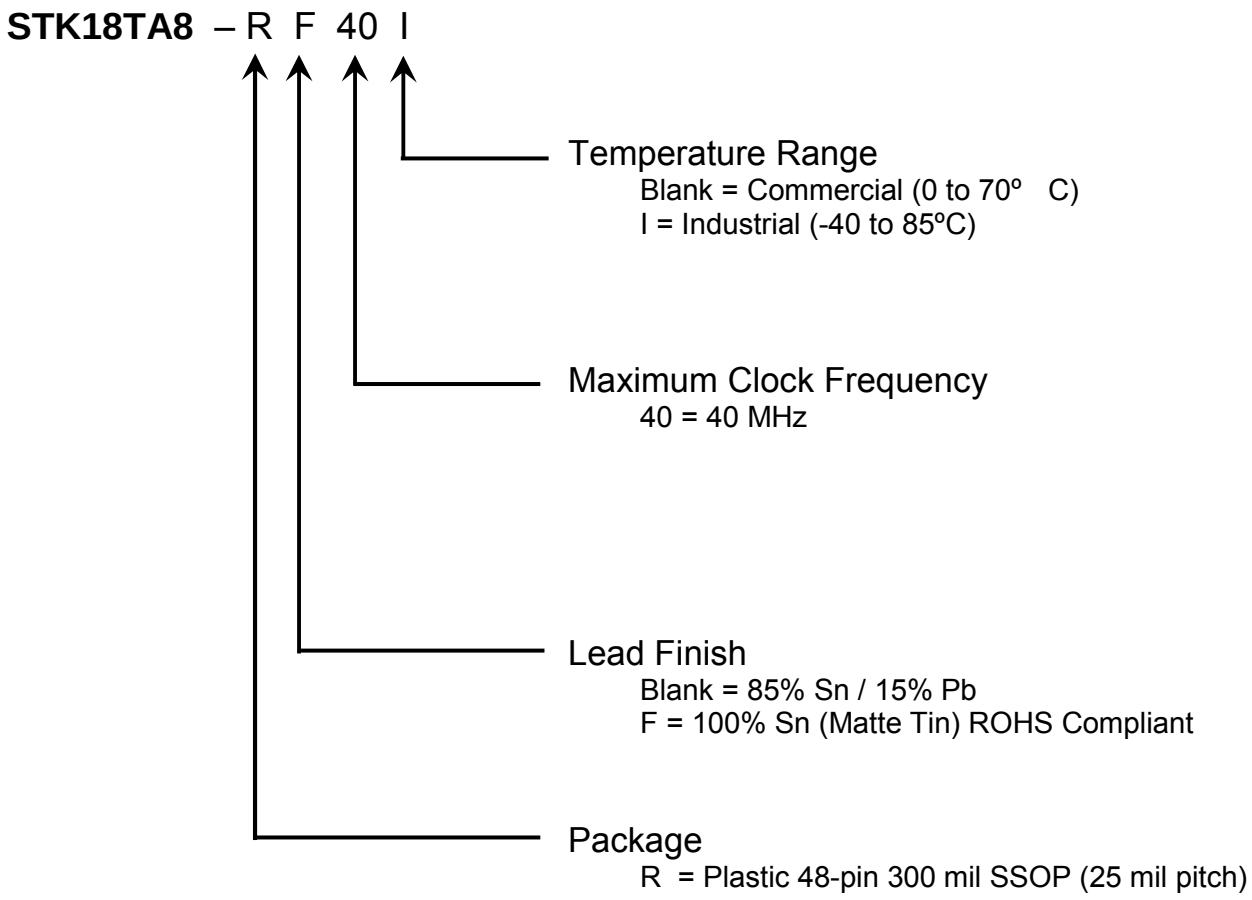
0x1FFF3	Alarm – Minutes							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{M}$	10s Alarm Minutes			Alarm Minutes			
	Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.							
$\overline{M}$	Match. Setting this bit to 0 causes the minutes value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the minutes value.							

0x1FFF2	Alarm – Seconds							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{M}$	10s Alarm Seconds			Alarm Seconds			
	Contains the alarm value for the seconds and the mask bit to select or deselect the seconds' value.							
$\overline{M}$	Match. Setting this bit to 0 causes the seconds' value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the seconds value.							

0x1FFF1	Timekeeping – Centuries							
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	10s Centuries		Centuries			

0x1FFF0	Flags							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDF	AF	PF	OSCF	0	CAL	W	R
WDF	Watchdog Timer Flag. This read-only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags/Control register is read.							
AF	Alarm Flag. This read-only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags/Control register is read.							
PF	Power-fail Flag. This read-only bit is set to 1 when power falls below the power-fail threshold V_{switch}. It is cleared to 0 when the Flags/Control register is read.							
OSCF	Oscillator Fail Flag. Set to 1 on power-up only if the oscillator is not running in the first 5ms of power-on operation. This indicates that time counts are no longer valid. The user must reset this bit to 0 to clear this condition. The chip will not clear this flag. This bit survives power cycles.							
CAL	Calibration Mode. When set to 1, a 512Hz square wave is output on the INT pin. When set to 0, the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power up.							
W	Write Time. Setting the W bit to 1 freeze updates of the timekeeping registers. The user can then write them with updated values. Setting the W bit to 0 causes the contents of the time registers to be transferred to the timekeeping counters.							
R	Read Time. Setting the R bit to 1 copies a static image of the timekeeping registers and places them in a holding register. The user can then read them without concerns over changing values causing system errors. The R bit going from 0 to 1 causes the timekeeping capture, so the bit must be returned to 0 prior to reading again.							

ORDERING INFORMATION



Document Revision History

Revision	Date	Summary
0.0	June 2003	Publish new datasheet
0.4	November 2004	Revised Feature Set
0.5	January 2005	Changed SI hold time t_H from 0 to 5 ns.
0.6	January 2005	Changed t_V, SCK to Data Valid from 5ns to 7ns. Changed $t_{SU,}$ SI hold time from 5ns to 3ns. Added $\overline{\text{HOLD}}$ signal to SPI interface.
0.7	January 2005	Removed RDSR Command.
0.8	April 2005	Changed RTC register unused bits "X" to require zero "0" value when writing values.

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