3.5A, 200V, 0.800 Ohm, N-Channel Power MOSFET

The 2N6790 is an N-Channel enhancement mode silicon gate power MOS field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This device can be operated directly from an integrated circuit.

Ordering Information

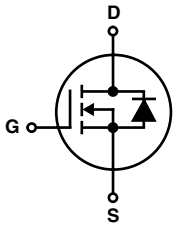
PART NUMBER	PACKAGE	BRAND
2N6790	TO-205AF	2N6790

NOTE: When ordering, include the entire part number.

Features

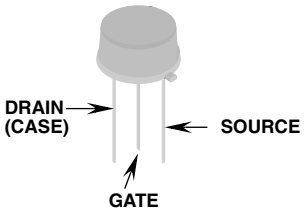
- 3.5A, 200V
- $r_{DS(ON)} = 0.800\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-205AF



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		2N6790	UNITS
Drain to Source Voltage	V_{DS}	200	V
Drain to Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200	V
Continuous Drain Current	I_D	3.5	A
$T_C = 100^oC$	I_D	2.25	A
Pulsed Drain Current	I_{DM}	14	A
Gate to Source Voltage	V_{GS}	±20	V
Continuous Source Current (Body Diode)	I_S	3.5	A
Pulse Source Current (Body Diode)	I_{SM}	14	A
Maximum Power Dissipation	P_D	20	W
Above $T_C = 25^oC$, Derate Linearly		0.16	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		200	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1.0mA		2	-	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200V, V_{GS} = 0V		-	-	250	µA
		V_{DS} = 160V, V_{GS} = 0V	$T_C = 125^oC$	-	-	1000	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0		-	-	100	nA
Drain to Source On-Voltage (Note 2)	$V_{DS(ON)}$	I_D = 3.5A, V_{GS} = 10V		-	-	2.8	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 2.25A, V_{GS} = 10V		-	.5	0.800	Ω
		I_D = 2.25A, V_{GS} = 10V	$T_C = 125^oC$	-	-	1.5	Ω
Diode Forward Voltage	V_{SD}	I_S = 3.5A, V_{GS} = 0V		0.7	-	1.5	V
Forward Transconductance (Note 2)	g_{fs}	I_D = 2.25A, V_{DS} = 5V		1.5	2.25	4.5	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V f = 1MHz		200	450	600	pF
Output Capacitance	C_{OSS}			60	150	300	pF
Reverse-Transfer Capacitance	C_{RSS}			15	40	80	pF
Turn-On Delay Time	$t_{d(ON)}$	I_D = 2.25A $V_{GS} \cong$ 74V, R_G = 50Ω		-	-	40	ns
Rise Time	t_r			-	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	50	ns
Fall Time	t_f			-	-	50	ns
Safe Operating Area	SOA	V_{DS} = 160V, I_D = 125mA		20	-	-	W
		V_{DS} = 5.7V, I_D = 3.5A		20	-	-	W
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	6.25	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	175	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, I_{SD} = 3.5A, dI_{SD}/dt = 100A/µs		350	-	ns
Reverse Recovered Charge	Q_{RR}	TJ = 150^oC, I_{SD} = 3.5A, dI_{SD}/dt = 100A/µs		2.3	-	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

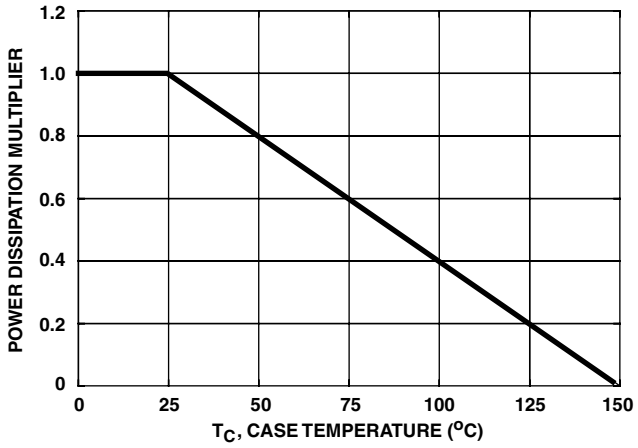


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

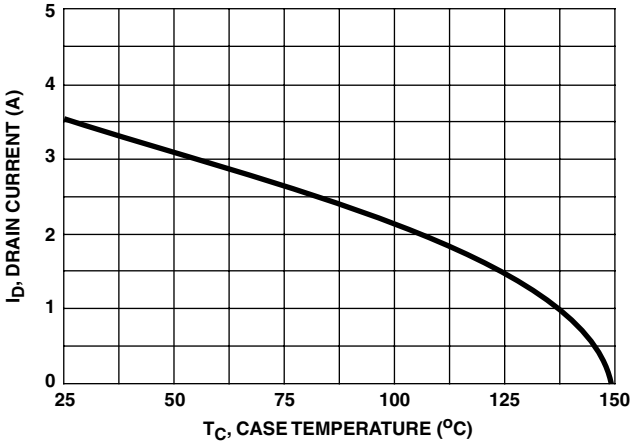


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

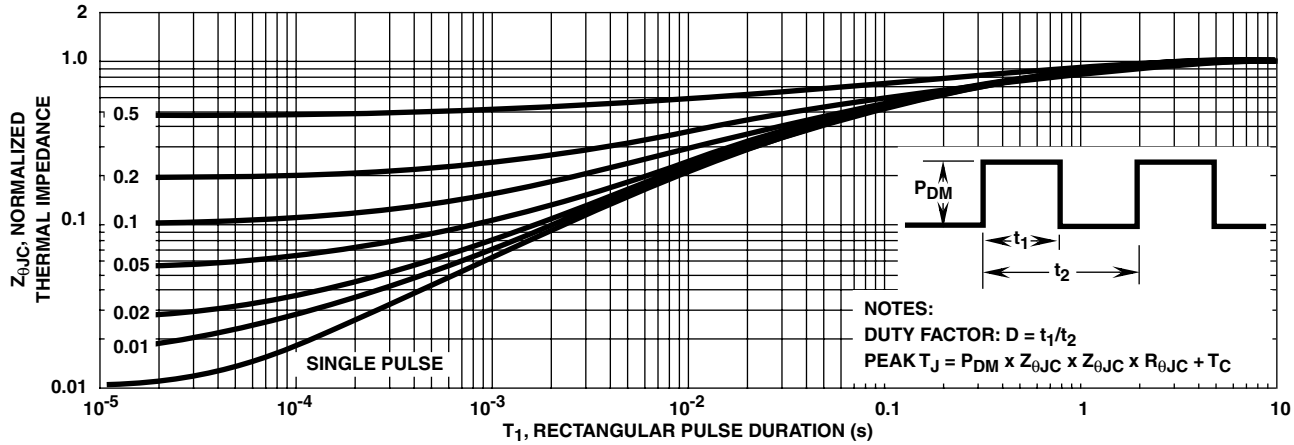


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

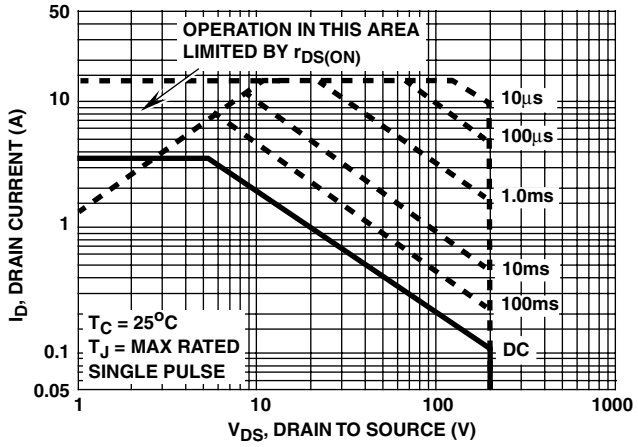


FIGURE 4. FORWARD BIAS SAFE OPERATING AREAS

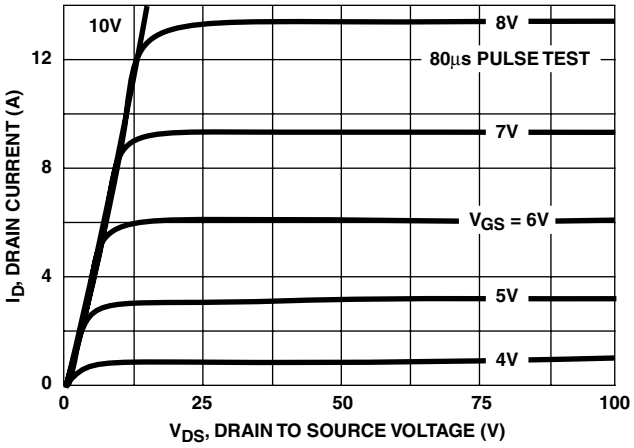


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

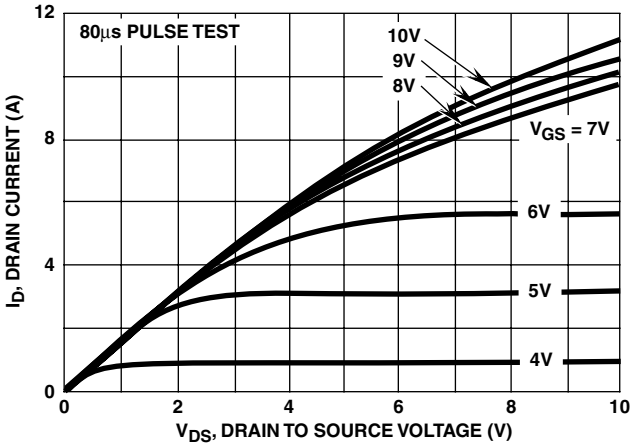


FIGURE 6. SATURATION CHARACTERISTICS

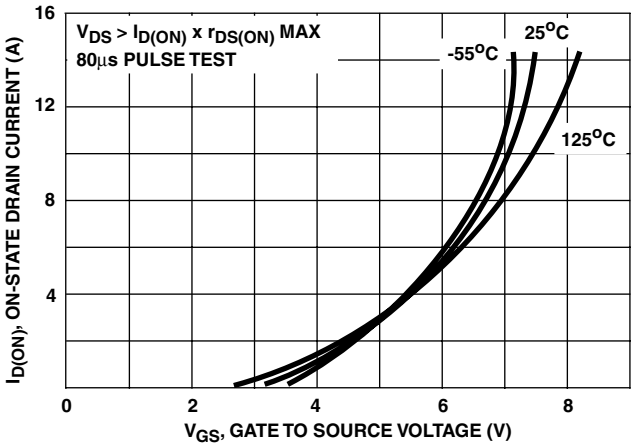


FIGURE 7. TRANSFER CHARACTERISTICS

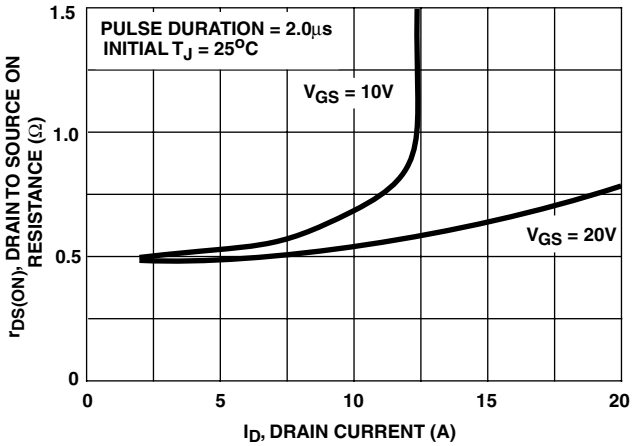


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

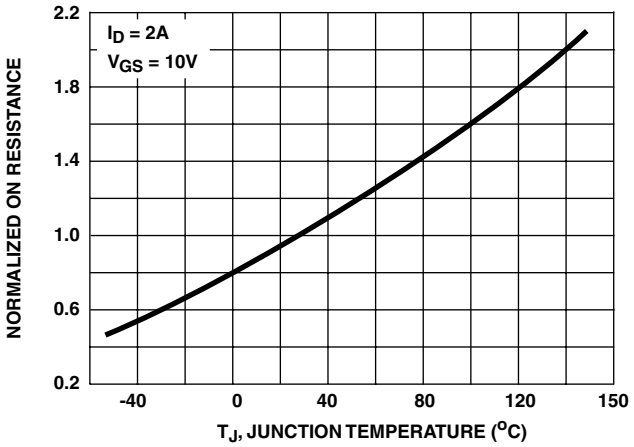


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

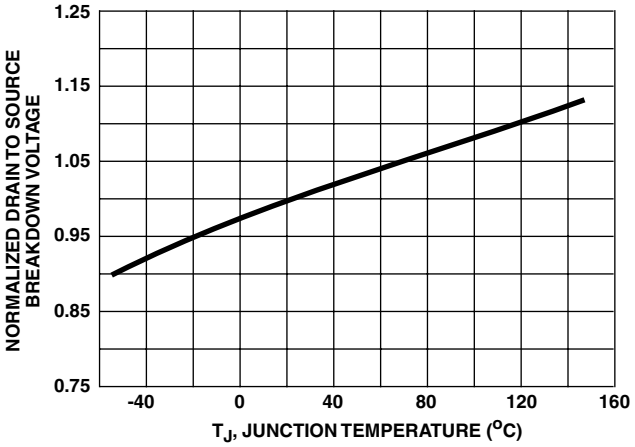


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

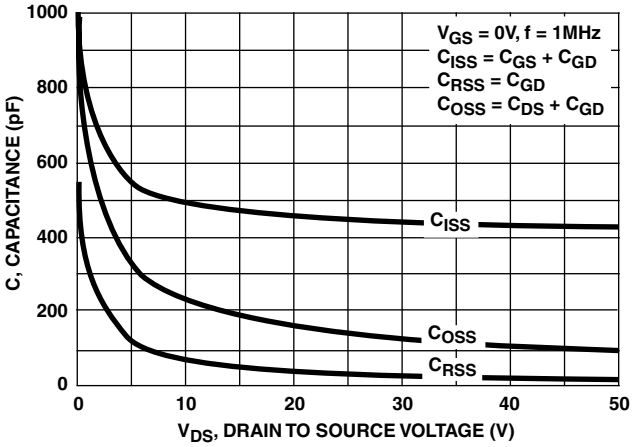


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

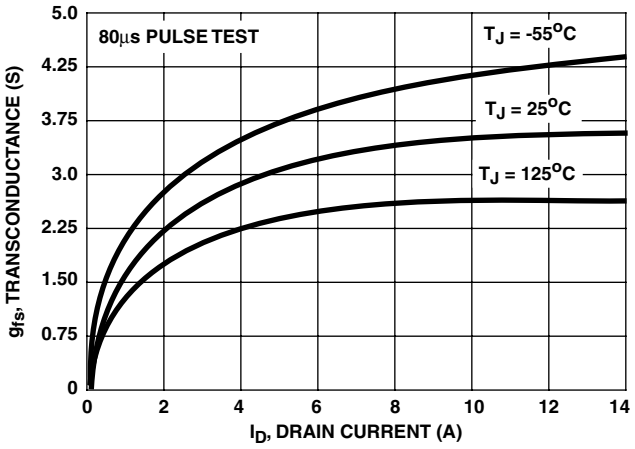


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

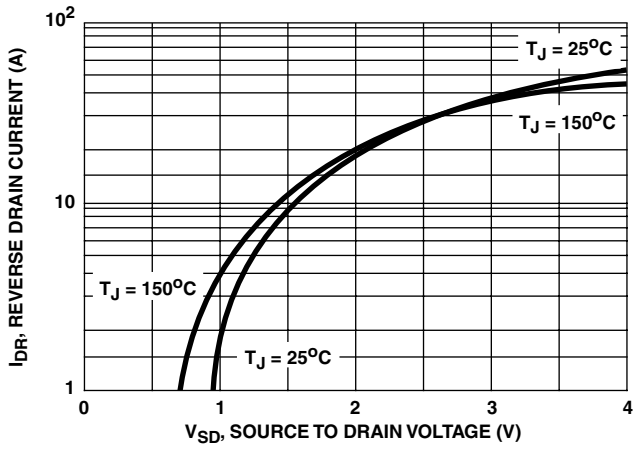


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

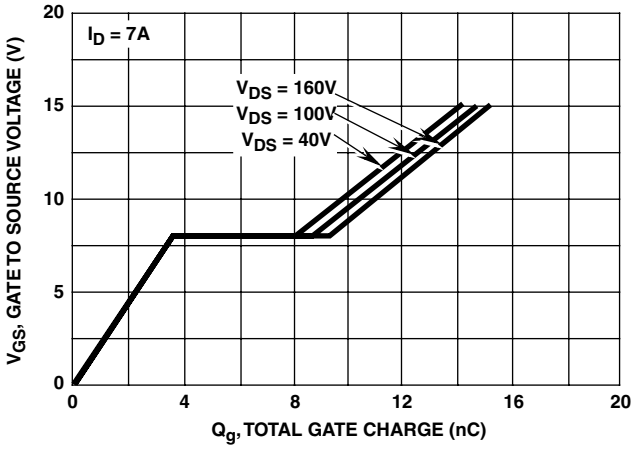


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

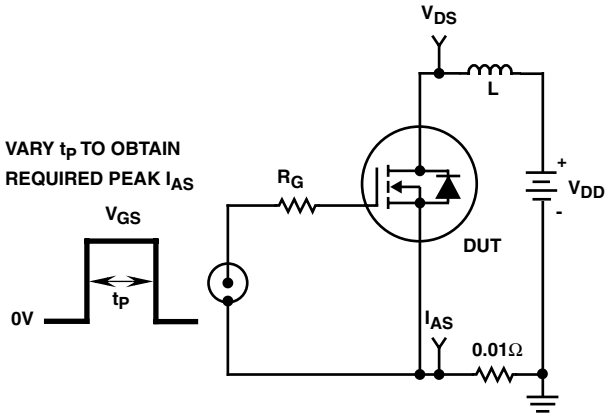


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

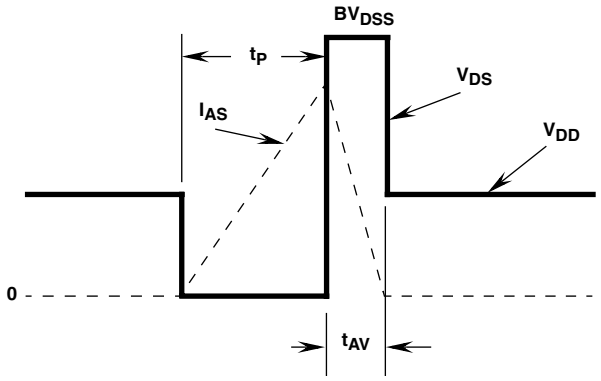


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

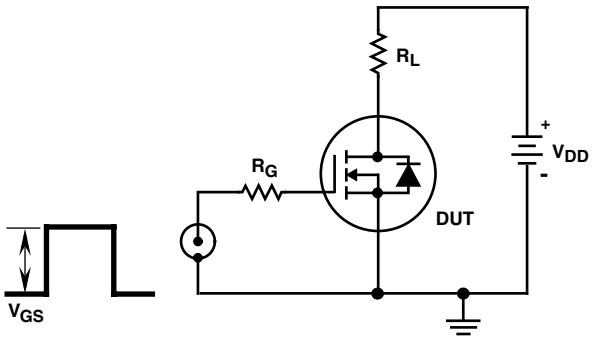


FIGURE 17. SWITCHING TIME TEST CIRCUIT

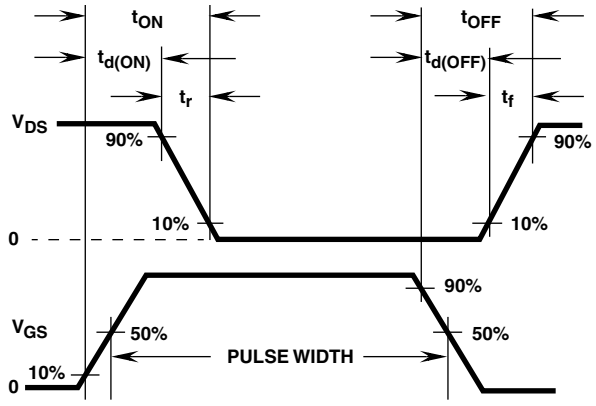


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

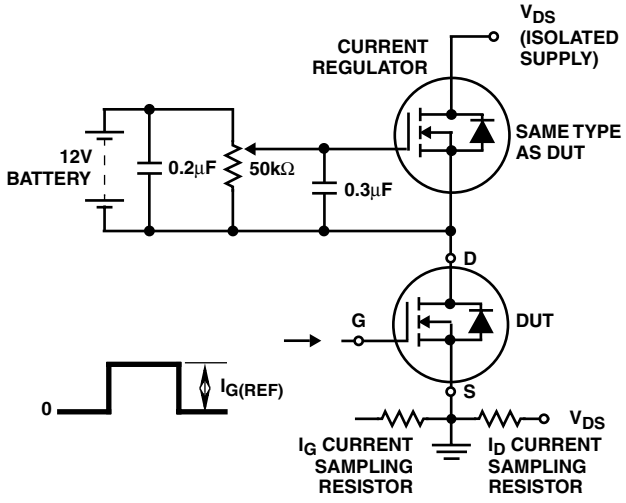


FIGURE 19. GATE CHARGE TEST CIRCUIT

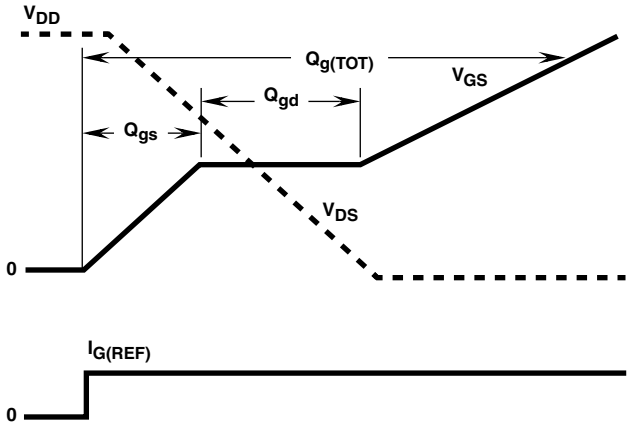


FIGURE 20. GATE CHARGE WAVEFORMS

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