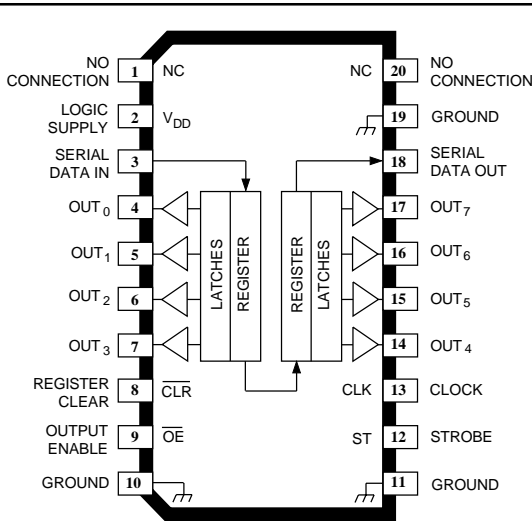


# 6B595

## ADVANCE INFORMATION

(Subject to change without notice)  
January 24, 2000

## 8-BIT SERIAL-INPUT, DMOS POWER DRIVER



Dwg. PP-029-12

Note that the A6B595KA (DIP) and the A6B595KLW (SOIC) are electrically identical and share a common terminal number assignment.

### ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

- Output Voltage,  $V_O$  ..... 50 V
- Output Drain Current,
  - Continuous,  $I_O$  ..... 150 mA\*
  - Peak,  $I_{OM}$  ..... 500 mA†
- Single-Pulse Avalanche Energy,
  - $E_{AS}$  ..... 30 mJ
- Logic Supply Voltage,  $V_{DD}$  ..... 7.0 V
- Input Voltage Range,
  - $V_I$  ..... -0.3 V to +7.0 V
- Package Power Dissipation,
  - $P_D$  ..... See Graph
- Operating Temperature Range,
  - $T_A$  ..... -40°C to +125°C
- Storage Temperature Range,
  - $T_S$  ..... -55°C to +150°C

\* Each output, all outputs on.

† Pulse duration  $\leq 100 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6B595KA and A6B595KLW combine an 8-bit CMOS shift register and accompanying data latches, control circuitry, and DMOS power driver outputs. Power driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads.

The serial-data input, CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Serial-data input rates are over 5 MHz. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial-data output enables cascade connections in applications requiring additional drive lines. Similar devices with reduced  $r_{DS(on)}$  are available as the A6595KA and A6595KLW.

The A6B595 DMOS open-drain outputs are capable of sinking up to 500 mA. All of the output drivers are disabled (the DMOS sink drivers turned off) by the OUTPUT ENABLE input high.

The A6B595KA is furnished in a 20-pin dual in-line plastic package. The A6B595KLW is furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads. Copper lead frames, reduced supply current requirements, and low on-state resistance allow both devices to sink 150 mA from all outputs continuously, to ambient temperatures over 85°C.

### FEATURES

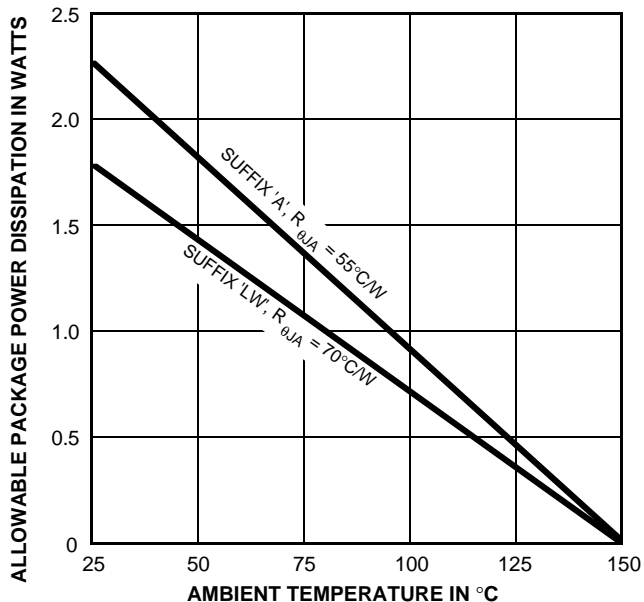
- 50 V Minimum Output Clamp Voltage
- 150 mA Output Current (all outputs simultaneously)
- 5  $\Omega$  Typical  $r_{DS(on)}$
- Low Power Consumption
- Replacements for TPIC6B595N and TPIC6B595DW

Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JC}$
A6B595KA	20-pin DIP	55°C/W	25°C/W
A6B595KLW	20-lead SOIC	70°C/W	17°C/W

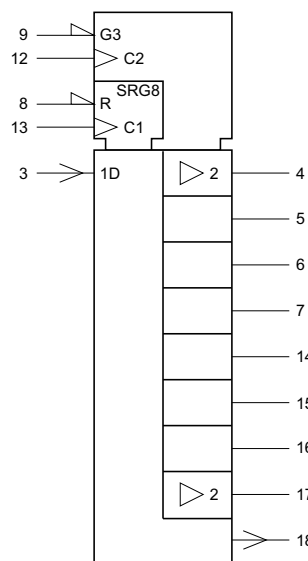
# 6B595

## 8-BIT SERIAL-INPUT, DMOS POWER DRIVER



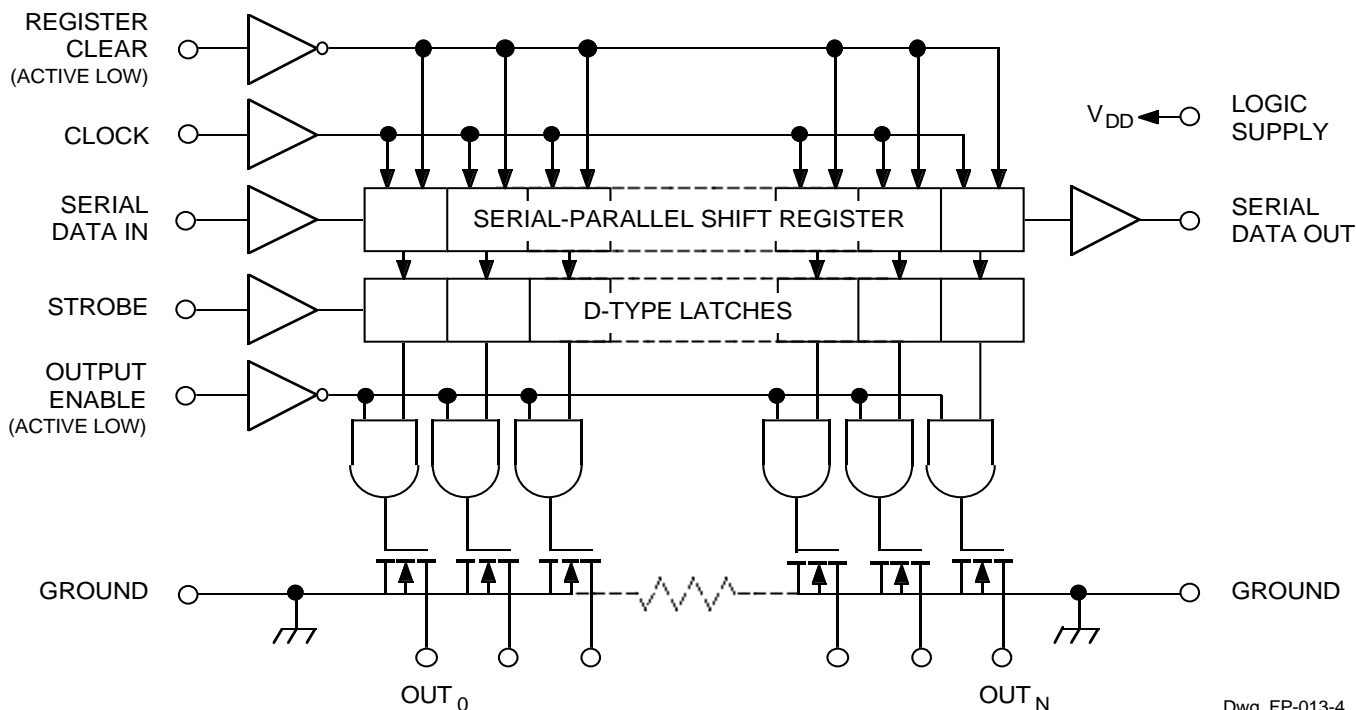
Dwg. GS-004A

### LOGIC SYMBOL



Dwg. FP-043

### FUNCTIONAL BLOCK DIAGRAM

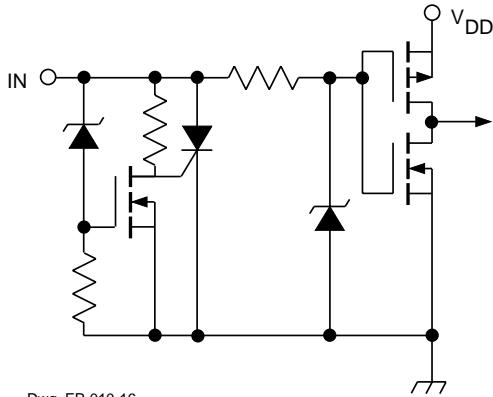


Dwg. FP-013-4

Grounds (terminals 10, 11, and 19) must be connected together externally.

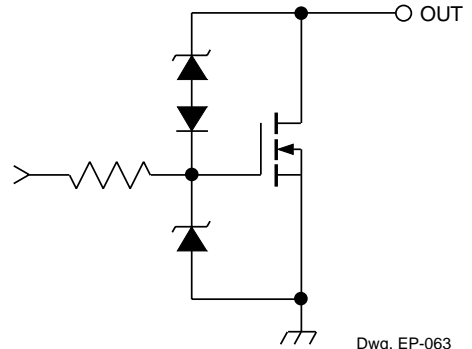
# 6B595

## 8-BIT SERIAL-INPUT, DMOS POWER DRIVER



Dwg. EP-010-16

**LOGIC INPUTS**



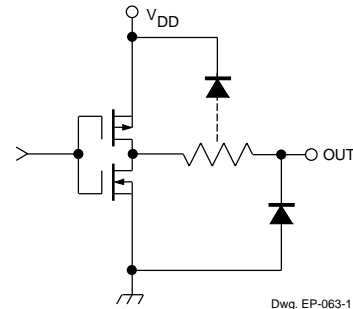
Dwg. EP-063

**DMOS POWER DRIVER OUTPUT**

### RECOMMENDED OPERATING CONDITIONS

over operating temperature range

Logic Supply Voltage Range,  $V_{DD}$  ..... 4.5 V to 5.5 V  
 High-Level Input Voltage,  $V_{IH}$  .....  $\geq 0.85V_{DD}$   
 Low-level input voltage,  $V_{IL}$  .....  $\leq 0.15V_{DD}$



Dwg. EP-063-1

**SERIAL DATA OUT**

### TRUTH TABLE

Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe	Latch Contents						Output Enable	Output Contents																				
		$l_0$	$l_1$	$l_2$	...	$l_6$	$l_7$			$l_0$	$l_1$	$l_2$	...	$l_6$	$l_7$		$l_0$	$l_1$	$l_2$	...	$l_6$	$l_7$															
H		H	$R_0$	$R_1$	...	$R_5$	$R_6$	$R_6$																													
L		L	$R_0$	$R_1$	...	$R_5$	$R_6$	$R_6$																													
X		$R_0$	$R_1$	$R_2$	...	$R_6$	$R_7$	$R_7$																													
		X	X	X	...	X	X	X	—			$R_0$	$R_1$	$R_2$	...	$R_6$	$R_7$																				
		$P_0$	$P_1$	$P_2$	...	$P_6$	$P_7$	$P_7$				$P_0$	$P_1$	$P_2$	...	$P_6$	$P_7$	L						$P_0$	$P_1$	$P_2$	...	$P_6$	$P_7$								
												X	X	X	...	X	X	H						H	H	H	...	H	H								

L = Low Logic Level    H = High Logic Level    X = Irrelevant    P = Present State    R = Previous State

# 6B595

## 8-BIT SERIAL-INPUT, DMOS POWER DRIVER

**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ ,  $t_{ir} = t_{if} \leq 10\text{ ns}$  (unless otherwise specified).**

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Breakdown Voltage	$V_{(BR)DSX}$	$I_O = 1\text{ mA}$	50	—	—	V
Off-State Output Current	$I_{DSX}$	$V_O = 40\text{ V}$ , $V_{DD} = 5.5\text{ V}$	—	0.1	5.0	$\mu\text{A}$
		$V_O = 40\text{ V}$ , $V_{DD} = 5.5\text{ V}$ , $T_A = 125^\circ\text{C}$	—	0.15	8.0	$\mu\text{A}$
Static Drain-Source On-State Resistance	$r_{DS(on)}$	$I_O = 100\text{ mA}$ , $V_{DD} = 4.5\text{ V}$	—	4.2	5.7	$\Omega$
		$I_O = 100\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ , $T_A = 125^\circ\text{C}$	—	6.8	9.5	$\Omega$
		$I_O = 350\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ (see note)	—	5.5	8.0	$\Omega$
Nominal Output Current	$I_{ON}$	$V_{DS(on)} = 0.5\text{ V}$ , $T_A = 85^\circ\text{C}$	—	90	—	mA
Logic Input Current	$I_{IH}$	$V_I = V_{DD} = 5.5\text{ V}$	—	—	1.0	$\mu\text{A}$
	$I_{IL}$	$V_I = 0$ , $V_{DD} = 5.5\text{ V}$	—	—	-1.0	$\mu\text{A}$
SERIAL-DATA Output Voltage	$V_{OH}$	$I_{OH} = -20\text{ }\mu\text{A}$ , $V_{DD} = 4.5\text{ V}$	4.4	4.49	—	V
		$I_{OH} = -4\text{ mA}$ , $V_{DD} = 4.5\text{ V}$	4.0	4.2	—	V
	$V_{OL}$	$I_{OL} = 20\text{ }\mu\text{A}$ , $V_{DD} = 4.5\text{ V}$	—	0.005	0.1	V
		$I_{OL} = 4\text{ mA}$ , $V_{DD} = 4.5\text{ V}$	—	0.3	0.5	V
Prop. Delay Time	$t_{PLH}$	$I_O = 100\text{ mA}$ , $C_L = 30\text{ pF}$	—	150	—	ns
	$t_{PHL}$	$I_O = 100\text{ mA}$ , $C_L = 30\text{ pF}$	—	90	—	ns
Output Rise Time	$t_r$	$I_O = 100\text{ mA}$ , $C_L = 30\text{ pF}$	—	200	—	ns
Output Fall Time	$t_f$	$I_O = 100\text{ mA}$ , $C_L = 30\text{ pF}$	—	200	—	ns
Supply Current	$I_{DD(OFF)}$	$V_{DD} = 5.5\text{ V}$ , Outputs OFF	—	20	100	$\mu\text{A}$
	$I_{DD(ON)}$	$V_{DD} = 5.5\text{ V}$ , Outputs ON	—	150	300	$\mu\text{A}$
	$I_{DD(fclk)}$	$f_{clk} = 5\text{ MHz}$ , $C_L = 30\text{ pF}$ , Outputs OFF	—	0.4	5.0	mA

Typical Data is at  $V_{DD} = 5\text{ V}$  and is for design information only.

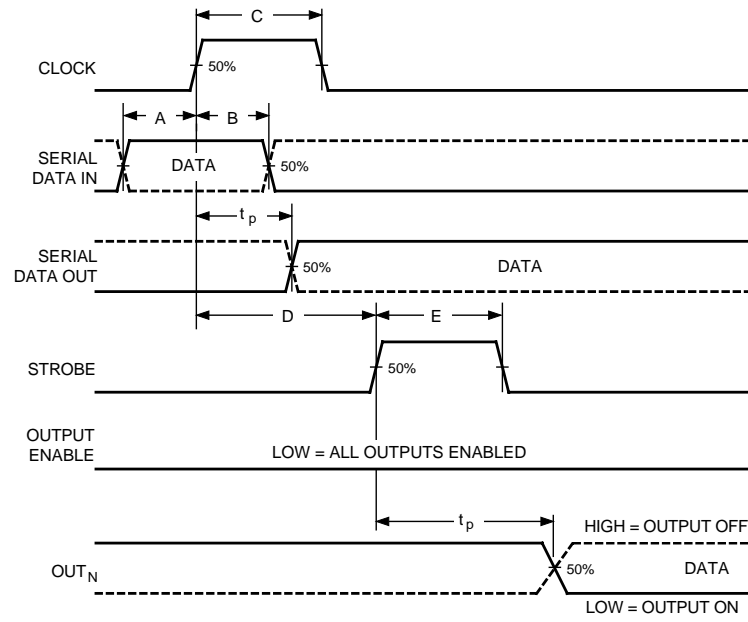
NOTE — Pulse test, duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

# 6B595

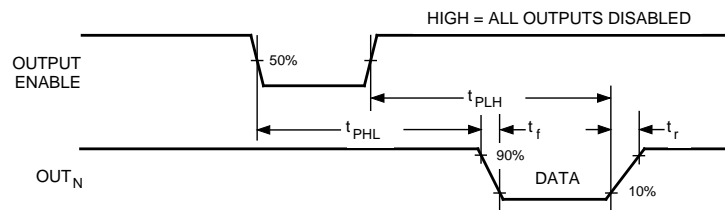
## 8-BIT SERIAL-INPUT, DMOS POWER DRIVER

### TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are  $V_{DD}$  and Ground)



Dwg. WP-029-2



Dwg. WP-030-2

- A. Data Active Time Before Clock Pulse**  
(Data Set-Up Time),  $t_{su(D)}$  ..... **20 ns**
- B. Data Active Time After Clock Pulse**  
(Data Hold Time),  $t_{h(D)}$  ..... **20 ns**
- C. Clock Pulse Width,  $t_{w(CLK)}$  ..... **40 ns****
- D. Time Between Clock Activation**  
and Strobe,  $t_{su(ST)}$  ..... **50 ns**
- E. Strobe Pulse Width,  $t_{w(ST)}$  ..... **50 ns****
- F. Output Enable Pulse Width,  $t_{w(OE)}$  ..... **4.5  $\mu$ s****

NOTE – Timing is representative of a 12.5 MHz clock.  
Higher speeds are attainable.

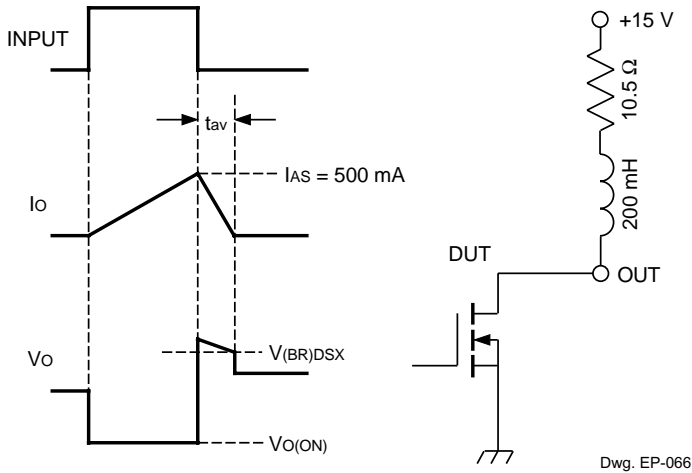
Serial data present at the input is transferred to the shift register on the rising edge of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT.

Information present at any register is transferred to the respective latch on the rising edge of the STROBE input pulse (serial-to-parallel conversion).

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

**6B595**  
**8-BIT SERIAL-INPUT,**  
**DMOS POWER DRIVER**

**TEST CIRCUITS**



$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

**Single-Pulse Avalanche Energy Test Circuit  
and Waveforms**

**6B595**  
**8-BIT SERIAL-INPUT,**  
**DMOS POWER DRIVER**

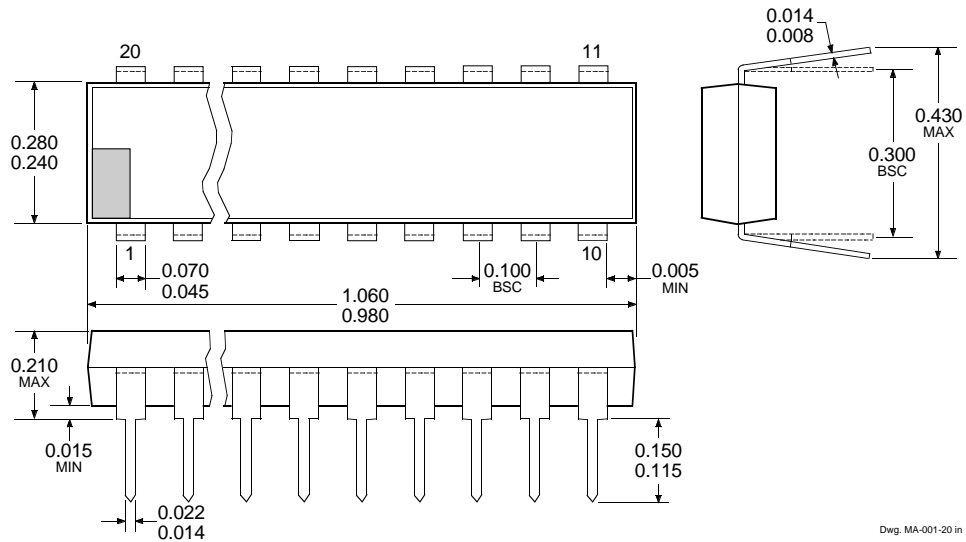
**TERMINAL DESCRIPTIONS**

<b>Terminal No.</b>	<b>Terminal Name</b>	<b>Function</b>
1	NC	No internal connection.
2	LOGIC SUPPLY	(V <sub>DD</sub> ) The logic supply voltage (typically 5 V).
3	SERIAL DATA IN	Serial-data input to the shift-register.
4-7	OUT <sub>0-3</sub>	Current-sinking, open-drain DMOS output terminals.
8	CLEAR	When (active) low, the registers are cleared (set low).
9	OUTPUT ENABLE	When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
10	GROUND	Reference terminal for output voltage measurements (OUT <sub>0-3</sub> ).
11	GROUND	Reference terminal for output voltage measurements (OUT <sub>0-7</sub> ).
12	STROBE	Data strobe input terminal; shift register data is latched on rising edge.
13	CLOCK	Clock input terminal for data shift on rising edge.
14-17	OUT <sub>4-7</sub>	Current-sinking, open-drain DMOS output terminals.
18	SERIAL DATA OUT	CMOS serial-data output to the following shift register.
19	GROUND	Reference terminal for input voltage measurements.
20	NC	No internal connection.

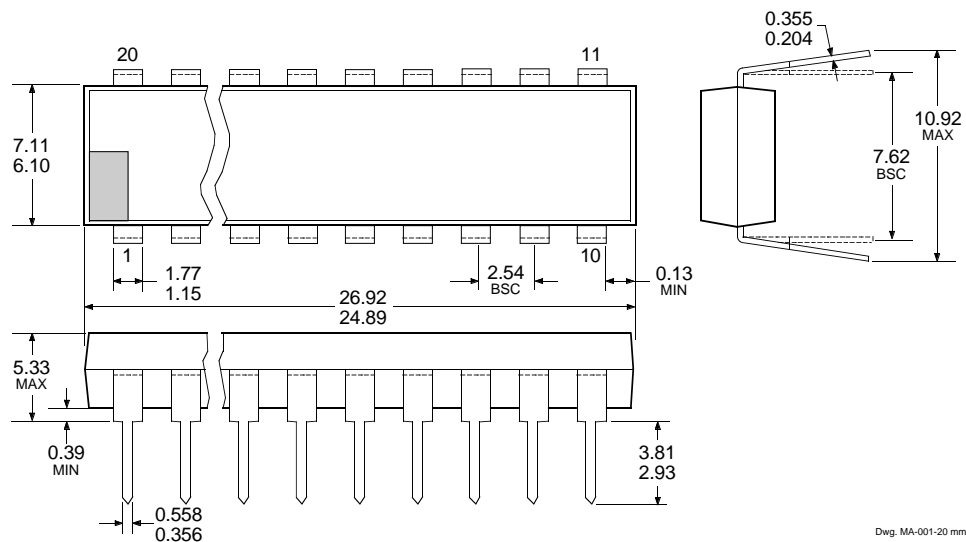
NOTE — Grounds (terminals 10, 11, and 19) must be connected together externally.

**6B595**  
**8-BIT SERIAL-INPUT,**  
**DMOS POWER DRIVER**

**A6B595KA**  
 Dimensions in Inches  
 (controlling dimensions)



Dimensions in Millimeters  
 (for reference only)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
 2. Lead spacing tolerance is non-cumulative  
 3. Lead thickness is measured at seating plane or below.

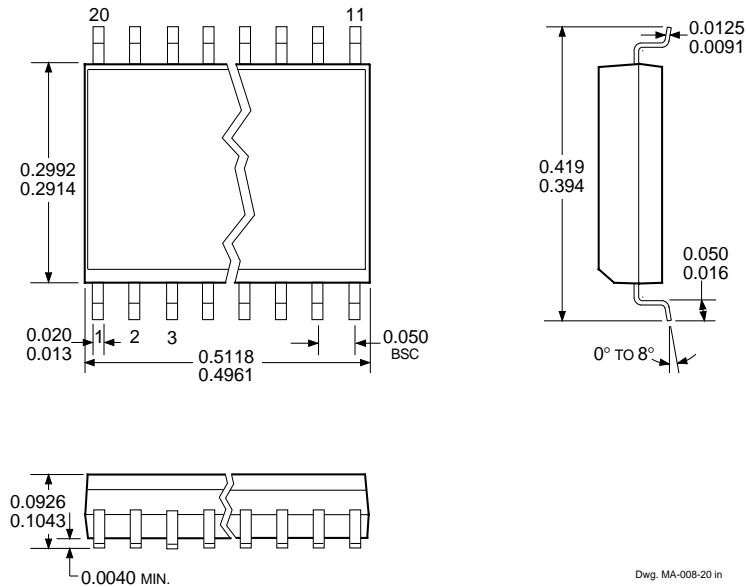


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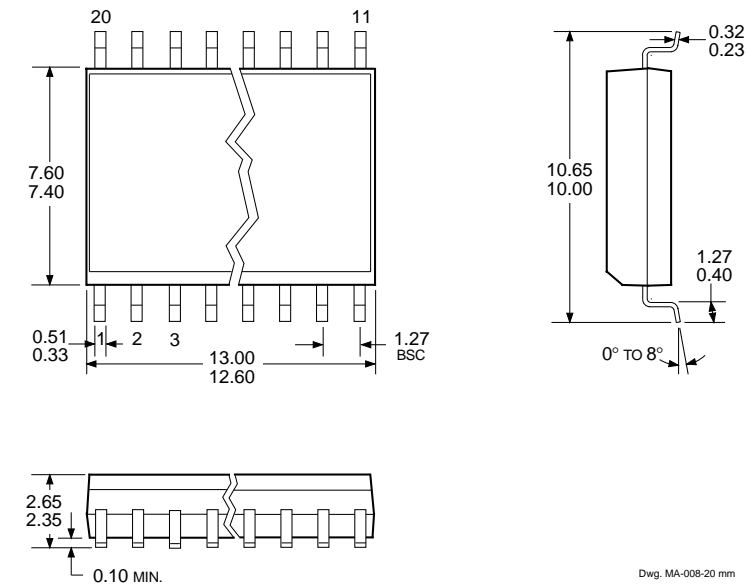
## 8-BIT SERIAL-INPUT, DMOS POWER DRIVER

### A6B595KLW

Dimensions in Inches  
(for reference only)



### Dimensions in Millimeters (controlling dimensions)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.

**6B595**  
***8-BIT SERIAL-INPUT,***  
***DMOS POWER DRIVER***

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***8-BIT SERIAL-INPUT,  
DMOS POWER DRIVER***

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**6B595**  
**8-BIT SERIAL-INPUT,**  
**DMOS POWER DRIVER**

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